Development of prototype components for the Silicon Tracking System of the CBM experiment at FAIR

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Abstract

The CBM experiment at future accelerator facility FAIR will investigate the properties of nuclear matter under extreme conditions. The experimental programm is different from the heavy-ion experiments at RHIC (BNL) and LHC (CERN) that create nuclear matter at high temperatures. In contrast, the study of the QCD phase diagram in the region of the highest net baryon densities and moderate temperatures that is weakly explored will be performed with high precision. For this, collisions of different heavy-ion beams at the energies of 10–45 GeV/nucleon with nuclear target will be measured.

The physics programme of the CBM experiment includes measurement of both rare probes and bulk observables that originate from various phases of a nucleus-nucleus collision. In particular, decay of particles with charm quarks can be registered by reconstructing the decay vertex detached from the primary interaction point by several hundreds of micrometers (e.g., decay length $c\tau = 123\,\mu\mathrm{m}$ for D^0 meson). For this, precise tracking and full event reconstruction with up to 600 charged particle tracks per event within acceptance are required. Other rare probes require operation at interaction rate of up to 10 MHz. The detector system that performs tracking has to provide high position resolution on the order of 10 µm, operate at high rates and have radiation tolerant design with low material budget.

The Silicon Tracking System (STS) is being designed for charged-particle tracking in a magnetic field. The system consists of eight tracking station located in the aperture of a dipole magnet with 1 T field. For tracks with momentum above 1 GeV, momentum resolution of such a system is expected to be about 1%. In order to fulfill this task, thorough optimization of the detector design is required. In particular, minimal material budget has to be achieved.

Production of a detector module requires research and development activities with respect to the module components and their integration. A detector module is a basic functional unit that includes a sensor, an analogue microcable and front-end electronics mounted on a support structure. The objective of the thesis is to perform quality assurance tests of the prototype module components in order to validate the concept of the detector module and to demonstrate its operation using radioactive sources and particle beams.

Double-sided silicon microstrip detectors have been chosen as sensor technology for the STS because of the combination of a good spatial resolution, two-dimensional coordinate measurement achieved within low material budget

(0.3%X_0), high readout speed and sufficient radiation tolerance. Several generations of double-sided silicon microstrip sensors have been manufactured in order to explore the radiation hard design features and the concept of a large-area sensor compatible with ladder-type structure of the detector module. In particular, sensors with double metal layer on both sides and active area of $62 \times 62\,\mathrm{mm}^2$ have been produced. Electrical characterization of the sensors has been performed in order to establish the overall operability as well as to extract the device parameters. Current-voltage, capacitance-voltage characteristics and interstrip parameters have been measured.

Readout of the sensors has been done using self-triggering front-end electronics. A front-end board has been developed based on the n-XYTER readout chip with data driven architecture and capable of operating at 32 MHz readout rate. The front-end board included an external analog-to-digital converter (ADC). Calibration of the ADC has been performed using both ^{241}Am X-ray source and external pulse generator. Threshold calibration and investigation of temperature dependence of chip parameters has been carried out.

Low-mass support structures have been developed using carbon fibre that has the rigidity to hold the detector modules and introduce minimal Coulomb scattering of the particle tracks. Analogue microcables have been produced with aluminium traces on a polyimide substrate, thus combining good electrical connection with low material budget. Microcable structure includes several layers optimized for low trace capacitance and thus low-noise performance.

A demonstrator tracking telescope has been constructed and operated in several beam tests including 2.5 GeV proton beam at COSY synchrotron (Jülich). Three tracking stations have been complemented with several beam hodoscopes. Analysis of the beam data has yielded information on analogue and timing response, beam profile. Tracking and alignment information has been obtained. Beam stability has been evaluated using specially developed monitoring tools.

As a result of conducted studies, performance of the module components have been evaluated and requirements to the detector module have been formulated. Practical suggestions have been made with respect to the structure of the detector module, whereas precise definition of the final detector module design was outside of the scope of this thesis.

Kurzfassung

Das CBM-Experiment an der zukünftigen Beschleunigeranlage FAIR wird die Eigenschaften von Kernmaterie unter extremen Bedingungen untersuchen. Das experimentelle Programm unterscheidet sich von den Schwerionen-Experimenten an RHIC (BNL) und LHC (CERN), die Kernmaterie bei hohen Temperaturen erzeugen. Im Gegensatz dazu kann die Untersuchung des QCD-Phasendiagramms, im Bereich der höchsten Nettobaryonendichten und moderaten Temperaturen, die nur schwach untersucht wurden, mit hoher Präzision durchgeführt werden. Hierzu werden Kollisionen der verschiedenen Schwerionenstrahlen, bei Energien von 10-45 GeV/Nukleon, mit nuklearem Target gemessen.

Das physikalische Programm des CBM Experimentes umfasst die Messung sowohl der seltenen Sonden als auch der Mengenobservablen, die aus verschiedenen Zeitphasen des Zusammenstoßes der Kerne stammen. Insbesondere kann der Zerfall von Teilchen mit Charm-Quarks durch Rekonstruktion des Zerfallsvertex, versetzt von dem primären Wechselwirkungspunkt um mehrere hundert Mikrometer (z.B. $c\tau = 123\,\mu\text{m}$ für D^0 meson), registriert werden. Hierzu ist präzises Tracking bei voller Ereignisrekonstruktion, mit bis zu 600 Spuren der geladenen Teilchen pro Ereignis innerhalb der Akzeptanz, nötig. Andere seltene Sonden erfordern den Betrieb bei einer Wechselwirkung von bis zu 10 MHz. Das Detektor-System, dass Tracking durchführt, muss eine hohe Ortsauflösung, auf der Ebene von 10 µm leisten, mit hohen Arbeitsgeschwindigkeiten zu betreiben sein und ebenso ein strahlungstolerantes Design mit geringem Materialbudget besitzen.

Das Silicon Tracking System (STS) wurde entwickelt um die Spuren geladener Teilchen in einem Magnetfeld zu rekonstruieren. Das System besteht aus acht Tracking Stationen, die sich in der Öffnung eines Dipolmagneten mit 1 T Feld befinden. Bei Spuren mit Impulsen über 1 GeV, beträgt die Impulsauflösung bei einem solchen System etwa 1%. Um diese Aufgabe erfüllen zu können, ist eine sorgfältige Optimierung des Detektordesigns erforderlich. Insbesondere muss ein minimales Materialbudget erreicht werden.

Die Herstellung eines Detektor-Moduls erfordert Forschungs- und Entwicklungsaktivitäten mit Bezug auf die Modul-Komponenten und deren Integration. Ein Detektor-Modul ist eine grundlegende funktionelle Einheit, die einen Sensor, ein Analog-Mikrokabel und Front-End-Elektronik umfasst, montiert auf einer Trägerstruktur. Das Ziel der Arbeit ist es, die Qualitätssicherungstests der Prototyp-Modulkomponenten, zur Bestätigung des Detektor-Modul-Konzeptes durchzuführen, und um seinen Betrieb mit radioaktiven Quellen und Teilchenstrah-

len zu demonstrieren.

Die doppelseitigen Silizium-Mikrostreifendetektoren wurden als Sensortechnik für den STS, aufgrund der Kombination einer guten Ortsauflösung, einer zweidimensionalen Koordinatenmessung mit geringem Materialbudget ($0.3\% X_0$), der hohen Auslesegeschwindigkeit und ausreichender Strahlungstoleranz gewählt. Mehrere Generationen von doppelseitigen Silizium-Mikrostreifendetektoren wurden zur Erkundung strahlenharter Konstruktionsmerkmale und des Konzepts, eines großflächigen Sensors und dessen Kompatibilität mit der Leiter-Struktur des Detektor-Moduls, hergestellt. Insbesondere wurden Sensoren mit doppelter Metallschicht auf beiden Seiten und aktivem Bereich von $62 \times 62\,\mathrm{mm}^2$ produziert. Die elektrische Charakterisierung der Sensoren wurde durchgeführt, um die gesamte Bedienbarkeit sowie die Extrahierung der Geräteparameter feststellen zu können. Strom- und Kapazitäts-Spannungs-Charakteristiken sowie Interstreifenparameter wurden gemessen.

Das Auslesen der Sensoren wurde mithilfe einer selbstgetriggerten Front-End-Elektronik getätigt. Ein Front-End-Board wurde auf der Grundlage eines n-XYTER-Auslesechips mit datengesteuerter Architektur entwickelt, der geeignet ist bei Auslesegeschwindigkeit von 32 MHz betrieben zu werden. Die Front-End-Platine enthält einen externen Analog-zu-Digital-Wandler (ADC). Die Kalibrierung des ADC wurde unter Verwendung von sowohl ^{241}Am Röntgenquelle als auch eines externen Impulsgenerators vorgenommen. Die Schwellenkalibrierung und Untersuchung der Temperaturabhängigkeit der Chip-Parameter wurden durchgeführt.

Die ultraleichten Halterungsstrukturen wurden aus Kohlefaser entwickelt, diese haben die Steifigkeit, die Detektor-Module halten, und die minimale Coulomb-Streuung der Teilchenspuren einbeziehen zu können. Es wurden Analog-Mikrokabel mit Aluminiumleiterbahnen auf einem Polyimidsubstrat produziert, also eine Kombination von guter elektrischer Verbindung und geringem Materialbudget. Die Mikrokabelstruktur umfasst mehrere Lagen optimiert für die niedrige Kapazität der Leiterbahnen und den damit verbundenen geräuscharmen Betrieb.

Es wurde ein Demonstrator-Tracking-Teleskop gebaut und in mehreren Strahltests, einschließlich 2.5 GeV Protonenstrahl an COSY Synchrotron (Jülich), betrieben. Drei Tracking-Stationen wurden mit mehreren Hodoskopen ergänzt. Die Datenanalyse ergab Informationen über Analog- und Zeitverhalten sowie Strahlenprofil. So wurden Tracking- und Alignmentinformationen erhalten. Mit speziell entwickelten Monitoring-Tools wurde die Strahlstabilität bewertet.

Als Ergebnis der durchgeführten Studien, wurde die Leistung der Modulkomponenten bewertet und die Anforderungen zum Detektormodul formuliert. Praktische Vorschläge wurden im Hinblick auf die Struktur des Detektormoduls gemacht. Die genaue Definition des endgültigen Detektormoduldesigns jedoch, war außerhalb des Geltungsbereichs dieser Arbeit.

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Chapter 1

Introduction

According to the present understanding of the earliest moments of the evolution of the universe, matter existed at very high temperatures and densities presumably in the form of a so called quark-gluon plasma (QGP). The equation of state (EoS) of nuclear matter relates pressure to the temperature and chemical potentials of the constituent particle species. In heavy-ion collisions, pressure is a key component for the description of the collective behavior of a QGP within a hydrodynamic approach, e.g., flow. In cosmology, the precise knowledge of pressure or the equation of state is necessary for the description of the evolution of the predicted primordial gravitational waves [1], density of dark matter candidates [2] or the interior structure of neutron stars [3].

Collisions of heavy ions at high energies will enable the investigation of a phase transition from partonic degrees of freedom (where chiral symmetry is restored and quarks are in a deconfined state) to hadronic degrees of freedom (with broken chiral symmetry). It is conjectured that this phenomenon can occur at matter densities several times larger than normal nuclear density. This state of matter, the quark-gluon plasma, is believed to be the dominant form of matter in the universe at the time scale of the order of a few microseconds after the Big Bang.

Employing heavy-ion collisions at (ultra-)relativistic energies aims at creating "mini Big Bangs" in the laboratory. This enables performing studies of fundamental aspects of QCD thermodynamics such as the equation-of-state of strongly interacting matter. It is expected that the properties of hadronic states are changed in a nuclear environment. The studies aim at the structure of the strongly interaction matter as a function of temperature and baryonic density in order to localize the phase transition between hadronic and partonic phases.

It is believed that at high baryon-chemical potentials matter undergoes a first order phase transition from a deconfined to a hadronic state, while at small μ_B a crossover occurs. This indicates the existence of a critical point at the end of the transition line. The phase boundary between quark-gluon plasma and hadronic matter is widely studied within the lattice QCD framework. Significant progress in the QCD calculations have recently lead to the consolidation of the critical temperature. Lattice QCD calculations agree on a critical temperature at around

175 MeV at $\mu_B = 0$ [4]. However, the existence or non-existence of a critical point at finite μ_B is still subject of a hot dispute [5].

The region of low beam energies is of great interest, because critical point and first order phase transition are potentially accessible there. Experiments were started in the early 1980s [6, 7]. Later on, experiments at RHIC (e.g., STAR [8], PHENIX [9]) turned to studying the properties of QGP matter at very high temperatures and low baryon densities, i.e., high beam energies. At LHC, the dedicated heavy-ion experiment ALICE, but also CMS and ATLAS have started the exploration of heavy-ion collisions at even higher energies. Recently, experimental programmes at low beam energy range have been taken up at RHIC (Brookhaven, New York) ("beam energy scan") and again at SPS (CERN, Geneva) (NA61 experiment). New experimental programmes are being prepared at NICA [10] (JINR, Dubna) and FAIR (GSI, Darmstadt). Different models of the hot and dense matter have been developed to understand signal which could characterize the QGP. Some of them are modification of characteristics short-lived states, e.g., invariant mass, width, cross-section (strangeness enhancement, charm suppression). The usual way of presenting these observables illustrating QGP properties is to compare their behavior in matter and in vacuum. Experimentally, one compares measurements in heavy-ion collisions and in collisions of light systems, e.g., proton-proton collisions.

These studies, extensively developing at the LHC experiment ALICE [11], have resulted in claiming that partonic degrees of freedom prevail in the early phase of the fireball evolution. Among the interesting features observed in ALICE, is jet suppression in di-jet events [12].

The phase diagram of QCD matter is presented in Fig. 2.1 and further discussed in the next chapter. The accessible region of RHIC and LHC experiments is located at high temperatures and low baryo-chemical potentials. The important feature of this diagram is the critical temperature and the first order phase transition line separating the hadronic phase from the partonic one phase. In order to search for features like the critical endpoint, the predicted first-order phase transition and the chiral phase transition, moderate temperatures and high baryo-chemical potentials must be achieved and experimentally accessed [13]. This is going to be realized in the experimental programme of the Compressed Baryonic Matter (CBM) experiment at the SIS-300 and initially the SIS-100 synchrotrons at FAIR. The Facility for Antiproton and Ion Research (FAIR) [14] is now (July 2012) under construction at GSI (Darmstadt, Germany). The CBM experiment will perform measurements of hadronic and leptonic channels. The observables, including rare probes, require novel experimental techniques such as a high-throughput free-streaming data acquisition concept with online event selection, and low-mass, fast and radiation hard detectors. The development of components for one of the detector systems, the Silicon Tracking System for the trajectory measurement of all charged particles and their momentum determination, is in the focus of this paper.

Chapter 2

Physics of the Compressed Baryonic Matter experiment

The goal of the heavy-ion experiments is to investigate the properties of strongly interacting nuclear matter. The state of matter is represented in terms of the QCD phase diagram that can be explored in the ultra-relativistic heavy-ion collisions towards higher temperatures and net baryon densities. The observables of the phase transition between deconfined and hadronic matter are discussed and requirements to the detector are formulated.

2.1 The QCD phase diagram

The state of the nuclear matter is described in terms of thermodynamical parameters temperature (T) and baryochemical potential (μ_B). At normal nuclear density and temperature, quarks are combined into hadrons (baryons or mesons) according to the confinement principle. At high temperature and density, hadrons "dissolve" into a mixture of quarks and gluons that can move freely. This state of matter where effective degrees of freedom change from hadrons to partons is referred to as quark-gluon plasma (QGP). Baryochemical potential is a measure of net baryon density. Due to large energy scale, particle creation is possible and number of particles is not conserved as opposed to the net number of baryons.

The current understanding of the QCD phase diagram has reached advanced level. A sketch of the phase diagram is shown in Fig. 2.1 [15]. Along with the basic features such as the first order phase transition, critical point and crossover region that separate hadronic and the QGP phase, existence of additional phases is predicted theoretically.

The nature of the phase transition depends on the path on the diagram. In the region of low net baryon densities and high temperatures explored in lattice QCD calculations, transition is expected to be a smooth crossover. At moderate temperatures and high net baryon densities, first order phase transition is predicted. Change of the transition nature between these two regimes of the phase transition is denoted by a critical point where strong fluctuations of the physical parameters occur.

Apart from the deconfinement phase transition, chiral phase transition is predicted. Transition from chirally symmetric matter at high temperatures and net baryon densities to the state with broken chiral symmetry is associated with conversion of the light ("massless") quarks into massive hadrons. Chiral and deconfinement phase transitions are not necessarily equivalent. Chirally restored and confined matter is referred to as quarkyonic matter.

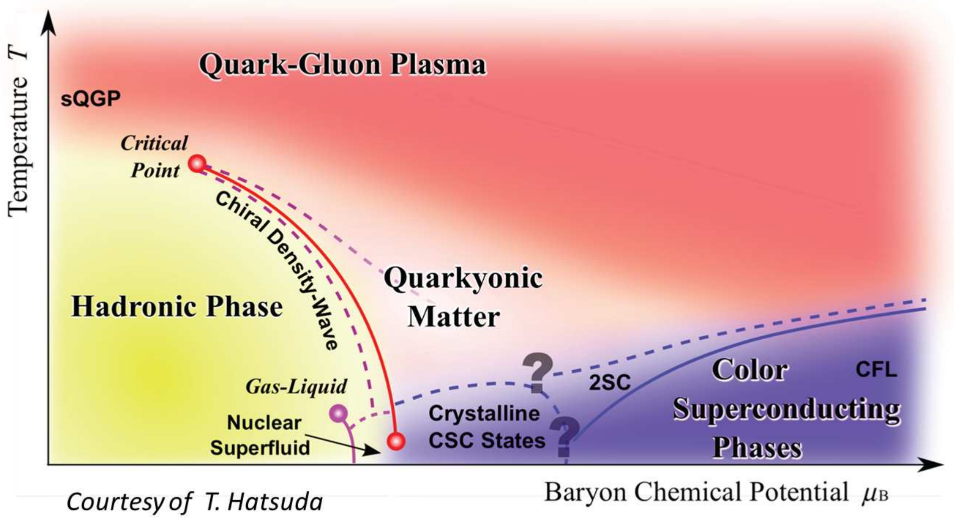


Figure 2.1: Schematic view of the phase diagram of strongly interacting matter represented in the plane of temperature and baryochemical potential. Different phases are shown in different colours. Lines denote phase transitions of different types.

A further phase transition is anticipated at low temperatures and net baryon densities. Matter in this form is represented by the nucleons that are bound into atomic nuclei. As temperature increases, nucleons cannot be held together by the binding forces. This is described as a transition of the matter from the liquid to the gas phase.

At low temperatures and net baryon densities well above nuclear density, quarks are conjectured to form Cooper pairs that condensate. Due to analogy with superconductivity in metals, this state of matter, possibly existing in the interiors of the neutron stars, is called colour superconducting condensate.

Observables are necessary to study the properties of strongly interacting matter in the region of the phase transitions. The CBM experiment at FAIR is designed to explore this region. The CBM experiment will enter a new era of nuclear matter research by measuring rare diagnostic probes never observed before, and thus has a unique discovery potential. In order to obtain a complete picture, a comprehensive set of observables will be measured in proton–proton, proton–nucleus and nucleus–nucleus collisions over the FAIR energy range. At SIS-100, collision energy will reach $\sqrt{s_{NN}} = 1.8 - 4\,\text{GeV}$ and at SIS-300 $\sqrt{s_{NN}} = 4.9 - 9\,\text{GeV}$. Particularly at the SIS-300 energies, the creation of the densest collision systems is predicted.

2.2 Observables

The key observables for the CBM experiment are discussed in this section. The in-depth description of the CBM physics programme is given in [16]. The signals for possible formation of quark-gluon plasma and potential for their measurement at CBM are discussed in [17].

2.2.1 Strangeness production

The first proposed phase transition signals were related to the enhancement of strange particles yield [18, 19]. Strange quarks, which are not present in the initial nuclei, are formed by the reaction. Therefore the formation of strange particles has substantial information about the environment formed during the nucleus-nucleus collisions. The basic idea is to compare yields of strange (especially multi-strange) particles in the nucleus-nucleus collisions with those in proton-proton or proton-nucleus collisions. Experimental data from SPS and RHIC [20–23] have confirmed these predictions. However, interpretation of the observed data remains controversial. Papers [24] and [25] present different explanation of that phenomena.

Experimental measurements of K/π ratio as a function of the centrality are required for clarification whether this enhancement is associated with thermalization or whether other mechanisms are responsible for it (including QGP formation). In particular, the beam energies at SIS-100/300 can provide the opportunity to make detailed studies of this value.

The experiments on strangeness production at GSI [26, 27] demonstrated how kaons can be used as diagnostic probes both for the properties of compressed nuclear matter and for the modifications of hadrons inside the dense medium. It turned out that the sensitivity of the kaon probe to medium properties is strongly enhanced if the beam energy is below the kaon production threshold energy in nucleon-nucleon collisions. Dynamical transport models play a crucial role in the extraction of the relevant physics information from the heavy-ion data. Transport calculations have shown a reasonable degree of consistency concerning K^+ meson production and dynamics. The comparison of theory to experiment concerning total yields, momentum distributions, and the collective flow pattern supports the existence of a slightly repulsive in-medium K^+N potential of $V_{K^+} = 25 \pm 5\,\text{MeV}$ at nuclear saturation density as predicted by chiral dynamics. This result is supported by data on K^+ meson production in proton-nucleus collisions [28, 29]. It was demonstrated that K^+ mesons provide information on the compressibility of nuclear matter at densities up to 2-3 times saturation density. In proton-nucleus collisions – where the strangeness exchange process $\pi Y \rightarrow K^-N$, where $Y = \Lambda, \Sigma$, is strongly suppressed – the measured K^-/K^+ ratio can be reproduced with an attractive in-medium K^-N potential of $V_{K^-} = -80 \pm 20\,\mathrm{MeV}$ at saturation density [29,30].

Microscopic coupled-channel calculations based on a chiral Lagrangian predict a dynamical broadening of the K-meson spectral function in dense nuclear matter [31,32]. Off-shell transport calculations using K^- meson spectral functions have been performed [33]. The ultimate goal of the calculations is to relate the in-medium spectral function of K^- mesons to the anticipated chiral symmetry restoration at high baryon density.

2.2.2 Charm production

Another observable considered as a candidate for physics signal of the QGP is related to charm production [34,35]. Due to the difference of dissociation temperature of different states of the charmonium, it is expected that sequential melting of ψ' and J/ψ might serve as a signal of the onset of deconfinement. The in-medium modification of D-mesons opens the decay of ψ' mesons into $D\bar{D}$ pairs, and, hence, contributes to the suppression of ψ' mesons. Within the statistical hadronization model (SHM), in-medium mass modifications of open charm hadrons can be considered at the phase boundary.

As far as the radii of charm mesons are comparable with the average distance between partons in QGP (about 0.2–0.5 fm) at temperatures around few hundred MeV, the cross-section of the charm production is considered as a possible probe of the determination of the stage of the deconfinement. Paper [36] indicates that a high density of gluons in a QGP originating from the ultra-relativistic heavy-ion collisions would destroy all charmonium created beforehand, similarly to Debye screening in electromagnetic plasma. In this way, charmonium suppression has been proposed as a signal of the quark gluon plasma. However, there are theoretical models which are able to reproduce experimental observation of charmonium suppression [37] as charmonium absorbtion by nuclear environment and breakup by comoving hadrons [38–40]. Therefore, the interpretation of the data on charmonium suppression remains ambiguous and studies of charmonium production are subject to future investigation at the CBM. A precise measurement of the excitation function of the ψ' to J/ψ ratio in central Au+Au collisions will shed light on the charmonium absorption processes in dense matter. A smooth excitation function is expected for comover absorption, whereas sequential charmonium melting in the QGP would cause a structure in the excitation function of the ψ' to J/ψ ratio.

Further progress requires new data on the yields and phase-space distributions of charmonia, charmed mesons, and charmed baryons as function of beam energy and collision centrality in p+A and A+A collisions. The measurement of ratios of hadrons containing charm quarks as a function of beam energy may provide direct evidence for a deconfinement phase transition. For instance, Fig. 2.2 depicts the ratio of J/psi over the sum of D and $\bar{D}$ mesons (for central Au+Au collisions) as a function of available energy in the nucleon-nucleon system as predicted by the HSD [41] hadronic transport model, and by the statistical hadronization model [42]. The SHM assumes complete dissociation of charmonium in the quark-gluon plasma, followed by statistical production of J/ψ mesons (and particles with open charm) during hadronization.

For a typical FAIR beam energy of $\sqrt{s_{NN}} = 7\,\mathrm{GeV}$ the hadronic transport model (HSD) predicts a J/ψ over $D+\bar{D}$ ratio which is about 5 times larger than the result of the statistical hadronization model (see Fig. 2.2).

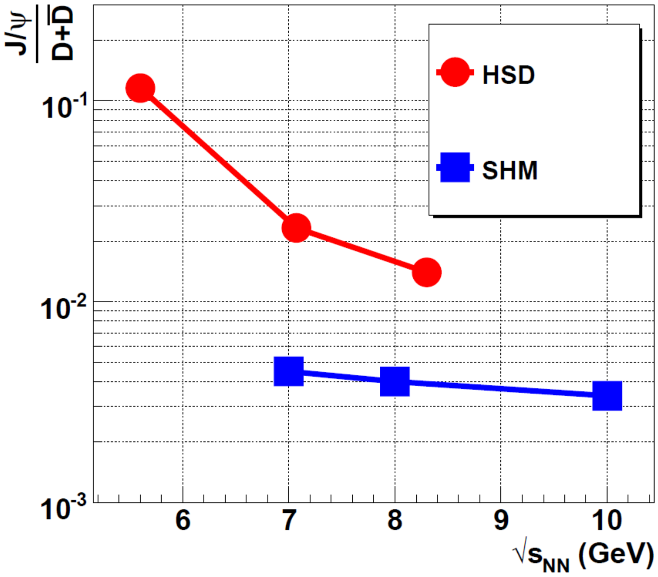


Figure 2.2: Ratio of J/ψ over $D+\bar{D}$ mesons as a function of center-of-mass energy in the nucleon-nucleon system predicted for central Au+Au collisions by the HSD transport model and by the statistical hadronization model SHM which assumes a QGP initial state. For the vector mesons (ρ, ω, ϕ, J/ψ, ψ') decay into lepton pairs was assumed, for D mesons the hadronic decay into kaons and pions.

2.2.3 Low-mass vector mesons

One reason for the high interest in studies of light vector mesons (ρ, ω and ϕ mesons) resulting from heavy ion collisions is the fact that the specific properties of some light vector mesons, such as short lifetime and dilepton decay modes, allocate them as a unique class of samples for the study of different segments of time, hot and dense medium, which was formed as a result of a collision. Photons and lepton pairs are not involved in strong interactions and their spectra practically are not affected by final state interactions. Therefore they bear information about the hot and dense matter phase. The ability to compare dilepton decay channels to hadronic decay channels will enable the understanding what processes dominate at different stages of fireball evolution. Leptonic decay products will test the hypothesis of chiral symmetry restoration, which probably occurs during the formation of strongly coupled QGP.

2.2.4 Elliptic flow

Collective flow of matter that expands appear in the spectra of emitted hadrons and strongly depend on the properties of strongly interacting dense matter, ie the equation of state. In the analysis of experimental data distinguishes between several types of flow: elliptic azimuthally asymmetric flow arising from the initial almond shape overlap area of two nuclei in noncentral collisions, as well as radial flow. Transverse collective flow which was one of the first observables, proposed as probes of hot and dense matter [43, 44]. The data from RHIC [45] show a "saturation" of elliptic flow between $\sqrt{s} = 63$ and 200 GeV, which was proposed as a signal of strongly interacting quark-gluon plasma. Another important issue is whether or not hadron elliptic flow "remembers" its partonic origin. As suggested by data obtained at RHIC, the observed strength of elliptic flow scaled not with hadron masses but with the number of constituent quarks, regardless of content of quark flavors. Is this scaling violated below certain beam energy? This is a question to be determined by the CBM experiment. To answer this question one needs to scan the elliptic flow of pions, kaons, ϕ-mesons, charmonium and nucleons, (multi) strange hyperons and charmed hyperons (including their antiparticles) as a function of energy. Such studies are planned in the CBM experiment.

2.2.5 Fluctuations

A phase transition from a quark-gluon plasma can cause fluctuations of certain observables such as particle multiplicities, yield ratios, transverse momenta, rapidity, etc. To a certain extent, these effects are not destroyed by subsequent thermalization in the hadron gas. This can signal the effects of the phase transition.

Experimentally, only a small difference is observed in terms of dynamic fluctuations of transverse momentum p_t in AA collisions relative to pp after scaling the number of participants of the collision and the average transverse momentum of particles [47,48]. Measurements by the STAR collaboration of dynamic p_t fluctuations in AA collisions do not provide any evidence of the expected strong increase of fluctuations near the critical point [49]. However, in view of predictions of the critical point in the energy range $10 \leq \sqrt{s_{NN}} \leq 60$ GeV [50,51] it can be expected that a larger reduction in net charge fluctuations at low energies which will be investigated in the CBM experiment can serve as guidance for a QGP formation threshold above the critical point. If the freeze-out in strongly interacting system occurs near the critical point, the observed fluctuations in non-statistical distributions in the momenta of particles and correlations among baryons can increase. This has been observed at SPS (CERN)for the K/π yield ratios in central collisions of lead nuclei at energies ranging between $\sqrt{s_{NN}} = 6.3$ GeV and 17.3 GeV [52]. The microscopic hadron/string transport model UrQMD [53] does not reflect a signal increase that may indicate the emergence of new sources of fluctuations. Non-monotonic appearance and then disappearance of any fluctuations will be strong evidence of the critical point. A simultaneous observation the non-statistical fluctuations for different observables measured event-by-event for the low energies can be considered an unequivocal evidence of the discovery of the critical point.

2.3 Experimental requirements

In order to meet its physics goals, the CBM detector will have to reconstruct bulk observables as well as rare signals, e.g., open charm and low-mass vector mesons in a high multiplicity and high rate environment. This challenge is illustrated in Fig. 2.3, where tracks from one Au+Au collision at beam energy of 25 AGeV are shown. In order to reconstruct up to 1000 charged tracks created in such collisions, the CBM detector has to feature high granularity and a low-mass design of the tracking and vertexing detectors.

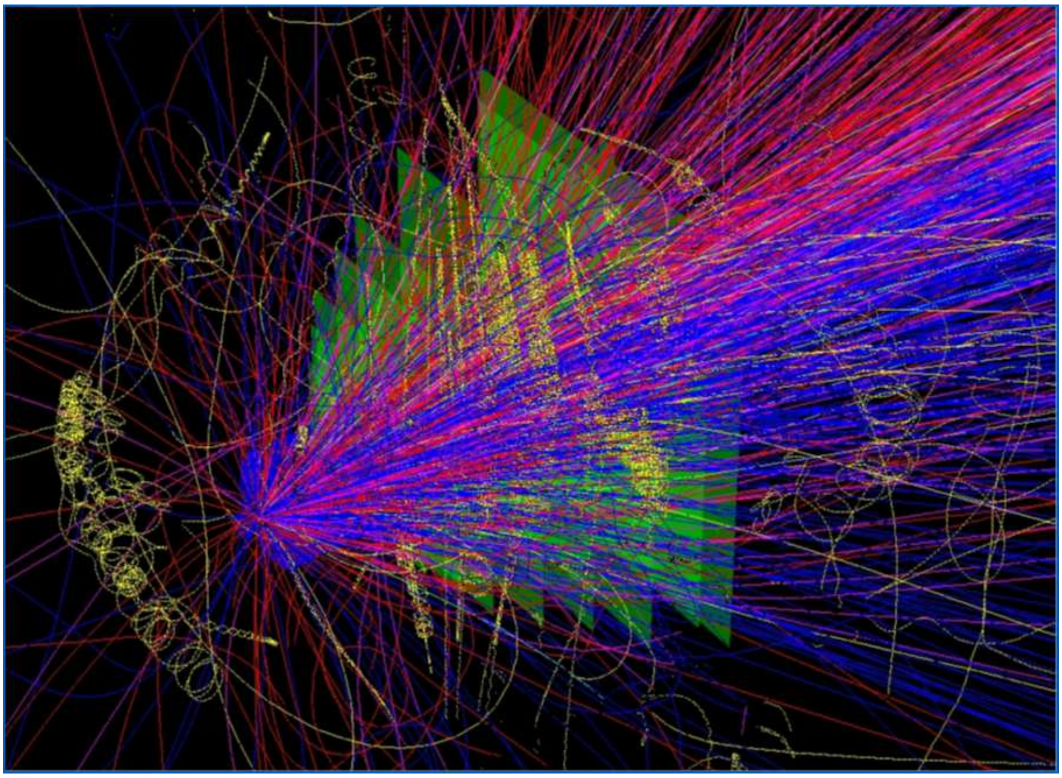


Figure 2.3: Particles produced in a central Au+Au collision at 25 AGeV. Particle properties are simulated with UrQMD event generator and transported through the detector geometry using Geant3 code.

The yields of the particles created in a Au+Au collision at 25 AGeV beam energy are shown in Fig. 2.4. Data points below the line correspond to particles that have not yet been measured at the highest baryon densities. The rare observables drive the requirement of the high interaction rate. Thus, the CBM experiment needs to have fast readout and radiation hard detectors.

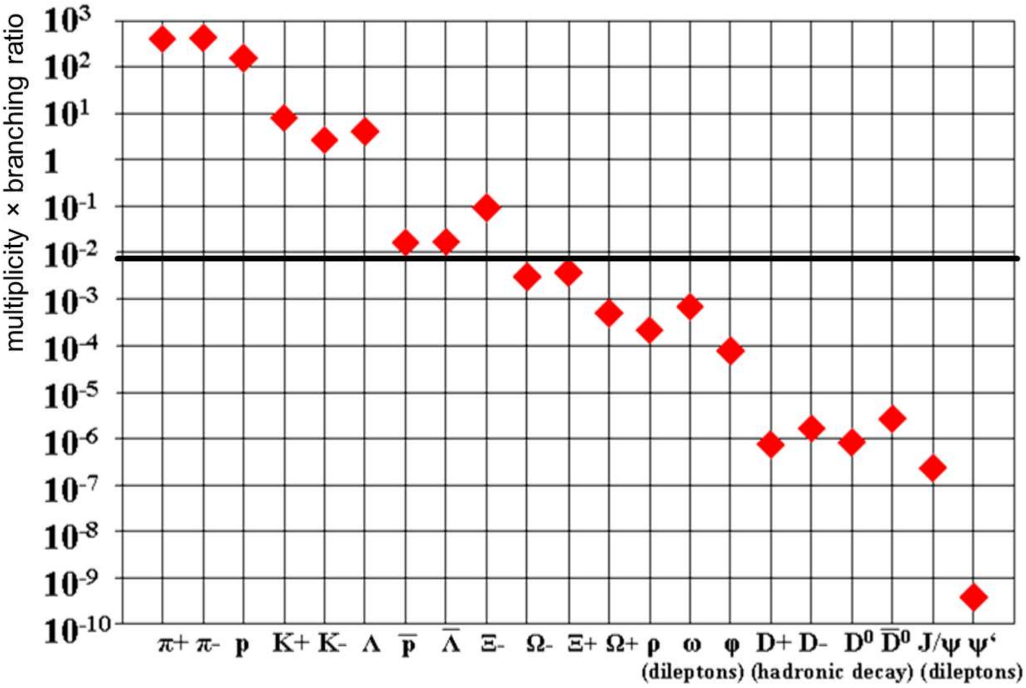


Figure 2.4: Multiplicity - branching ratio product for particles produced in minimum bias Au+Au collision at 25 AGeV.

The measurement procedure consists of track reconstruction with a high-granularity detector, reconstruction of particle decay vertices and measurement of yields for identified particles. As a result, the detector has to reconstruct particles and their properties (mass, momentum, particle type, etc). The mass of the particles has to be reconstructed with a precision high enough to be sensitive to the predicted mass shifts. The yields have to be measured with high signal-to-background ratio. The secondary vertex resolution has to be about 50 µm to provide reliable separation of detached vertices from the primary vertex. In order to fulfill the experimental requirements, the CBM detector has to provide tracking, vertexing, particle identification for the charged particles as well as energy measurement for photons.

Tracking and vertexing detectors have to operate in the magnetic field to provide particle momentum measurement with about 1% momentum resolution. A dipole magnet with 1 Tm bending power is required for this. Measurement of photons will be provided by an electromagnetic calorimeter.

Measurement of rare processes requires experimental operation at high interaction rates. This leads to the requirement of high segmentation in order to reduce channel occupancy and pile-up probability, in particular for the detectors located close to the interaction point, e.g., STS and MVD. As a consequence of high interaction rates reaching up to 10 MHz, radiation hardness of the silicon detectors has to be sufficient to stand fluence up to $4 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$ which will be accumulated in 6 years of operation. Fast tracking requires front-end electronics with shaping time of about 20 ns (for fast channel). Due to random interaction times in a DC beam, the event reconstruction is based on four-dimensional tracking [54], which requires explicit event association with time stamp precision of 1 ns.

The requirement on momentum resolution $\delta p/p \sim 1\%$ limits the material budget of the silicon tracking detector modules to $< 1\% X_0$. For the vertexing detector, open charm measurement requires even lower material budget of $< 0.3\% X_0$.

Chapter 3

The CBM detector

In order to realize the physics goals presented in the previous section, experimental setup has to allow measurements of flow of protons, pions, kaons, hyperons, hadronic resonances, light vector mesons, charmonium and open charm. One has to measure multiplicities, phase-space distributions, their correlations and event-by-event fluctuations in heavy-ion collisions. This introduces a new challenge to the CBM experiment: to identify both, hadrons and leptons, and to filter out rare probes at reaction rates of up to 10 MHz with charged particle multiplicities of up to 1000 per event. This technical specification cannot be matched by earlier developed detectors based on, e.g., Time-Projection Chambers (TPC) or similar devices. One has to build fast and radiation hard detector modules which have to provide lepton identification, high-resolution secondary vertex determination and at speed compatible with the high rate requirements.

Studies presented in this dissertation are related to the Compressed Baryonic Matter (CBM) experiment, planned for the construction at Facility for Antiproton and Ion Research (FAIR). Layout of the FAIR facility is shown in Fig. 3.1. The heavy-ion beam energies range from 10 GeV/nucleon to 45 GeV/nucleon. Studies of the QCD phase diagram will be performed exploring main physical observables as well as properties of rare decays (e.g., light vector mesons). Besides the studies of the QCD phase diagram at high baryonic densities, it is expected to get information on the properties of dense nuclear matter as well as first order phase transition from partonic to hadronic matter. It is necessary to identify signals from the partonic phase, coexistence of phases or critical point which survive passing through hadronization phase. It is clear that those species which are created at early stage of the fireball evolution and are weakly interacting with any participants are the most suitable candidates for such signals. Among them are excitation functions and flow of strangeness, charm, low mass lepton pairs, modification of elliptic flow as well as fluctuations and correlations.

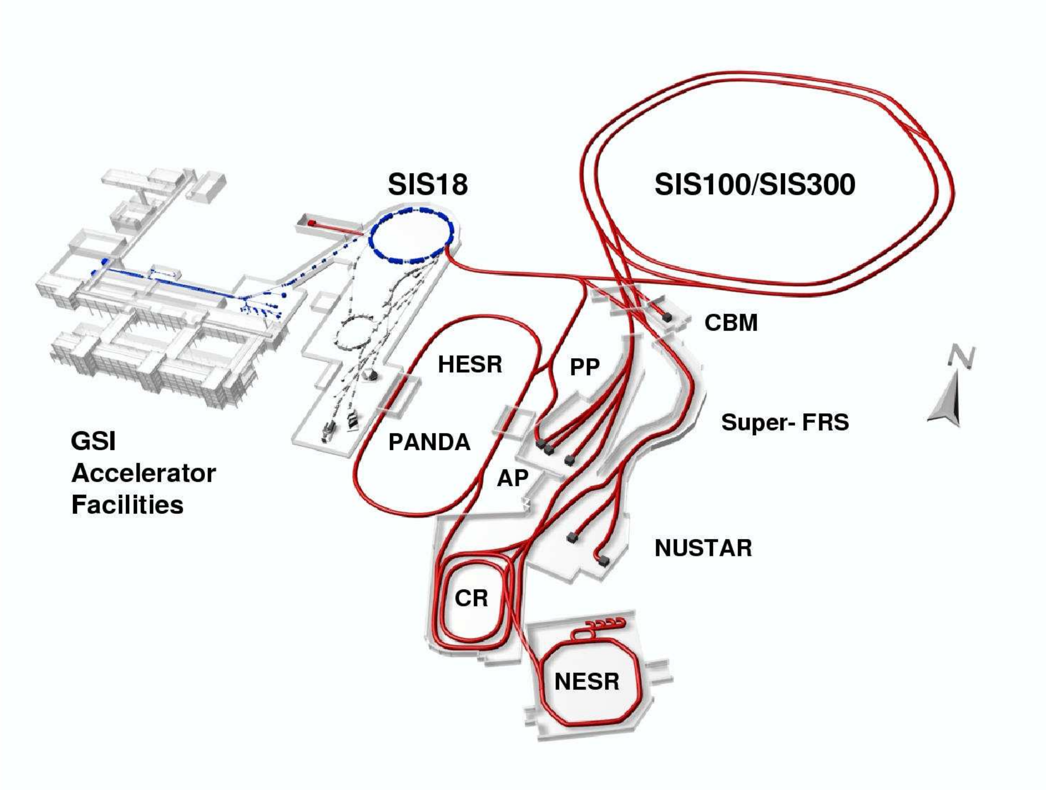


Figure 3.1: Layout of the FAIR facility. The double synchrotron SIS-100/300 directly provides the nuclear beams for the CBM experiment. In parallel operation, it transports the secondary beams of antiprotons or rare nuclear isotopes from a production target to the new fragment separator (super FRS). These beams are subsequently stored and further manipulated in special purpose storage rings, such as the HESR for antiproton research at the PANDA detector or for nuclear structure and atomic and plasma physics investigations at the other rings.

The layout of the CBM experiment which is expected to be efficient for fulfilling such specification is shown in Figs. 3.2 and 3.3 [55]. The central task in the experiment belongs to tracking. This will be provided by Silicon Tracking System (STS) and Micro Vertex Detector (MVD). Evaluation studies of earlier built experiments has brought an idea to build STS based on silicon microstrip detectors (single- and double-sided). Since CBM is going to measure rare probes, one has to reconstruct physical events in the environment of huge background with high accuracy of track reconstruction. That implies that one has to build a low-mass tracking system. STS will consist of low-mass silicon microstrip detectors which have to provide unambiguous space point measurement. The STS allows track reconstruction with a precision of about 15 µm in a wide momentum range from about 100 MeV/c up to more than 10 GeV/c with a momentum resolution of about 1%. The Micro Vertex Detector will be used for determination of secondary vertices with precision better than 5 µm, for instance to identify charmed mesons [56]. The MVD will be constructed from ultra-thin and highly-granulated Monolithic Active silicon Pixel Sensors (MAPS) which are placed in close vicinity to the target.

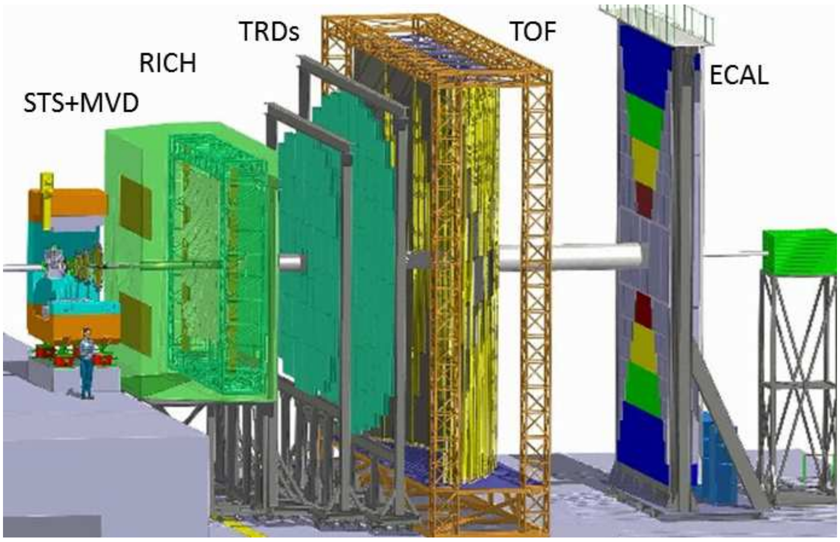


Figure 3.2: The CBM detector in electron-hadron configuration.

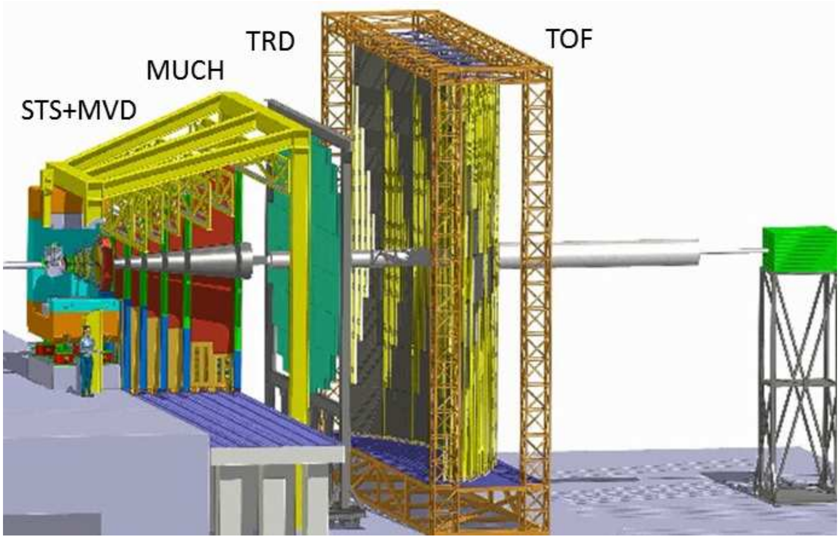


Figure 3.3: The CBM detector in muon configuration.

Electrons (momenta below 8–10 GeV/c) identification will be provided by Ring Imaging Cherenkov detector (RICH) in combination with transition radiation detectors (TRD). Muons features will be measured by an active hadron absorber system and muon tracking chambers (MuCh). For muon measurements, the MuCh will be moved to the position of the RICH.

Charged hadron identification will be performed by a time-of-flight (TOF) measurement with a wall of resistive plate chambers (RPC) located at a distance of 10 m behind the target. Information about photons and neutral particles will be provided by Electromagnetic Calorimeter (ECAL). Additional component of the setup is Projectile Spectator Detector (PSD) needed for the determination of the collision centrality and the orientation of the reaction plane. CBM experiment data acquisition is aimed at online event selection. This requires free streaming read-out electronics and fast algorithms running on computer farms based on future many-core architectures [57]. Performed simulations [58] show that measurement of the observables for different particle species requires detector to include different subsystems. For instance, for identification of pions, kaons and protons experimental setup will include the STS, RICH, TRD, TOF and PSD. For electrons and open charm mesons, the information comes from the MVD, STS, RICH, TRD, TOF, and PSD detectors.

The technical characteristics of the CBM detector setup have been formulated by performing simulation studies where detector resolution and granularity are implemented in a generic way not yet taking into account the detailed structures and the supporting material using CbmRoot framework [59].

Chapter 4

The Silicon Tracking System

The CBM experiment will measure rare observables with complex decay topology. This requires fast tracking and system design with minimal material budget that would enable inter alia the measurement of open charm decays with high statistics.

Double-sided silicon microstrip detectors are well suited for the particle tracking due to high granularity and speed of operation. In this chapter, layout of the Silicon Tracking System are described based on the requirements with respect to granularity, speed, radiation hardness, etc (Sect. 4.1).

In this chapter, prototype module components are described. The operation principle of the silicon microstrip detectors and STS prototype sensors are discussed in Sects. 4.2 and 4.3. An alternative module design based on the single-sided microstrip detectors is considered as a fallback solution. Prototype developments of the front-end electronics and low-mass module components are presented in Sects. 4.4 and 4.5, respectively.

4.1 Task, radiation environment and system concept

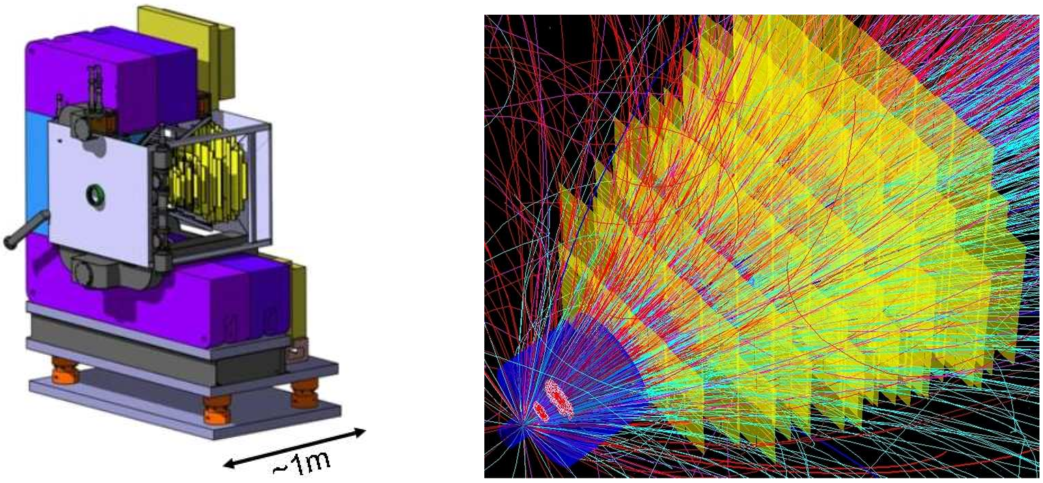
The physics goals of the experiment discussed in Chapt. 2 affect the technical design to the Silicon Tracking System that needs to accommodate conflicting requirements. Thus, the detector system has to be made of fast, radiation hard and thin silicon sensors.

The first part of the section includes the mission statement and radiation environment description. The use of self-triggering front-end electronics and radiation hard silicon sensors is motivated.

In the second part, the R&D strategy for the individual detector components is discussed as well as a concept of system mechanical integration. It will be shown that double-sided silicon microstrip detectors represent the best compromise between all the requirements. For the cases where the use of double-sided sensors is restricted (e.g., due to radiation hardness constraints), alternative solution based on single-sided detector modules is described.

4.1.1 Task

The Silicon Tracking System (STS) of the CBM experiment is being designed for charged-particle tracking in a magnetic field. Its task is to provide track reconstruction and standalone determination of the event multiplicity. The system will operate in the magnetic field in order to determine momentum of the particles from the track curvature. Calculations described in [60] show that magnetic field affects the the charge carrier transport, in particular leading to the increase of probability of charge sharing due to Lorentz shift [61]. The trajectories of the particles have to be identified with high efficiency, and their momenta have to be measured with high resolution ($\delta p/p \sim 1\%$). A prerequisite for this is hit reconstruction with efficiency $\varepsilon > 95\%$. The detector system has to be installed in the start-up phase of the CBM physics programme at SIS-100 with ion beam energies between 2 AGeV and 11 AGeV, and protons up to 29 GeV, and later at SIS-300 with ion beam energies up to 45 AGeV and protons up to 90 GeV. The readout of the STS has to be capable of following interaction rates up to 10 MHz without event pile-up. The typical track multiplicity reaches up to 600 per central gold-gold collision at 25 AGeV in the aperture of $2.5° < \theta < 25°$.



(a) (b)

Figure 4.1: (a) Schematic view of the STS system in the magnet. (b) Tracks from a central 25 AGeV gold-gold collision overlaid with geometry of the STS tracking stations in the GEANT simulation.

The STS extends about 1 m along the beam and will be installed in a $\sim 1\,\mathrm{m}^3$ volume in a 1 T dipole magnet to generate sufficient bending power for momentum measurement and suppress the low-energy δ-electrons. It will be built around a section of the vacuum beam pipe inside of the thermal enclosure, with an upstream window facing the vacuum vessel with the target and the Micro Vertex Detector (MVD), and a downstream window facing either the RICH or the MUCH detector systems. The tracking performance will allow extrapolating tracks into the

MVD to distinguish between primary and short-lived decay vertices (e.g., D-meson decays), and for standalone identification of decay topologies within the STS volume (e.g., K and Λ decays). Some physics observables (e.g., J/ψ decays) require the detection of high-momentum tracks with little curvature; others involve also low-momentum tracks, e.g., the leptonic decays of low-mass vector mesons which are strongly bent in the field. The horizontal extent of several upstream tracking stations is therefore enlarged with respect to the nominal aperture. A schematic illustration of the STS installed in the superconducting magnet is shown in Fig. 4.1a. A UrQMD-simulated central gold-gold collision at 25 GeV per nucleon and tracks transported in a GEANT [62] study of the STS are shown in Fig. 4.1b.

4.1.2 Radiation environment

The radiation environment of the tracking system has been calculated using the FLUKA [63] code and double-checked with UrQMD generated nuclear reactions transported through Virtual Monte Carlo (CbmRoot) simulation code for particle transport and interactions with matter. FLUKA covers an extended range of applications spanning from proton and electron accelerator shielding to target design, calorimetry, activation, dosimetry, detector design, Accelerator Driven Systems, cosmic rays, neutrino physics, radiotherapy etc. It is capable of calculating from the impinging beam and a geometrical description of the apparatus: ionization dose (Gy/year), non-ionizing energy loss (NIEL [64] expressed in 1-MeV equivalent neutrons cm^{-2}/year), high-energy hadron flux (cm^{-2}/s), and dose rate after irradiation (µSv/h) relevant for radiation protection of staff. Flux of high-energy hadrons includes both charged and neutral particles with energy above 20 MeV.

A simplified CBM geometry was realized in FLUKA, comprising the massive components in the cave and a number of detector stations of interest. Several two-dimensional grids of voxels (“scoring planes”) in the positions of detector systems were filled with the calculated fluences of different particles (charged hadrons, neutrons, electrons), expressed for 1-MeV neutron equivalent in silicon, and the ionizing dose in Gy. For the calculations, the FLUKA internal event generator has been used. A 35 AGeV Au beam on a Au target of 1% interaction length (corresponding to 250 µm thickness) was adjusted. The normalization of the data obtained is for one CBM run year equivalent to 2 months of beam time (5.1×10^6 seconds) at beam intensity 10^9 Au ions/s leading to 5×10^{15} beam particles that pass through target. Calculations involving the MVD detector system assume a reduced beam intensity of 10^7 Au ions/s.

The radiation damage of the silicon detectors has been studied by the ROSE collaboration [65, 66] and continued within the RD50 collaboration [67, 68]. The effects of non-ionizing (bulk) damage of the sensors are the increase of the leakage current, change of the effective doping concentration and increase of the charge carrier trapping. All of these effect are detrimental to the performance of the STS microstrip sensors. In particular, change of the effective doping concentration leads to the change of full depletion voltage. In case full depletion voltage is limited, e.g., by the sensor breakdown condition, the detectors may operate under-depleted. For double-side sensors, this would mean the loss of sensitivity on one side of the sensor. The increase of the leakage current leads to the increase of the shot noise contribution in the readout electronics and increase of the power dissipation in the system that may lead to the thermal runaway condition. Charge carrier trapping reduces the charge collection efficiency [69, 70] and hence the signal-to-noise ratio for the detector system.

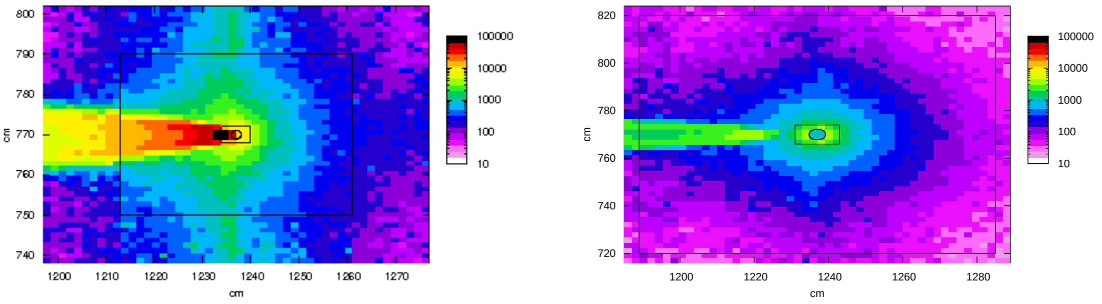
The ionizing damage alters the silicon sensor performance due to the formation of defects in the silicon oxide and its interface to the bulk silicon that trap positive charge. As a result, positive oxide charge induces negative charge at the interface between silicon and silicon oxide (electron accumulation layer). The electron accumulation layer alters the device properties, such as isolation between n^+-implants (i.e., n-side electrodes), interstrip capacitance, electric field distribution at the surface. The value of the interstrip resistance affects the sharing of the signal charge between neighboring electrodes. Parasitic capacitance between the strips is a dominant contribution to the noise in the detector system. The effect of radiation on the interstrip parameters and their measurement are described in Sect. 5.1. Electric field configuration at surface defines the breakdown voltage of the sensor [71]. Another effect of the surface oxide is generation of the surface current [72] that becomes prominent for large area devices.

ROSE and RD50 collaborations have achieved understanding of the role of the damage effects in the macroscopic detector behavior (defect engineering) [73] and developing radiation hard silicon detectors. Different detector materials have been studied for radiation hardness [74]. Among them, diffusion oxygenated float-zone (DOFZ) silicon has shown lower change of the depletion voltage with neutron fluence with respect to standard float-zone silicon [113]. Methods for obtaining the oxygenated silicon have been developed [76]. Operation and characterization of the heavily irradiated silicon sensors is described in [77–79].

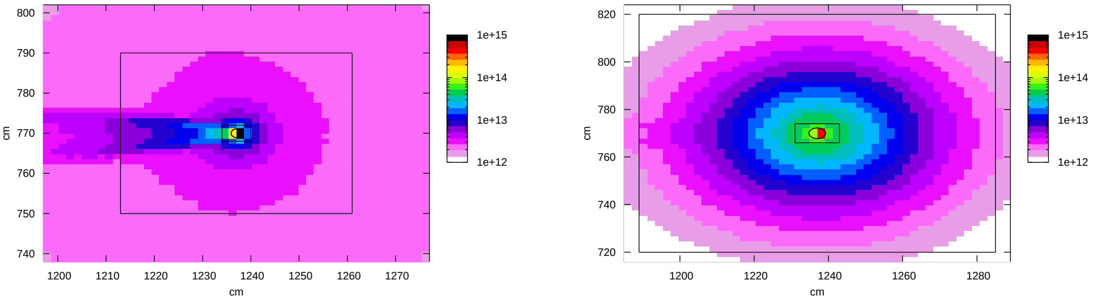
Conducted R&D studies are of great importance for the construction of the STS. The choice of sensor material as well as detailed scenario for defect annealing and reverse annealing [80] during the system operation at different temperatures will be based on the obtained results. A separate task to be fulfilled within the STS project is to achieve high voltage stability of the sensors. The sensor design has to optimized in order to reach high surface breakdown voltage, e.g., by optimizing the guard ring structure [81].

The radiation field in the STS volume causes cumulative damage and stochastic failures. Cumulative damage comes from energy deposition (ionizing dose) and lattice displacements (normalized to 1-MeV equivalent neutron fluence) in the detector material. Stochastic failures, also known as single event upsets (SEU), are changes of state in microelectronic devices due to charge deposition in a sensitive node or a logic element. The mechanism of charge deposition is often erroneously attributed to dE/dx ionization losses. With modern sub-micron transistor sizes, deposited charge would not be enough to cause a change of state in a transistor. In fact, single event upsets occur as a result of inelastic interaction between a high-energy particle and a nucleus in the electronic device. Such an interaction causes spallation of the target nucleus followed by localized emission of energy (O(MeV)).

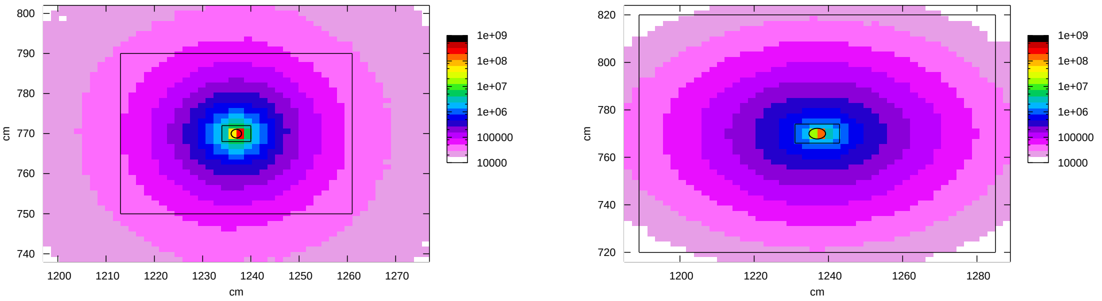
STS 1, z = 30 cm STS 8, z = 100 cm



ionizing dose



non-ionizing dose



flux of high-energy hadrons

Figure 4.2: Radiation profiles in the most upstream and downstream STS stations. For orientation, rectangular outlines of the stations are superimposed on the figures.

The radiation profiles are shown in Fig. 4.2. For ionizing dose and non-ionizing

Detector	**Normalization**	**Dose, Gy/year**	
		max. value	min. value
MVD	5×10^{13} beam particles	10^4	50
STS	5×10^{15} beam particles	8×10^4	50
MUCH 1	”	10^3	50

Detector	**Normalization**	**NIEL, n_{eq}/cm^2/year**	
		max. value	min. value
MVD	5×10^{13} beam particles	2×10^{13}	5×10^{10}
STS	5×10^{13} beam particles	2×10^{13}	5×10^{12}
MUCH 1	”	8×10^{13}	5×10^{12}

Detector	**Normalization**	**High-energy hadron flux, cm^{-2}/s**	
		max. value	min. value
MVD	10^7 beam particles/s	1×10^6	5×10^3
STS	10^9 beam particles/s	1×10^6	5×10^4
MUCH 1	”	8×10^5	5×10^4

Table 4.1: Minima and maxima of ionizing and non-ionizing dose as well as the flux of high-energy hadrons in the STS and its neighboring detector systems. Normalization denotes number of beam particles that pass through the target during one CBM run year or beam intensity for high-energy hadron flux. The beam intensity for MVD has been taken as 1% of the nominal beam intensity.

energy loss, otherwise monotone distributions decreasing towards station periphery, have additional components from δ-electrons. Their contribution can be seen in the middle left part of the histograms. The minimum and maximum values for NIEL fluence, ionizing dose and high-energy hadron flux are then summarized in Table 4.1 putting the radiation load on the STS system into context with the other detectors just up and downstream of the STS. Minimum and maximum values do not necessarily correspond to the inner and outer radii of the stations.

In the detector configuration with MUCH detector, the last STS station will be exposed to additional radiation load due to albedo neutrons reflected from massive absorbers in the MUCH detector. To mitigate this effect, neutron shielding has been considered. Recent FLUKA calculations with a 5 cm thick borated polyethylen layer in front of the MUCH detector system show that the neutron fluence at the last STS station is reduced by a factor of about 2.5. A 10 cm thick layer yields a reduction factor of about 3.5.

4.1.3 Layout of the detector system

The STS will consist of 8 planar tracking stations covering the aperture between the polar angles $2.5^\circ < \theta < 25^\circ$. Installed in the gap of the dipole magnet, they extend from about 30 cm to 1 m downstream of the target. The number of tracking stations is a tradeoff between precision of a track fit on one hand and spacial constraints as well as requirement of minimal material budget to reduce distortion of tracks by multiple Coulomb scattering. The arrangement of the tracking stations is schematically shown in Fig. 4.3.

The conceptional layout of a tracking station and nomenclature for its components are illustrated in Fig. 4.4. The building block of the STS is a module comprising an individual double-sided silicon microstrip sensor or a set of daisy-chained sensors, two multi-layer flat readout cables attached to one edge of either side of the detectors, and two front-end electronics boards. Sensors of three sizes will be used corresponding to the regions with different hit occupancy. The number of senor sizes is kept low in order to simplify production and maintenance. A set of daisy-chained sensors forms a sector. Daisy chaining of the sensors in low occupancy regions reduces the number of required readout channels. Due to spatial constraints, up to 5 front-end boards can be used for readout of one side of the half ladder. Modules of different type will be built, differing in their detector size, number of detectors used, and lengths of the readout cables. The front-end electronics is the same for all modules. A front-end board with 8 chips will read out 1024 channels.

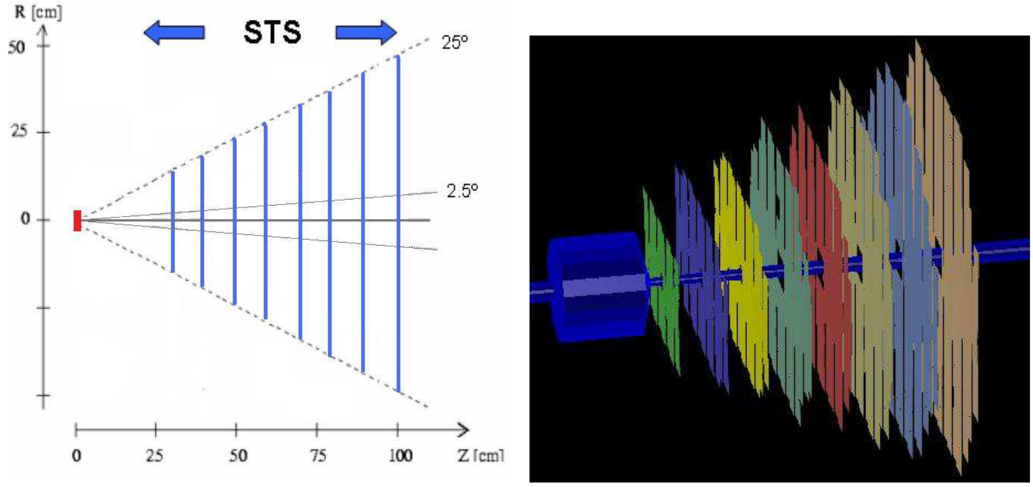


Figure 4.3: (Left) Concept of STS tracking stations covering the polar angles between 2.5° and 25° around the beam pipe. Positions along the beam axis and radii of the stations are indicated. (Right) Schematic view of the beam pipe with vacuum vessel and STS stations with realistic sensor arrangement, including gaps and overlaps. Stations are shown in different colours.

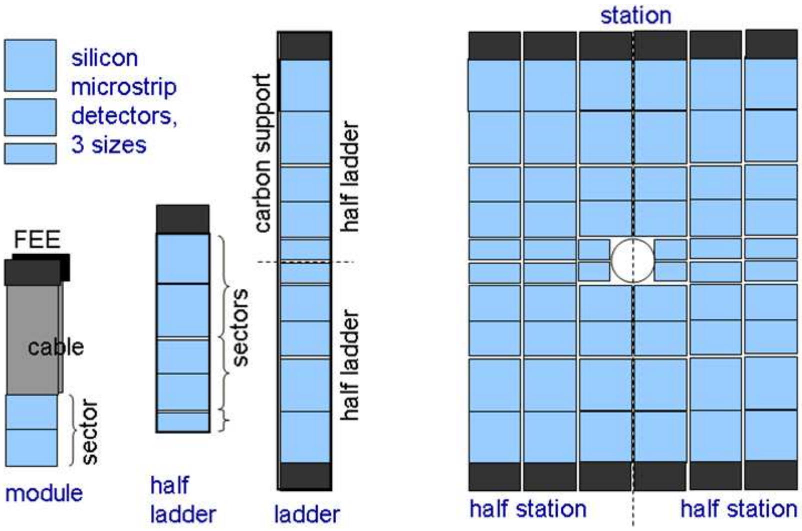


Figure 4.4: Conceptional layout of the tracking stations and their building blocks. Sensors of three different sizes are used (shown in blue). Front-end electronics at the periphery of the station is shown in black. Daisy-chained sensors form sectors that are connected to the readout electronics via microcables.

The modules will be arranged on carbon fibre ladders, allowing them to be mechanically and electrically integrated into the tracking stations. A ladder will be populated to form two half-ladders, with the readout directions oriented towards the top and bottom part of the STS. The ladders will be mounted on a super frame to form a tracking station. A station may be built from half-stations, each realized by a staggered downstream and upstream part, to cover gaps between neighboring ladders on a super frame.

Design of the STS tracking stations will be optimized for ultra-low material budget not exceeding $1\%X_0$ per tracking station, where X_0 is the radiation length of silicon[1]. Such material budget is needed to minimize multiple Coulomb scattering and achieve momentum resolution at the level of 1%. For this, module support structures will be made of low-Z material carbon fibre with large radiation length (25 cm) of the composite and low material budget (25 mg/cm^2 in the active area) [148]. Microcables with low mass design comprising polyimide films with aluminium traces have material budget of $< 0.17\%X_0$ (see Sect. 4.5). Material distribution for a tracking station at $Z = 60$ cm is shown in Fig. 4.5. Material budget is minimal in the center of the station and increases towards the periphery due to microcables. The outer edges of the ladders located outside of the acceptance are populated with readout electronics and cooling blocks. The remaining vertical space in the magnet aperture will be filled with data acquisition electronics (see Sect. 4.4.4).

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[1] Radiation length of silicon $X_0^{Si} = 21.82\,\mathrm{g/cm^2}$ or 9.36 cm. Silicon sensor thickness of 300 µm corresponds to about $0.3\%X_0$.

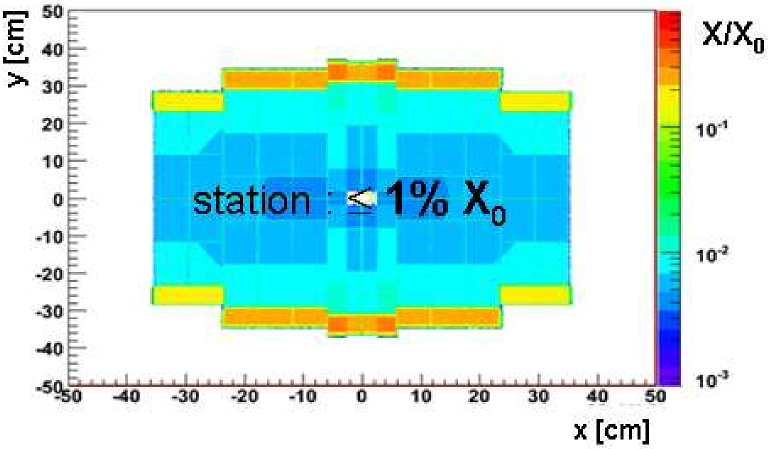


Figure 4.5: Material distribution in a tracking station expressed in the units of radiation length X_0.

In order to optimize the ladder production and facilitate maintenance of the system, STS stations will be composed of 8 ladder types only. This is depicted in Fig. 4.6. Ladders with different structure (i.e., length) are shown in different colours. A ladder of a given type is used in several stations. For example, modules used in the central part of the first station (shown in dark blue in the figure) are used at the same time in four subsequent stations. Some of the ladders will require a layout adapted to the hole around the vacuum beam pipe. Such a ladder will be missing an innermost sensor.

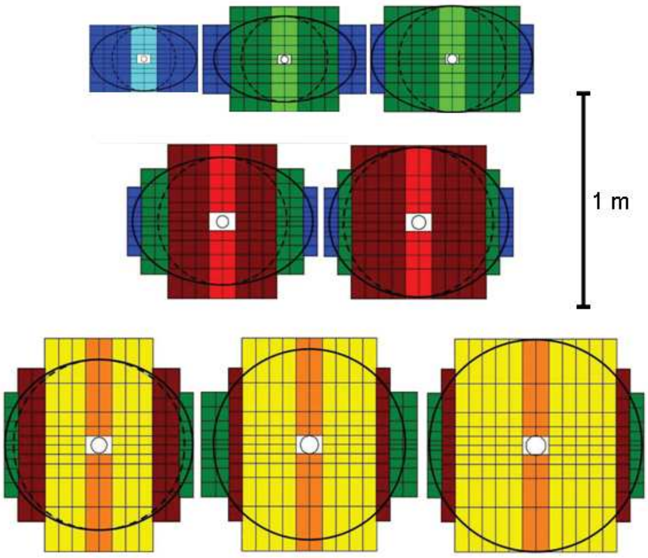


Figure 4.6: Layout of the STS stations optimized for minimal number of ladder types. A set of 8 stations is realized with 8 different ladder types (indicated by different colours). Several stations are horizontally enlarged in order to increase the acceptance for low-momentum particleas in the magnetic field.

Engineering models of carbon fibre ladder support structures and their arrangement into the detector system are shown in Fig. 4.7. A station sideview is shown with staggered orientation of the neighboring ladders. A closeup of the schematic front-end electronics block is shown with inclined front-end boards. The sketch of the whole system is shown with one tracking station for illustration. The system design is being elaborated, including the placement of services, electronics for data aggregation and copper-to-optical conversion of signals as well as thermal enclosure. Inside of the enclosure, sensors will be cooled using circulation of dry nitrogen. For the front-end boards, liquid or bi-phase CO_2 cooling options are considered.

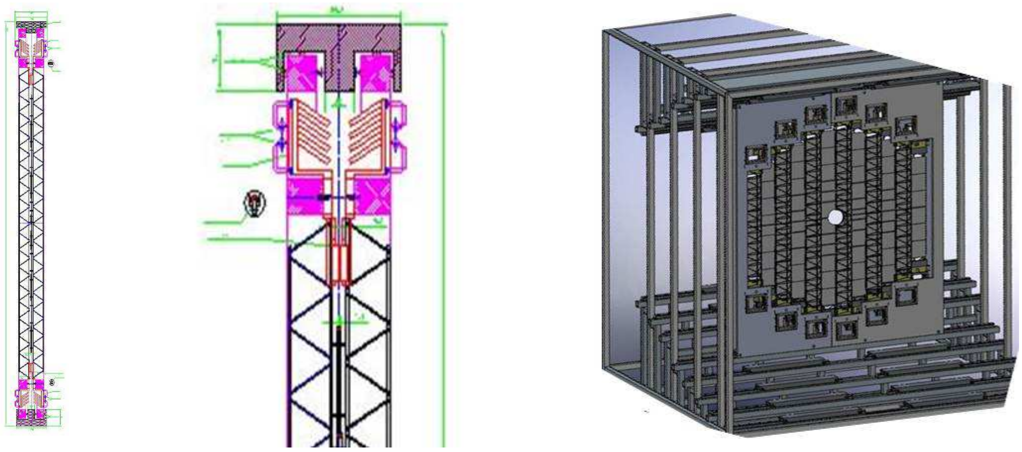


Figure 4.7: Engineering model of carbon fibre ladders and their arrangement into the detector system: (left) ladder with FEE blocks on the top and bottom ends, (middle) closeup of the FEE block of the station, (right) model of the STS with a tracking station.

4.1.4 Silicon microstrip detectors

The technical specifications of the microstrip sensors are based on the requirements of the STS with respect to tracking performance, radiation hardness, rate capability and stability of operation.

For the accurate track reconstruction with momentum resolution of about 1%, high position resolution and low-mass design of the system are required. A readout strip pitch of about 60 µm provides position resolution of about 25 µm that is dominated by the multiple scattering. Therefore, material budget of the system has to be as low as possible, keeping the readout electronics outside of the acceptance. System with material budget of the sensors $0.3\% X_0$ and realistic implementation of the detector module with material budget not exceeding $1\% X_0$ has been assessed in the simulations and yielded momentum resolution of about 1.5%.

Reliable long-term operation of the system requires hit reconstruction efficiency well above 95%. In order to meet this condition, signal-to-noise ratio of the detector system has to exceed 10 consistently during the detector lifetime, as the signal degrades due to radiation damage [83].

Relativistic heavy ion collisions with multiplicity up to 600 charged particle tracks at interaction rates of up to 10 MHz cause hit rates up to 30 MHz/cm^2 in the innermost part of the STS. At the periphery of the stations, hit rates decrease by two orders of magnitude. Silicon sensors of different lengths and daisy chaining of the sensors are used to accommodate the detector granularity to the highly non-uniform distribution of the hit rates.

In order to reduce the probability of event pile-up, fast self-triggering front-end electronics with shaping time of about 20 ns is required.

The innermost regions of the STS will accumulate during the experiment lifetime a neutron fluence of $4 \times 10^{14}\,\mathrm{cm}^{-2}$. For this, sensors with radiation tolerant design have to be used. In order to retain high charge collection efficiency, sensors have to be biased up to 500 V. The operation temperature has to be $-7\,^{\circ}\mathrm{C}$ or lower in order to suppress the radiation damage to the the sensors and reduce the leakage current.

The requirement of high spacial resolution at the level of 10 µm can be fulfilled either by pixel or by strip detectors. The pixel sensors have the advantage of true 2D space point measurement that comes at the expense of high number of readout channels. The microstrip detectors require less channels but have the ambiguity in signal assignment due to the projective topology (fake hits) at high multiplicities. This problem is handled in the track finding algorithm. The use of the microstrip sensors is preferred for the STS due to relatively large total area of the tracking stations (about 4.2 m^2).

The silicon tracker ladders can, in principle, be populated with either double-sided or single-sided silicon micro-strip detectors. Double-sided microstrip detectors would have the advantage of the (projective) space-point determination using two times less sensitive material for this task. On the the other hand, single-sided sensors are preferable taking into account the performance during the lifetime of the detectors in the radiation field. The space point determination in double-sided detectors requires that the full detector thickness is depleted of free charge carriers so that the strip implants on both detector sides are able to collect the transient charges created by the passage of the particles emitted as an effect of the nuclear collision on the target. An under-depletion of the detector will leave one detector side unable to collect the charge and thus a 2-dimensional space point cannot be reconstructed. If n-type silicon is considered, the material undergoes type-inversion after about 10^{13} equivalent neutrons per cm^2 depending on the material resistivity. The reverse bias voltage required for full depletion increases continuously after type inversion and reaches finally practical limits dictated by power dissipation due to leakage current or by the the high-voltage breakdown. The operation of the irradiated double-sided silicon microstrip detectors biased up to 500 V has been demonstrated in [84], however due to more complicated layering and sequence of fabrication processes their operation voltage is normally limited to several hundred volts.

Single-sided detectors can typically stand higher operation voltages, which is partly due to their relatively simple manufacturing steps and a predictable stable behavior of the electrical fields. In addition, they do not need to be reverse biased to the extent that the full detector thickness depleted. The width w of the depletion layer in a pn-junction biased to voltage V_{bias} is given by

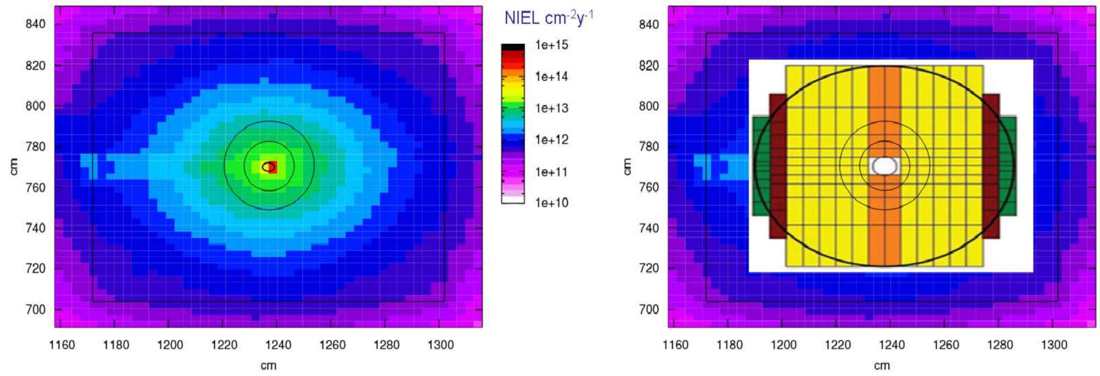
$$w = \sqrt{2\varepsilon\rho\mu V_{bias}}, \tag{4.1}$$

where ε and ρ are permittivity and resistivity of the sensor material, respectively. The built-in voltage that is much less than typical bias voltages is neglected.

For the single-sided sensors, it is sufficient to have the electrical field at the segmented side. Provided that the depletion layer is still thick enough, a charge pulse can be detected on the this side. Since a pair of detectors is used mounted back-to-back the space-points can be still reconstructed despite the harsher conditions at which full sensor depletion cannot be achieved. The material budget doubles in this case, unless the use of thinner sensors is considered.

The operation voltage as a function of the NIEL equivalent neutron fluence in the detector system can serve as one criterion to discriminate between possible use cases of different detector technologies in the STS tracking stations along with other criteria described at the beginning of Sect. 4.1.4.

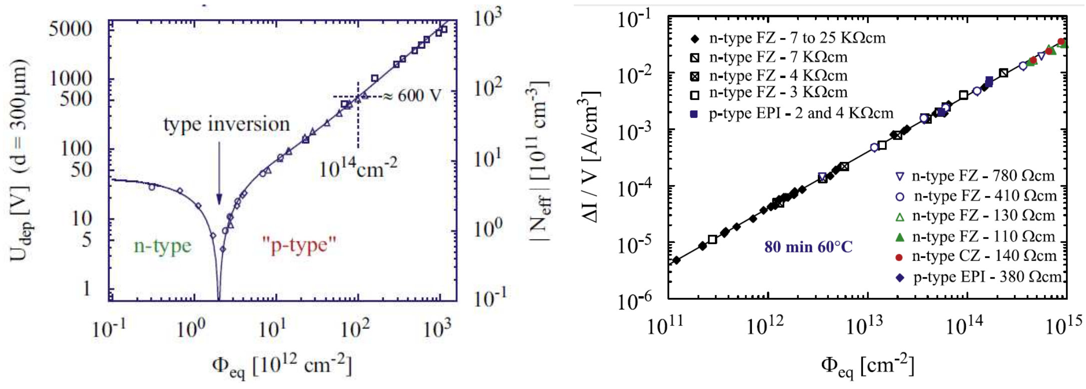
Fluence distribution in the most downstream STS station for one standard CBM year, obtained with the FLUKA code is shown in Fig. 4.8a. Sensors in the peripheral part of the station accumulate fluence less than $10^{13}\,\mathrm{n/cm^2}$ and have depletion voltage less than 100 V. Sensors located close to the beam pipe, will see higher fluences and may require single-sided technology. For illustration, regions with different fluences are projected onto the station in Fig. 4.8b.



(a) (b)

Figure 4.8: (a) Radiation pattern in the most downstream STS station with the muon detector system present. (b) Several fluence limits are projected onto the tracking station to establish different radiation regions. Solid box indicates the magnet opening. The circles mark the regions with different fluence ranges: beam pipe (inner circle); region with $\Phi > 10^{13}\,\mathrm{n/cm^2}$; region with fluences about $10^{13}\,\mathrm{n/cm^2}$; fluence not leading to type inversion.

Data available from the performance studies of various types of silicon and growth processes in radiation fields (see Fig. 4.9) yield the required depletion voltages and leakage current per unit volume in the devices. Up to fluences of $\sim 1 \times 10^{13}\,\mathrm{n_{eq}/cm^2}$ the depletion can be achieved with 100 V, considering the silicon resistivity of about 3–4 kΩ cm. In the STS stations this technology will be able to cover at least 70% of the total area, i.e., all the outer part beyond the radius of about 16 cm. The region close to the beam line will see higher fluences, in particular if several years of operation are considered as the time-of-life criterion for the silicon detectors. For the inner part of the STS, single-sided silicon detectors should be explored. They can be of either *n* or *p*-type bulk material [85] and, with about 300 µm individual thickness, resulting in two times the material budget comparing to their double-sided counterpart.

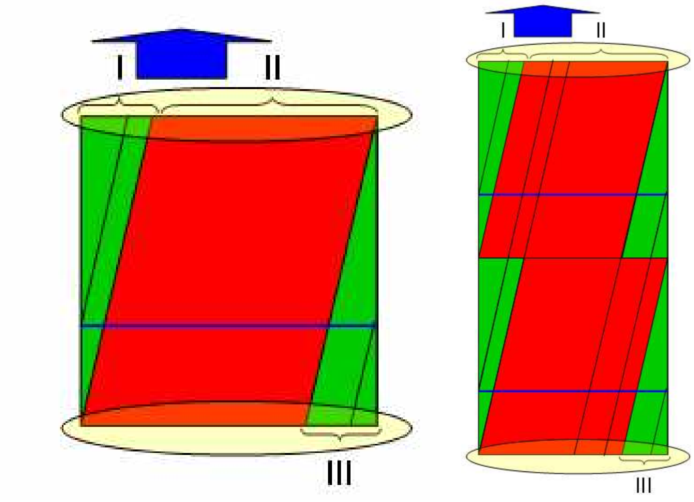


(a) (b)

Figure 4.9: (a) Depletion voltage and (b) current per unit volume in silicon detectors exposed to neutron irradiation (courtesy of F. Hartmann).

The detector topology proposed the STS ladders foresees a strip orientation of 7.5° with respect to the vertical detector edge, and a fully vertical orientation on the back-side of the sensor (alternatively also the negative angle as compared with the front side). The detector geometry is described in details in Sect. 4.3. The stereo angle is a trade-off between the number of combinatorial space points and the space point measurement error in the horizontal plane. It has to be kept reasonably low since the horizontal resolution strongly affects the momentum measurement in the bending plane of the dipole magnet. The problem of the stereo angle has been solved in LHCb Silicon Tracker by tilting the individual detector ladders with single-sided sensors under a certain angle within the station [86]. This approach is not applicable for the STS due to spacial constraints in the magnet aperture. In order to be compatible with a sector construction out of several daisy-chained sensors, including the above mentioned stereo angle, a double metallization is connecting the AC coupled readout strips of a corner region to their partner strips in the opposite corner of the detector. Daisy chaining of the sensors allows to reduce the granularity at the periphery of the stations, where hit rate is low, and thus reduce the amount of readout channels. It is also necessary because of the spacial constraints: the amount of detector modules that are readout by a front-end hybrid is limited to five per half-ladder. The use of double metal interconnects and daisy chaining of the sensors are schematically illustrated in Fig. 4.10. The advantage of the double metallization is the readout of a given full sensor side from one edge only, thus achieving minimal material budget. The downside of this approach is, however, the increased complexity of the sensor fabrication, increased capacitance contribution form additional metal layer and longer signal propagation path. Without double metallization, the readout of a sensor implies the use of two microcables to access the strips from both top and bottom edges of the sensor. This option leads to the increased material budget and complexity of a detector module. Another option would be not to read out the short corner strips that correspond to region III in Fig. 4.10a.

The total number of readout channels in the STS is about 2.1 million, that poses challenge for placement of the readout electronics within the magnet aperture and its cooling. Figure 4.11 depicts the first prototype detector that was realized in cooperation of GSI and CiS, Erfurt. The parameters for current detector developments are summarized in Table 4.2.



(a) (b)

Figure 4.10: (a) Schematic double-sided microstrip detector shown with the strips under a stereo angle of 7.5° on the front (p) side. Three different strip regions are shown: Corner regions (I) and (III), and central region (II). In order to realize a readout in the vertical direction (blue arrow), a connectivity problem in the corner region (III) of the stereo side shall be avoided by interconnecting the AC layers of pairs of the readout strips through horizontal metal lines. (b) The situation is shown for two daisy-chained detectors.

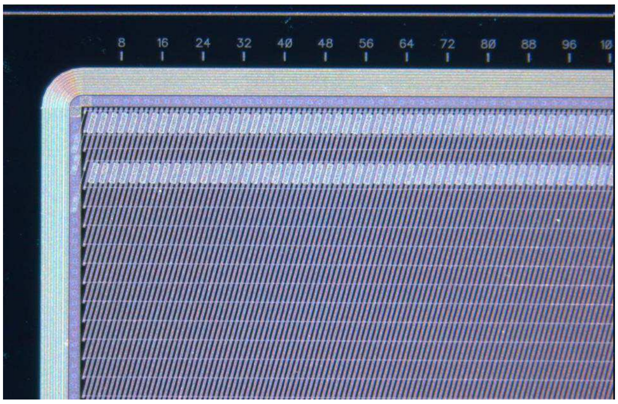
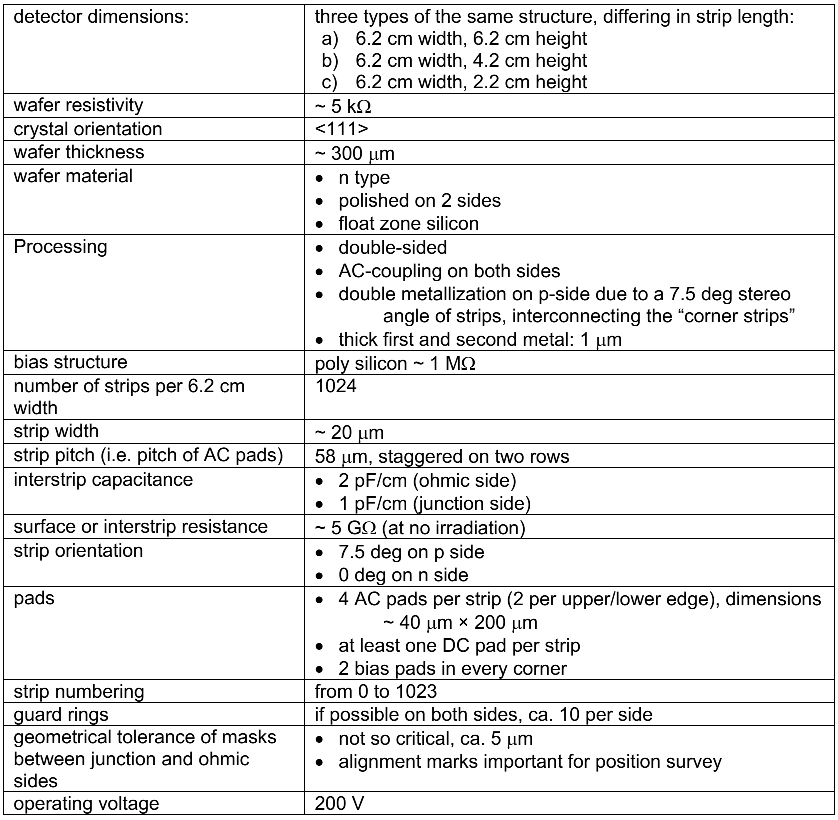


Figure 4.11: Prototype sensor CBM01 realized in cooperation of GSI and CiS, Erfurt, Germany. The double-sided sensor features a design with a strip pitch of 50.7 µm, AC coupled readout strips (seen as slanted lines in the photo) and a metal interconnects between pairs of corner strips (horizontal lines).



detector dimensions:	three types of the same structure, differing in strip length: a) 6.2 cm width, 6.2 cm height b) 6.2 cm width, 4.2 cm height c) 6.2 cm width, 2.2 cm height
wafer resistivity	~ 5 kΩ
crystal orientation	<111>
wafer thickness	~ 300 µm
wafer material	• n type • polished on 2 sides • float zone silicon
Processing	• double-sided • AC-coupling on both sides • double metallization on p-side due to a 7.5 deg stereo angle of strips, interconnecting the “corner strips” • thick first and second metal: 1 µm
bias structure	poly silicon ~ 1 MΩ
number of strips per 6.2 cm width	1024
strip width	~ 20 µm
strip pitch (i.e. pitch of AC pads)	58 µm, staggered on two rows
interstrip capacitance	• 2 pF/cm (ohmic side) • 1 pF/cm (junction side)
surface or interstrip resistance	~ 5 GΩ (at no irradiation)
strip orientation	• 7.5 deg on p side • 0 deg on n side
pads	• 4 AC pads per strip (2 per upper/lower edge), dimensions ~ 40 µm × 200 µm • at least one DC pad per strip • 2 bias pads in every corner
strip numbering	from 0 to 1023
guard rings	if possible on both sides, ca. 10 per side
geometrical tolerance of masks between junction and ohmic sides	• not so critical, ca. 5 µm • alignment marks important for position survey
operating voltage	200 V

Table 4.2: Parameters of double-sided silicon microstrip detectors currently under preparation for production.

4.1.5 Mechanical integration of a detector module

The integration of the silicon microstrip detectors into the basic operational unit, the module, is being explored. Module design is driven by the requirement of minimal material budget of the STS. For this, modules will be mounted on a rigid low-mass support structure (ladder). Sensors along the ladder, are grouped into sectors by daisy chaining. A sector side (p or n) is read out from one edge only in order to minimize the number of microcables. Concept of a detector module is sketched in Fig. 4.12. In the figure, double-sided sensor is read out via long microcables. Interconnect technology chosen for module integration is TAB bonding[2]. Thus, on one end microcable is TAB-bonded to a microstrip sensor and on the other – to a front-end hybrid. The problem of high-density interconnect layout of the front-end board, where signals form 1024 channels are routed to 8 analogue microchips, is addressed in [87].

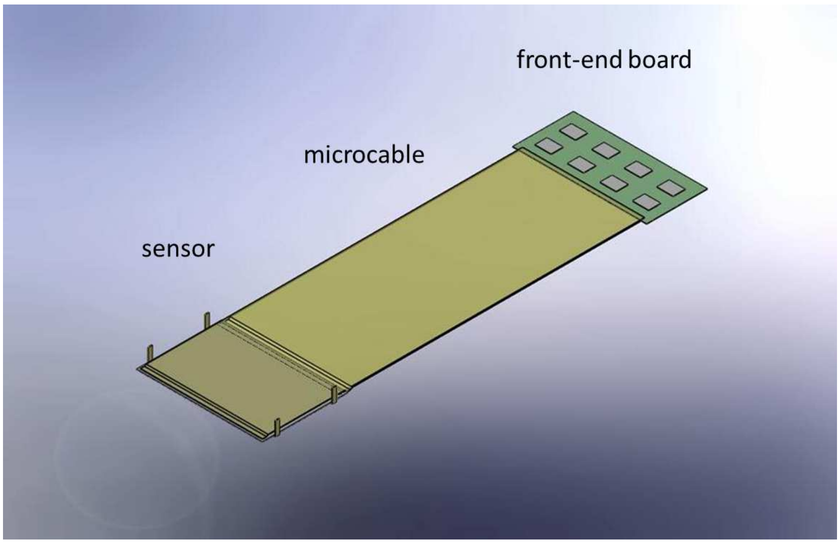


Figure 4.12: Schematic view of the detector module (without support structure). Silicon microstrip sensor with 1024 channels is read out by a front-end hybrid with bump-bonded low power chips via stacked microcable optimized for low-noise and low-crosstalk operation.

The first prototype components of a detector module have been realized in order to test crucial design aspects, e.g., TAB bonding technology and feasibility of manufacturing microcables with length up to 60 cm (see Sect. 4.5).

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[2] TAB – tape-automated bonding

4.2 Microstrip detector basics and operation principle

Semiconductor detectors have been extensively applied to ionizing radiation detection since the middle of the 20th century due to their superior spectroscopic properties. Adaption of the planar process to the fabrication of silicon detectors opened a way to creation of position-sensitive devices that made use of the fine segmentation of detector channels. After the invention of silicon microstrip detectors their development has been boosted by application in particle physics that required position measurement with approximately 10 µm precision and operation at high rates needed for measurement of rare particles. Due to relatively long lifetimes (10^{-13} to 10^{-12} seconds), these rare signals form a specific tracking topology with decay vertex detached from the point of primary interaction with target.

One of the first applications of silicon microstrip detectors in high-energy physics experiments dates back to the early 80s. In NA11 experiment, strip detectors have been applied to flavor tagging, namely vertex reconstruction of particles containing c-quark. Close integration with miniature electronics allowed for the construction of large-scale detector systems with barrel-type geometry. At LEP and Tevatron, strip detectors have been employed for particle decay vertex reconstruction along with gas detectors that provided tracking. Examples include DELPHI MVD [88] and CDF [89]. At high-luminosity environment of the LHC experiments (ATLAS [90], CMS [91]), vertexing has become a task for pixel sensors due to their high granularity and 2D hit information, avoiding ambiguity of projective topology inherent to the strip detectors. The strip detectors, in turn, have been used to build large area silicon detectors used for tracking. Evolution of the silicon detectors in high energy physics is summarized in [92].

Silicon trackers placed in the magnetic field provide the most accurate measurement of particle momentum. Over the years, they have been extensively applied in high-energy physics experiments with a trend towards higher detector areas with CMS topping out at around 200 m^2 of silicon. Comparing to that, CBM Silicon Tracking System will have microstrip detector area of around 4.2 m^2 constrained by the aperture of the dipole magnet but instead excel in channel density.

In order to make a solid-state device operational during a long period of time with its signal being fast and proportional to the energy deposited by the particles, its detecting material has to fulfill the following requirements:

- low energy required to create an electron-hole pair
- absence of charge recombination and trapping
- high carrier mobility with close values for electrons and holes
- high electrical resistivity

Detector material that has all the necessary properties doesn't exist. However, silicon offers the best compromise to the listed requirements. Comparing to the other detector materials (Ge, GaAs, diamond), it has low energy needed to generate an electron-hole pair ($E_{\text{e-h}} = 3.6\,\text{eV}$). Table summarizing the properties of different detector materials can be found in [93]. Specific energy loss of a minimum ionizing particle in silicon is

$$\left(\frac{dE}{dx}\right)^{Si}_{MPV} = 0.29\,\text{keV/µm} \tag{4.2}$$

that equals approximately 80 electron-hole pairs. Thermal current generation is essentially suppressed at room temperature due to large band gap ($kT = 26\,\text{meV} < E_{gap} = 1.12\,\text{eV}$). Thus, little or no cooling is required during the operation. Due to the fact that silicon is an indirect semiconductor, transition of the electrons from the conduction band to the valence band requires additionally momentum transfer to the crystal lattice such that direct recombination of the charge carriers is suppressed. This property results in relatively long charge carrier lifetimes ($\sim 1\,\text{ms}$ for preirradiated silicon).

In order to to detect particles reliably, fluctuation of charge carrier number has to be much less than this number itself (e.g., $\Delta N/N = 10^{-3}$). As elaborated in [94], this condition requires material with resistivity beyond practical limits ($\sim 10^{10}\,\Omega\,\text{cm}$). In order to make silicon a suitable detector material, one has to exclude free carrier exchange between the electrodes and semiconductor by increasing its resistivity.

Decrease of carrier injection form the electrodes is reached by creating barrier contacts based on junction properties of semiconductors with different types of conductivity (pn-junction). At the interface between p and n-doped regions, potential gradient emerges (built-in voltage V_{bi}) and space charge region is created. By applying external voltage to the electrodes, space charge region is extended. Since free charge carriers are almost completely removed from the space charge region, its resistivity is much higher than that of material outside of the junction. Thus, pn-junction plays a major role in applying silicon to charged particle detection. Junctions patterned in form a long strips provide positional sensitivity.

A charged particle passing through the sensitive volume generates pairs of mobile charge carries of the opposite sign (electrons and holes). External voltage applied to the electrodes creates electric field in the crystal which causes the charge carriers to drift towards the electrodes. As the charge carriers move, they induce a mirror charge in the electrodes. Current pulse induced by moving charges at the electrodes is used to detect a particle. A simplified detector scheme is shown in Fig. 4.13. On the scheme, the pn-junctions are shown as diodes. Charge sensitive amplifiers (CSA) read the signals out via coupling capacitors C_{coupl} form the diode terminals that correspond to p^+ or n^+-strips. Biasing resistors that connect every strip to a corresponding bias rail on the n or p-side are shown as $R_{biasN,P}$. The bias rails of a sensor are connected to a high voltage source via limiting $1\,\text{M}\Omega$ resistors.

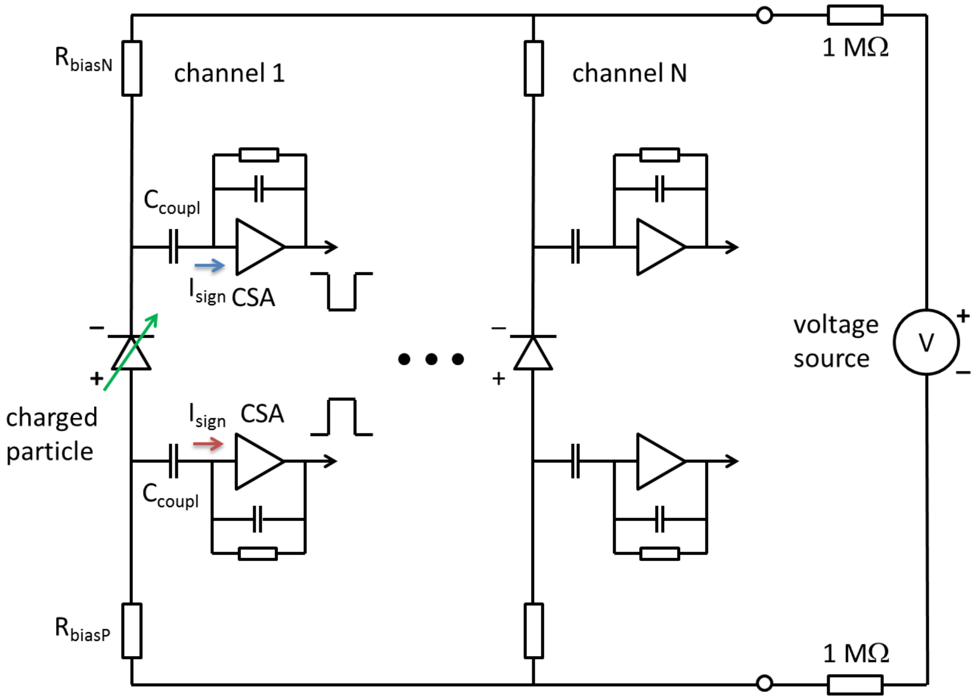

Figure 4.13: Operation principle of a double-sided silicon microstrip detector.

Typical structure of a microstrip sensor is shown in Fig. 4.14. Every strip consists of an implant with a metal strip on top separated by a coupling dielectric. The dielectric prevents the detector leakage current from flowing into the readout electronics, thus implementing the AC coupling. A stack of several dielectric materials (SiO_2 and Si_3N_4) is sometimes used to provide better high voltage stability of the coupling capacitors. AC and DC contact pads are integrated on the strip for readout and probing (e.g., during the quality assurance). Every strip is connected to the bias ring with external voltage applied to it. For a long-term stability of operation, proper edge termination of sensor has to be provided. Due to the mechanical damage caused by the cutting procedure, the sensor edge becomes highly conductive due to introduced lattice damage. Thus, electric field should not reach the sensor edge in order to avoid generation of additional leakage current and edge breakdown. For this purpose, a guard ring or often a set of floating guard rings is introduced in order to gradually reduce the potential in the region between the strips and the sensor edge. The sensor surface is passivated with a SiO_2 layer with openings for contact pads in order to protect it from the contamination.

On the n-side of the sensor, additional design effort has to be made to isolate the n-strips that are otherwise shorted by the electron accumulation layer. Special mitigation techniques to break the electron accumulation layer are described in Sect. 4.3.1 (part “Wafer type CBM02”).

Silicon sensors with double metal layer offer an advantage of routing the signals not along the implanted strips. Thus, sensor designs optimized for a particular detector module structure become possible. The isolation between the two metal layers is done using SiO_2 or polyimide (Kapton) layer. The disadvantage of the double metal layer is the increased complexity of sensor production and crosstalk between readout and routing lines. In the STS silicon microstrip sensors, double metal layer is used to connect the short corner strips that appear due to stereo angle (see Sect. 4.1.4). In this case, due to less number of microcables, module design with a minimal material budget is achieved.

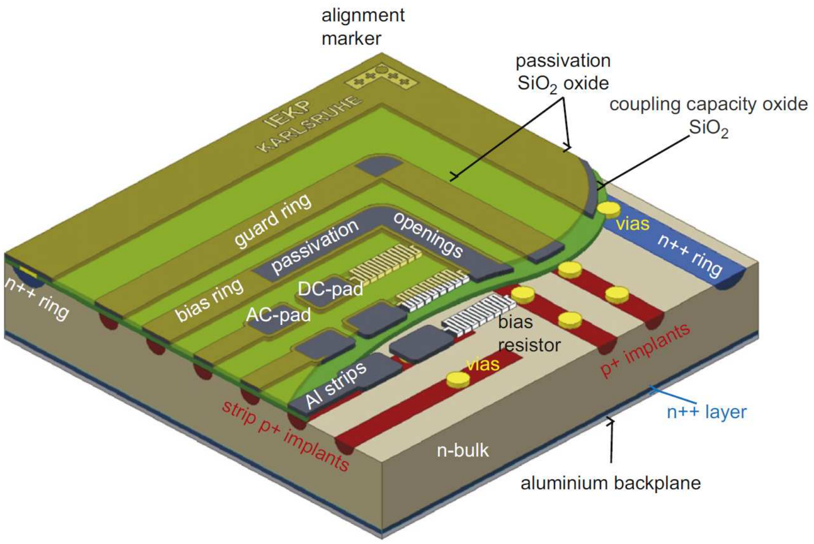

Figure 4.14: Structure of a silicon microstrip detector (courtesy of F. Hartmann).

Types of silicon detectors

Silicon detectors differ in their applications mainly due to the segmentation of the electrodes (see Fig. 4.15). Devices with largely asymmetric electrodes (few tens of µm wide and several cm long) are called strip detectors. Fine segmentation of the electrodes provides precision of the position measurement as good as 5–10 µm. Strip sensors have large active area with strip length up to 10 cm [95]. Microstrip sensors with double-sided structure can provide 2D position information using the same amount of material as the single-sided ones. Often, the coupling capacitance and the bias resistor are implemented on every strip of a sensor, thus providing the AC-coupled readout.

Devices with approximately equal dimensions of electrodes are called pad or pixel detectors. Pad detectors with coarse or no segmentation are used for low-multiplicity particle tracking or event sampling (e.g., in calorimeters). The electrode dimension of the pixel sensors range from several hundreds to several tens of micrometers. Such sensors provide true two-dimensional position measurement without fake hits that are inherent to the projective topology. Due to the high channel density, pixel detectors are applied in the high track density environments, e.g, at positions closest to the interaction point of an experiment.

In silicon drift detectors (SDD), a sideward depletion of the bulk is achieved in combination with an electric field parallel to the wafer surface. Thus, signal electrons drift in a potential valley towards the anode. The silicon drift detectors can be used to obtain position and energy information from the drift time and amplitude of the signal. In case of a segmented n^+-strip anode, two-dimensional position information is obtained. Due to the low capacitance of the collecting electrode (10–100 fF) and hence low noise, SDDs with radial geometry are applied for the X-ray spectroscopy. A silicon drift detector has been applied for particle tracking in the ALICE experiment as a part of Inner Tracking System [96].

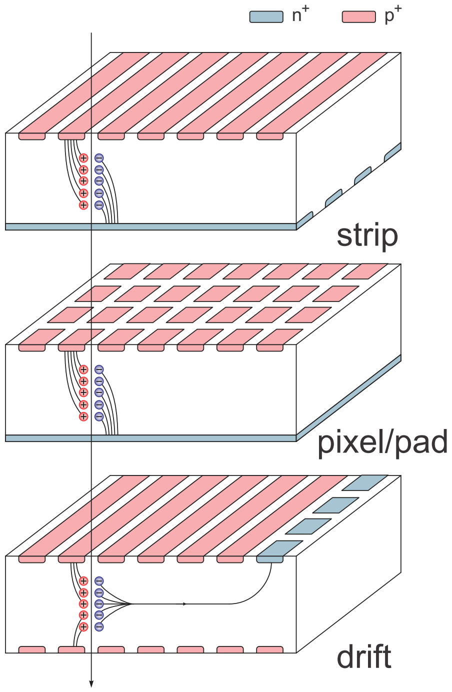

Figure 4.15: Types of silicon detectors.

Requirements to the physics performance of the STS favour the use of double-sided silicon detectors for tracking purposes due the best compromise between material budget, channel density and speed of operation. Fabrication of the double-sided silicon microstrip sensors for the STS is a complex task due to their double-sided layout, large area (up to $62 \times 62\,\mathrm{mm}^2$) and the use of the double metal layer on both sides. For the production, 19 photolithographic masks will be required. The design ensures full geometric efficiency of the sensor (no “dead” corners) and compatibility with detector module structure that has minimal material budget.

4.3 Development of CBM silicon microstrip sensors

The CBM experiment will operate at high interaction rates in a radiation environment of up to 4×10^{14} 1-MeV $\mathrm{n_{eq}cm^{-2}}$ in 6 years of operation. Defects introduced into the silicon lattice due to irradiation lead to a formation of charge traps and increase of leakage current. This causes a degradation of charge collection efficiency on one hand and increase of noise on the other. Therefore, radiation tolerant design of the double-sided microstrip sensors for the STS is required to achieve sufficient signal-to-noise ratio $S/N > 10$ for $> 95\%$ of hits and a robust detector breakdown performance as the particle fluence increases during the detector operation.

Wafer type	Description
CBM01	First full-size prototype sensor compatible with the construction of a low-mass module featuring 15° stereo angle and double metal interconnects of the short corner strips at *p*-side
CBM02-SPID	Technology wafer to explore radiation tolerant design elements, i.e., *n*-side strip isolation structures, guard rings, bulk doping concentration etc
CBM03	Wafer design with full-size sensor with ±7.5° stereo angle at both sensor sides. Double metallization is likewise used for interconnecting of the short corner strips. Detector is optimized for the module design where analogue signals are read out via microcables from two detector edges only.
CBM03′	Intermediate single-sided wafer based on CBM03 *p*-side design to investigate the high-voltage stability issues with AC coupling capacitors (described in). Introduced improvements include combinations of thicker dielectric layers (oxide-nitride or oxide-nitride-oxide) and polysilicon buffer layer.
CBM04-FSD	Second technology wafer dedicated to exploring radiation tolerant design features with emphasis on the *n*-side strip isolation. Novel isolation technique based on Schottky barrier effect is introduced. Main emphasis during the characterization is put to verifying the efficiency of strip isolation and its radiation-damage susceptibility.
CBM05	Resubmission of the CBM03 wafer with similar geometrical design but deep modifications towards high voltage stability, noise reduction and ease of use. Production has been started in parallel at CiS and Hamamatsu.

Table 4.3: Wafer generations of microstrip sensors for the Silicon Tracking System.

Stringent requirements to the material budget of the detector require placement of the front-end electronics at the periphery of the tracking stations. In this case, the signals from the detector are read out via long analogue microcables whose length reaches up to 60 cm. Capacitance of a microcable along with detector capacitance[3] thus becomes a dominant noise source in the preamplifier of the front-end chip and reduces the signal-to-noise ratio. In order to preserve sufficiently high signal-to-noise ratio one may increase the amount of a signal charge by employing thicker sensors. Successfully applied in the LHCb Silicon Tracker [97], this approach is limited in case of STS due to dramatic influence of extra material in the detector acceptance on the momentum resolution of the reconstructed particles [98]. Therefore, sensor thickness is restricted to about 300 µm.

This section describes existing prototype wafers with microstrip sensors for the STS produced in cooperation with CiS Institute for Microsensor Systems and Photovoltaics (Erfurt, Germany). Four wafers designed and produced from 2007 till 2011 have included the design changes towards higher radiation hardness and geometrical parameters corresponding to the ladder structure of the detector module (see Table 4.3).

In the context of this work, double-sided microstrip detectors have been characterized in order to establish general electrical functionality, measure interstrip parameters, channel yield as well as some other technological parameters.

4.3.1 Double-sided radiation tolerant microstrip detectors

The major part of the STS will be populated with the detector modules based on double-sided silicon microstrip sensors. The sensors will be mounted on low-mass carbon fibre support structures and read out via long microcables by the front-end electronics placed outside of the detector acceptance. Structure of the sensors including double metallization on both sides to connect the short corner strips is in line with the low-mass design of the detector modules. The following section describes five subsequent generations of the wafer design, including underlying sensor technology and steps for the full-size prototypes towards the final design.

Wafer type CBM01

The first dedicated wafer layout CBM01 [99] manufactured by CiS, Erfurt contains a full-size prototype sensor compatible with the construction of a low-mass module of the STS, as well as further smaller test sensors (see Fig. 4.16). The double-sided design is needed to achieve minimum material budget within the detector aperture. They were produced on 4” wafers of 285 µm thickness made of n-type float-zone silicon with 3–4 kΩ cm resistivity. The full-size sensor (CBM01) is being used for detector module prototyping where the issues of mechanical integration, cooling infrastructure and long analogue readout cable are to be addressed. Sensors with smaller sizes (CBM01B1 and CBM01B2 types) are suitable

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[3] Detector capacitance “seen” in the readout channel comprises contributions from the backplane capacitance and capacitance to the neighboring channels.

for testing of radiation tolerance and the construction of test systems with prototype front-end electronics. The strips on all sensors on the wafer are biased via punch-through structures [100] and are read out in the AC mode through integrated coupling capacitors. In order to avoid shorting of the strips on the n-side, p-spray isolation has been used. Some of the geometrical sensor parameters are summarized in Table 4.4.

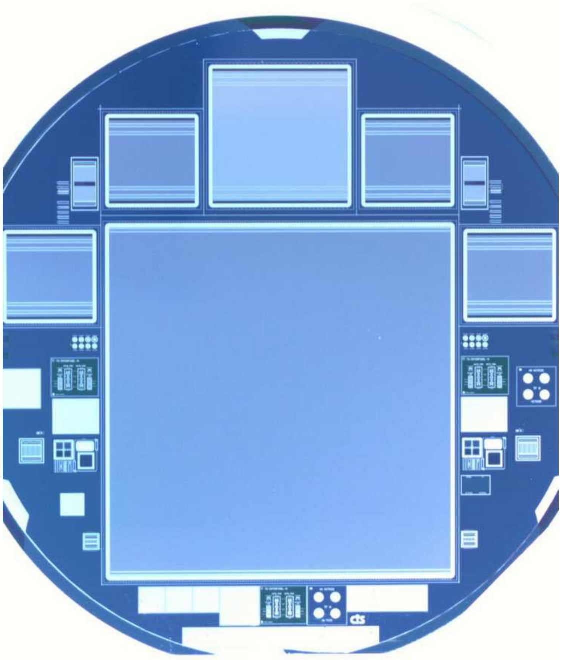

Figure 4.16: First prototype wafer with full-size sensor and smaller test sensors.

The CBM01 sensor addresses specific connectivity issues of the detector module with ladder structure where sensors need to be daisy chained. The prototype features a 15° stereo angle between the p and the n-side strips. On both sensor sides, 1024 contact pads are arranged near the top and bottom edges in a staggered manner. Their pitch of 50.7 µm matches the input of the n-XYTER chip that is used during the initial prototyping phase. On the stereo (p-implanted) side, unconnected corners are avoided by linking the metal of every short strip with its matching partner in the opposite corner through a line on the second metal layer.

Two other sensor types called CBM01B1 and CBM01B2 are nicknamed as big and small baby sensors, respectively. Both sensors have 256 orthogonally oriented strips at each side placed with a pitch of 50.7 µm and 80 µm. Additionally, extra rows of AC-pads for testing purposes and DC-pads for probing the strip implants have been added.

The close-ups of the sensor corners shown in Fig. 4.17 and Fig. 4.18 illustrate the arrangement of the strips and their biasing principle. The CBM01B2 type sensors have a row of DC-pads and a redundant row of AC pads that can be

Parameter	**CBM01**	**CBM01B1**	**CBM01B2**
Strips per side	1024	256	256
Pitch, μm	50.7	80	50.7
Width, μm	18	40	18
Stereo angle, $^\circ$	15	90	90
Chip size, mm^2	54.9×53.9	22.4×22.4	14.9×14.9
Pads per strip	2 AC pads	4 AC + 2 DC pads	4 AC + 1 DC pads

Table 4.4: Geometrical parameters of the CBM01 sensors.

contacted by the probes needles leaving the readout pads intact. The bias rail on the N-side is represented by a solid metal stripe without guard rings. Likewise, the CBM01 type sensor has guard ring structures on the *p*-side only (shown in the photograph). Due to the stereo angle, only one row of AC pads can fit the available area. The thin horizontal metal lines seen in the photo are made using the second metal layer to interconnect the short strips in the sensor corners to the matching strips in the opposite sensor edge. Both sensors have a punch-through type biasing. For this reason, the strip implants need to reach just up to the bias rail with a gap between the bias rail and strip implant equal to 7 µm.

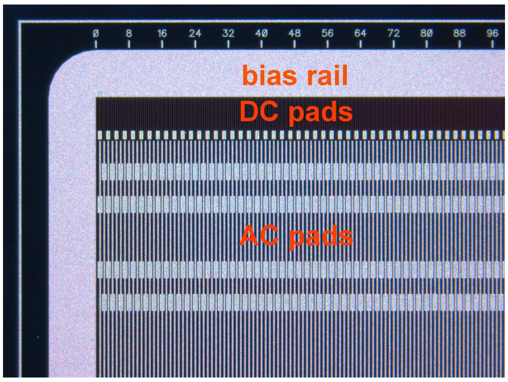

Figure 4.17: N-side of CBM01B2 type sensor with two rows of AC pads and one row of DC pads.

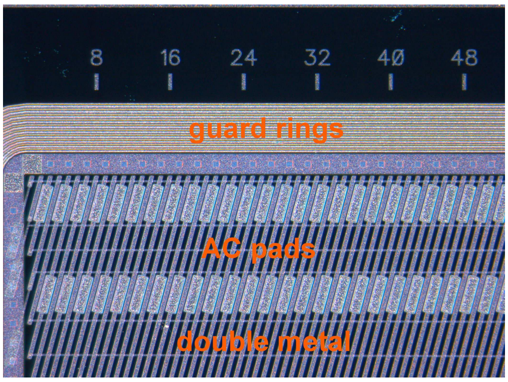

Figure 4.18: P-side of CBM01 full-size sensor with one row of AC pads and 10 guard rings.

Wafer type CBM02-SPID

Further sensor prototyping activities were aiming at the exploration of radiation tolerant design features. Wafer type CBM02[4] has been designed at CiS,

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[4] Project supported by German Federal Ministry of Economics and Technology (BMWI), project INNOWAT SPID.

Erfurt carrying 2 pixel sensors, 18 strip sensors and various test structures including PIN diodes [101]. The layout of the 4" wafer is shown in Fig. 4.19. The largest structures are the double-sided microstrip sensors with orthogonal 256 AC-coupled strips per side and 50 µm and 80 µm pitch. Every sensor is different and includes either structures for punch-through biasing, polysilicon biasing, or a combination of both. On the *n*-side, the strip insulation was realized using *p*-stop, *p*-spray and field plate techniques. Some sensors were implemented with a combination of different isolation techniques. Comparing to CBM01 sensors, edge isolation has been improved by introducing five additional guard rings with larger spacing preserving the outer dimensions of the sensors. A batch of 18 wafers has been produced using 285 µm thick *n*-type float-zone material, every wafer with a different doping concentration of isolating structures on the *n*-side.

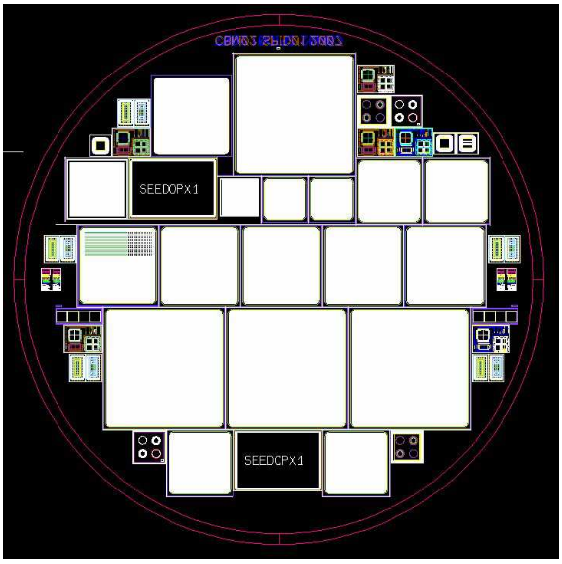

Figure 4.19: Layout of the CBM02 wafer with double-sided microstrip test sensors and other test structures for manufacturing process control.

The choice of biasing scheme is one of the elements of radiation tolerant sensor design. This becomes important at high accumulated fluences when charge collection efficiency decreases due to the trapping of signal charge and sensor needs to be operated with overbias. Two mostly used methods are punch-through and polysilicon biasing. The first one is based on the punch-through effect in p^+np^+ structures where potential of the strips is set by the voltage of the bias line separated by a small gap (typically of the order of 10 µm) [102]. This method offers significant simplification of production since it doesn't require additional lithographic steps to form the bias resistor. However, punch-through resistance that reaches GΩ level creates a substantial voltage drop reaching up to few tens of Volts. Voltage drop depends on the strip current which in its turn strongly depends on irradiation and detector bias. These circumstances make it difficult to control the actual voltage across the detector.

Another way to bias the strips in the detector is using bias resistor made of doped polysilicon. Such resistor is usually fabricated as a thin line with a meander shape in order to create a compact structure. The actual value of the resistance is achieved by modifying the polysilicon trace width which is, however, kept above certain minimum length (about 10 µm) to make the resistance value less susceptible to process variations. Typical sheet resistance of the implanted resistor is of the order of few kΩ/sq[5] yielding the final value of the resistance ranging from few MΩs to few tens of MΩs [103]. Naturally, polysilicon resistors introduce dead area into a sensor and increase the complexity of its fabrication comparing to punch-through biased sensors. Nevertheless, high-intensity applications favour the use of polysilicon biasing due to its better radiation tolerance [104]. Moreover, additional noise contribution related to the punch-through current has been reported in [105]. It is worth mentioning that certain sensor characteristics, e.g., interstrip resistance are impossible to measure with polysilicon biased sensors in a non-destructive way. Therefore, special test sensors with punch-through biasing should be placed on the silicon wafer along with main sensors. Two techniques may be combined within one sensor, where strips are biased with a polysilicon resistor at normal conditions and a punch-through structure is connected in parallel [106].

In double-sided silicon strip detectors, electrons generated in the bulk are collected by the n^+-electrodes. For the detectors made of n-type silicon, such strips form n^+-n-n^+ structures. This side of the sensor is called an ohmic side. A commonly known problem for the operation of the detector n-side as well as for n-in-n type pixel sensors is presence of positive charge and traps in the overlying oxide layer. Several contribution to this effect include [107]:

- interface trapped charge Q_{it} present due to the traps at the Si-SiO$_2$ interface that have energy levels deep in the band gap. The traps act as generation-recombination centers and originate from unterminated bonds of silicon atoms and impurities.

- fixed oxide charge Q_f located close to the Si-SiO$_2$ interface (within few nm). The charge is trapped due to ionic Si and uncompensated Si-Si or Si-O bonds.

- oxide trapped charge Q_{ot} that comes due to the defects in the SiO$_2$ crystal lattice. Presence of this type of charge is negligible in newly produced oxide but it increases with ionizing radiation (e.g., X-rays) or due to hot carrier injection into the dielectric.

- mobile ionic charge Q_m (e.g., Na, K) that may move in the oxide at extreme field or temperature conditions. This kind of charge affected the early stages of MOS structures and is not considered an issue nowadays.

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[5] Sheet resistance is a measure of resistance for thin films with even thickness. Dimension-wise, the units of sheet resistance are ohms, but for the sake of unambiguity "ohms per square" (denoted as Ω/sq or Ω/□) are also used.

Certain amount of positive charge is present even in the fresh oxide. Its density is increased by the ionizing radiation that creates electron-hole pairs. Most of these pairs recombine and among those which don't recombine holes are trapped with higher probability due to their much lower mobility in SiO_2 compared to electrons ($\mu_p = 2 \times 10^{-5}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ vs. $\mu_n = 20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$).

Positive oxide charges attract electrons from the silicon bulk and thus lead to a formation of *electron accumulation layer* under the oxide. This layer creates a conductive path between the n-strips and essentially shorts them leading to the loss of coordinate sensitivity. In order to interrupt the accumulation layer p-implants and fieled plates are used:

- p-stop: intermediate floating p-type strip between the readout strips. The design task for p-stop isolation is to find optimal implant width and geometry (e.g., single implant between two strips vs. individual implant surrounding every strip.)
- p-spray: large-area and low-dose surface doping. Advantageous, because no additional mask is required for patterning the implants. For pre-irradiated sensor, high-field region builds up at the strip edges, therefore p-spray dose has to be chosen carefully in order to prevent electrical breakdown.
- moderated p-spray: combination of the two approaches mentioned above. Medium dose p-spray is combined with relatively wide p-stop in the middle.
- field plate: MOS gate structure biased negatively with respect to the n^+-strips. Inconvenience related to this type of isolations comes from the necessity to have additional bias for the field plate.

Type of isolation technique has to be chosen depending on the radiation hardness and high voltage requirements [108]. The final design choice is a tradeoff between interstrip capacitance and detector breakdown voltage. Thus, for the p-spray, breakdown voltage increases and interstrip capacitance decreases with irradiation [109]. This happens because oxide charge compensates the p-spray charge. Surprisingly enough, both of these trends are beneficial for the detector operation, therefore annealing of the ionizing radiation defects is detrimental in this case.

Comparing to p-spray, p-stop implants feature higher doping concentration that leads to formation of high-field regions at the implant edges. Potential of the p-implant is set by the neighboring n^+ electrodes. When certain maximum potential difference between the strip and p-implant is reached, breakdown happens in the silicon bulk. p-stop potential is higher for wide implants, that is why narrow p-stops are preferred for higher breakdown voltages. This is equivalent to the statement that p-stops have to be placed further away from the n-strips for better breakdown performance (in case of more complex p-stop configuration than just a single p-stop between two strips). However, due to the fact that electron accumulation layer acts as an extension of the n^+-strip narrow p-stops give rise to higher

Name	**Pitch, μm**	**Biasing scheme**	**N-side isolation**	**Guard rings**
Twpsp12	80	punch	p-spray	p-side
Twpsp13	80	punch + poly-Si	p-stop	p-side
Twpsp14	80	punch	p-spray	p-side
Twpsp15	80	poly-Si	p-spray	p-side
Twpsp2	50	poly-Si	p-spray	p-side
Twpsp22	50	punch	p-spray	p-side
Twpsp23	50	punch + poly-Si	p-stop	p-side
Twpsp24	50	punch + poly-Si	field plate	p-side
Twpsp25	50	punch	p-spray	both sides

Table 4.5: Technology variations within the CBM02 sensor family.

interstrip capacitance. As the surface oxide charge increases with irradiation, interstrip capacitance also increases.

Finally, the combination of p-stop and p-spray (also called moderated p-spray) allows to have sufficiently high initial breakdown voltage before irradiation due to medium dose p-spray and low interstrip capacitance after irradiation due to wide p-stop.

A value that quantifies the quality of interstrip isolation is *interstrip resistance* that reaches $O(\mathrm{G}\Omega)$ for well isolated n-strips. Measurement procedure for interstrip capacitance, resistance, breakdown voltage, etc., are described later in Sect. 5.1.

Table 4.5 shows technology variations within CBM02 detector family. Apart from applying various isolation techniques for different sensors within a wafer, different wafers from the batch had different p-implant dose and implantation energy: $(1.1 - 2.0) \times 10^{13}\,\mathrm{cm}^{-2}$ at 70 keV for p-stops and $(3.5 - 5.0) \times 10^{12}\,\mathrm{cm}^{-2}$ at the energies of 80–115 keV for p-spray.

Wafer type CBM03

Based on the first prototype CBM01 and experience with the technology wafer CBM02, the new design CBM03[6] realizes a large double-sided sensor with the strips under a stereo angle on both sides [111]. This design is favoured for aspects of the module assembly but requires interconnecting the short corner strips on both edges through lines on a second metal layer in order to read out the sensor from one edge per side only. In total, the wafer requires 19 masks for production. The CBM03 design has the following features (see Fig. 4.20 for wafer layout):

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[6] Developed within EU Project ULISI, FP7 HadronPhysics2.

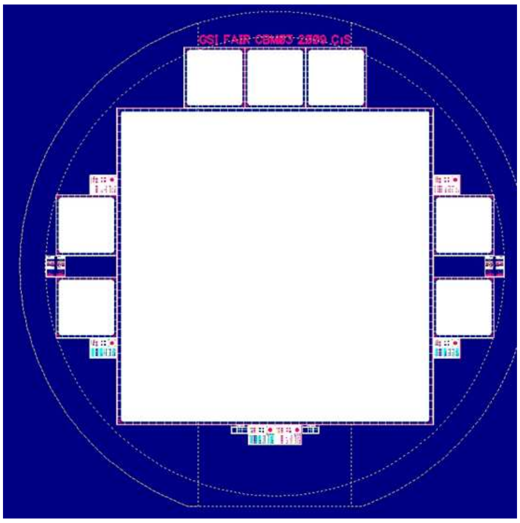


Figure 4.20: Layout of the CBM03 wafer (4" diameter) with the main sensor in the center and various test structures.

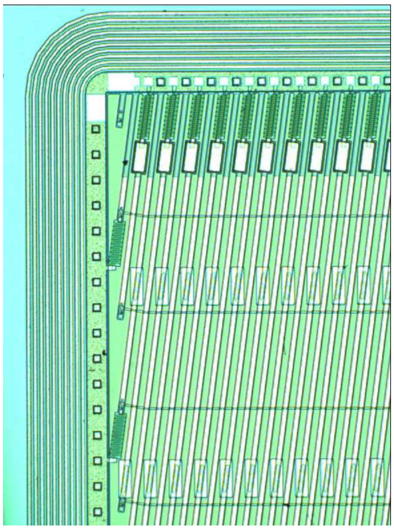


Figure 4.21: Photo of a front side of the CBM03 main sensor with strips under ±7.5° stereo angle and double metal interconnections of the corner strips.

- n-type float-zone silicon material
- double-sided layout
- 1024 strips per side
- stereo angle ±7.5°
- 58 µm strip pitch
- AC-coupled readout
- 1 DC pad and 4 AC pads per strip
- poly-silicon resistor plus punch-through biasing
- p-spray isolation on the ohmic side
- two metal layers per side
- 10 guard rings
- outer dimensions $6.2 \times 6.2\,\text{cm}^2$

Symmetric design of the p- and n-side of the sensor, in particular with respect to contact pads geometry, allows to facilitate the production of analogue microcable which disfavours the kinks in the conducting lines needed to read out the strips at stereo angle as large as 15°. The use of twice smaller stereo angle at both sides (i.e., ±7.5°) allows to rotate the contact pads with respect to the strip orientation as shown in Fig. 4.21, thus keeping the conductor lines at microcable straight. Apart from that, similar cable structure for both sides of the sensor reduces the effort for module production.

Additionally to the main sensor, CBM03 wafer includes smaller test sensors as well as company test structures. Baby sensors typically used for simple tests such as determination of full depletion voltage or breakdown voltage have the following geometrical parameters:

- 50 µm strip pitch
- 90° stereo angle
- 192 strips
- 20 µm strip width
- sensor size $1.18 \times 1.18\,\mathrm{cm}^2$
- single level metallization

Close-up of the corner of a baby sensor is shown on Fig. 4.22.

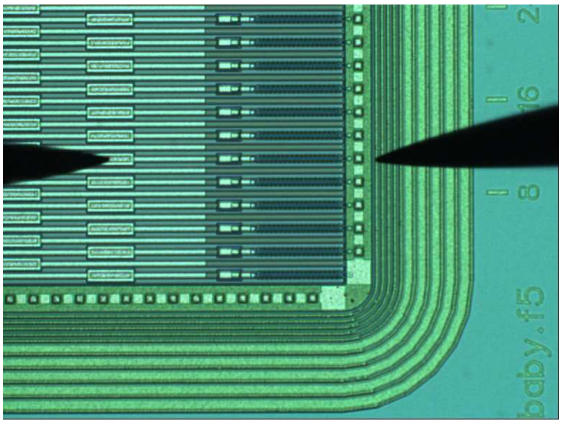


Figure 4.22: Photo of the CBM03 baby sensor corner with 10 guard rings and mixed polysilicon + punch-through biasing.

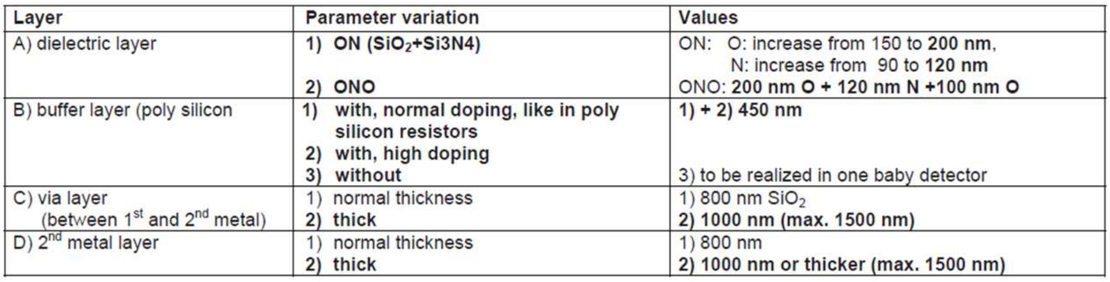
Wafer type CBM03′

In preparation of the next full-size prototype microstrip sensor CBM05, short circuits in the AC coupling layer have been addressed in the intermediate design CBM03′. Discovered problems with the coupling capacitors in a prototype sensor CBM03 are described in section 5.1.2 (part “Coupling capacitance”).

Measurements indicate that thin oxide layer was shorted in certain areas. This may be due to the complex structure of the detector. The processing steps for 19 masks, including the two metal layers per side, may have introduced stress there. A more sturdy layout including a slightly increased thickness of some of the layers has been proposed for the next prototype.

Technological tests have been prepared, reusing the masks of layout CBM03 for the production of a single-sided prototype CBM03′. After testing the intermediate prototype, production will be started for a batch of the next double-sided full-size prototype CBM05. Like the previous prototype, it comprises 2 × 1024 strips of 58 µm pitch arranged under a stereo angle of ±7.5° on an area of 62 mm by 62 mm. The detector is laid out for readout connections at its top and bottom edge, involving double metal interconnections of the corner strips so that sectors of daisy-chained detectors can be built and arranged on the Silicon Tracker's ladders.

Modifications implemented in the CBM03′ wafer are summarized in Table 4.6. First evaluations have identified the design improvements that eliminate the short circuits in the AC coupling capacitors. Optimized parameters will be used for the production of the CBM05 sensors.



Layer	Parameter variation	Values
A) dielectric layer	**1) ON (SiO_2+Si3N4)** **2) ONO**	ON: O: increase from 150 to **200 nm**, N: increase from 90 to **120 nm** ONO: **200 nm O + 120 nm N +100 nm O**
B) buffer layer (poly silicon	**1) with, normal doping, like in poly silicon resistors** **2) with, high doping** **3) without**	**1) + 2) 450 nm** 3) to be realized in one baby detector
C) via layer (between 1st and 2nd metal)	1) normal thickness **2) thick**	1) 800 nm SiO_2 **2) 1000 nm (max. 1500 nm)**
D) 2nd metal layer	1) normal thickness **2) thick**	1) 800 nm **2) 1000 nm or thicker (max. 1500 nm)**

Table 4.6: Summary of the parameter space for an improved full-size sensor.

Wafer type CBM04-FSD

Double-sided silicon microstrip sensor R&D has been continued with the technology wafer CBM04-FSD[7] that focuses on the investigation of radiation tolerant design elements with particular focus on the isolation techniques on the ohmic side of the sensor. Present design comprises novel isolation technique - Schottky contact isolation, based on the barrier properties of metal-semiconductor interface. Unlike blocking *p*-implants that cause high electric field either prior to or after irradiation, Schottky barrier isolation promises low field intensity and low interstrip capacitance providing still enough isolation to suppress the electron accumulation layer between the neighboring *n*-strips. Another advantage of this type of isolation is that no additional mask is required for patterning the *p*-implants between the strips on the ohmic side.

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[7] Supported by German Federal Ministry of Economics and Technology, project INNO-KOM-Ost.

Wafer batch produced of the n-type material with $\langle 111 \rangle$ crystal orientation has resistivity in the range of 3.5–5.5 kΩ cm. Sensor thickness is 285 µm that is less than the industry standard of 300 µm due to mechanical treatment of the raw wafers. The first step in the production cycle, before photolithography and ion implantation take place, is wafer polishing needed to guarantee the proper quality of the sensor surface.

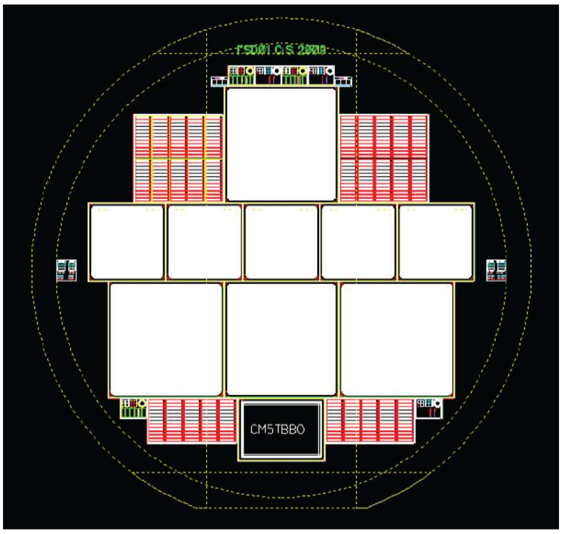


Figure 4.23: Layout of the CBM04-FSD wafer with two types of sensors. Different isolation techniques for ohmic side are utilized for different sensors while keeping the same contact pad pattern.

Out of many sensors present on the multi-project wafer CBM04-FSD (see Fig. 4.23), two sensor types are relevant for CBM (seen on the layout as white squares). The geometry of the sensors with respect to strip pitch, bonding pad layout and sensor dimensions has been preserved from the wafer CBM02. The difference in size between small and big sensors is dictated by the different pitch. Apart from that, two sensor types feature different strip width to pitch ratio as can be seen from the Table 4.7.

Typical views of the p-side and the n-side of the sensors are shown in Fig. 4.24 and Fig. 4.25, respectively. P-side of the *bo4pr* type sensor features guard rings with variable width. Every even strip ends with a DC pad and a polysilicon resistor connecting the strip implant and the bias rail, thus implementing the polysilicon biasing. Every odd strip is separated from the bias rail by a narrow gap in order to form a punch-through biasing structure. Design of the n-side of the *bo5tb* sensor type does not include guard rings and polysilicon resistors so that only punch-through mechanism is available to bias the strips. As seen in the photo, the interstrip gaps are covered with a metal layer that implements Schottky barrier isolation for the ohmic side.

Common to the design of both sides of the sensor are alignment marks in the

Parameter	**Big sensor**	**Small sensor**
Pitch, μm	80	50
Strip per side	256	256
Strip width, μm	40	20
Chip size, mm^2	23×23	15.3×15.3
Guard rings	15	15
Pads per strip	4 AC + 2 DC pads	4 AC + 1 DC pads
Sensors per wafer	4	5

Table 4.7: Geometrical parameter table of two sensor types from the CBM04-FSD wafer.

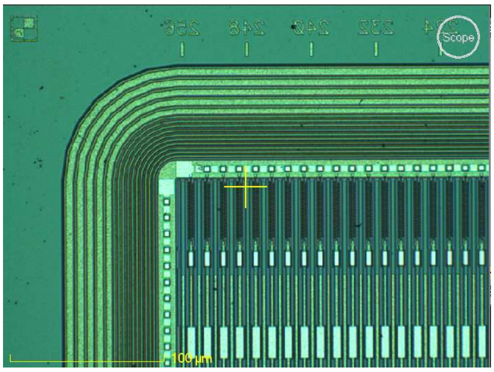


Figure 4.24: Sensor type *bo4pr* (n-side) with polysilicon + punch-through biasing and variable guard ring spacing.

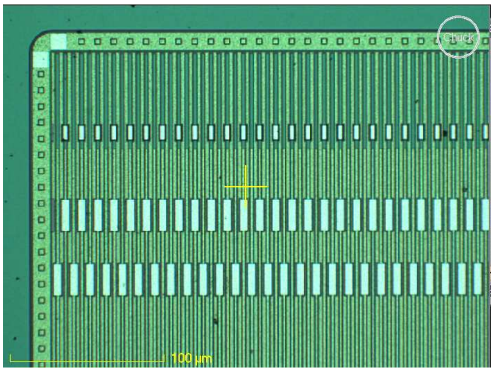


Figure 4.25: Sensor type *bo5tb* (n-side) with no guard rings and pure punch-through biasing.
Schottky barrier isolation is seen as a metallization between the strips.

sensor corners as well as strip numbering that marks every 8th strip. For the convenience of the user, sensor type and name of the side can be found on the sensor using a microscope (not visible on the photo).

Despite the common geometry and bonding pad topology, all sensors have different structure. Variations of design parameters are summarized in Table 4.8. The width of Schottky isolation electrodes and their passivation, type of sensor biasing as well as presence of guard rings on the n-side of the sensor are the technological variables implemented in the CBM04-FSD wafer design.

The use of novel isolation technique for the n-side of the sensor makes investigation of the interstrip parameters of the irradiated sensors, e.g., capacitance and resistance, the main goal of the characterization effort.

Name	**Guard rings**	**Biasing**	**Poly-resistor width**	**Schottky contact width**	**Schottky contact passivation**
bo5tb	p-side	punch	no	21	open
bo4pr	both sides	poly-Si	5	no	
bo4pa	both sides	poly-Si	5	18	
bo4pw	p-side	poly-Si	5	18	
bo4nx	p-side	poly-Si + punch	5	18	open

Table 4.8: Technology variations for different sensor types within the CBM04-FSD wafer.

Wafer type CBM05

Wafer CBM05 has been planned as a reiteration of CBM03 wafer production. Wafer material and geometrical parameters such as sensor dimensions, strip width to pitch ratio, stereo angle and AC pad geometry have remained unchanged. Placement and size of the DC pads also remained intact but additional DC pad will be introduced, giving two DC pads per strip.

Complex design and numerous production steps involving 19 photolithographic masks resulted in technology flaws detrimental for the yield of operational channels. Large fraction of the AC coupling capacitors has shown short circuits due to defects in the capacitor dielectric material. Also, during the characterization some other sensor parameters appeared to be not optimized for the use in long ladder-type detector modules. For example, standard metal layer thickness for both metallization levels turned out to be insufficient for long signal paths as in the case of daisy-chained sensors. The problem arises from the series resistance that contributes to noise of the preamplifier proportionally to the $\sqrt{R}$, where R is the total series resistance attached to the front end. In the STS detector modules, where up to three 6.2 cm long sensors may be daisy chained, noise contribution from the series resistance (in the current CBM03 implementation) surpasses the contribution from sensor strip capacitance and microcable trace capacitance.

These major modifications as well as smaller design improvements that came up during the sensor characterization can be summarized in the following list:

- improved high-voltage tolerance of the AC capacitors by introducing thicker or stacked dielectric layers
- thicker metal layers in the first and second metallization levels in order to reduce noise contribution from the series resistance
- 2 bias structures and 2 DC pads per strip (1 DC pad at each end) for easier probing

- planar AC pads to provide bondable surface

- improved labeling for easier handling with respect to the complex module integration requirements

Before starting the production of the CBM05 wafer some of the above mentioned improvements will be implemented on the test structures in a separate production run.

The sensor characterization routines and measurement results are presented in Chapt. 5.

4.3.2 Single-sided microstrip detectors

Reconstruction of the two-dimensional space points can be done with a combination of two single-sided sensors mounted back-to-back. Detector modules based on the single-sided sensors are considered as an alternative solution for the inner part of the tracking stations. The choice of substrate material and operation voltage allow for operation of the sensors with acceptable charge collection efficiency throughout the experiment lifetime.

The estimations of radiation environment for the STS detector (Sect. 4.1.2, 4.1.4) give for the central region the maximum fluence of about $4 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$ accumulated in six years of operation. The full depletion voltage as a function of proton fluence is shown in Fig. 4.26. The conversion between the proton and equivalent neutron fluence is done using the relation

$$\Phi_{eq}[n_{eq}/cm^2] = \kappa \Phi_p[p/cm^2],$$

where κ is a hardness factor. For the 23 MeV protons available at Cyclotron facility (Karlsruhe, Germany) that is often used for irradiations of silicon microstrip detectors, the value of $\kappa = 2.0$ has been reported [112]. The plot shows the fluence dependence of the full depletion voltage V_{FD} for silicon wafers manufactured using different technologies. For the standard technology V_{FD} is significantly higher than for the oxygen enriched silicon wafers. Operation the microstrip detectors at lower bias reduces the leakage current leakage current and breakdown probability. Therefore, diffusion oxygenated wafer technology is suitable for the high radiation environment [113].

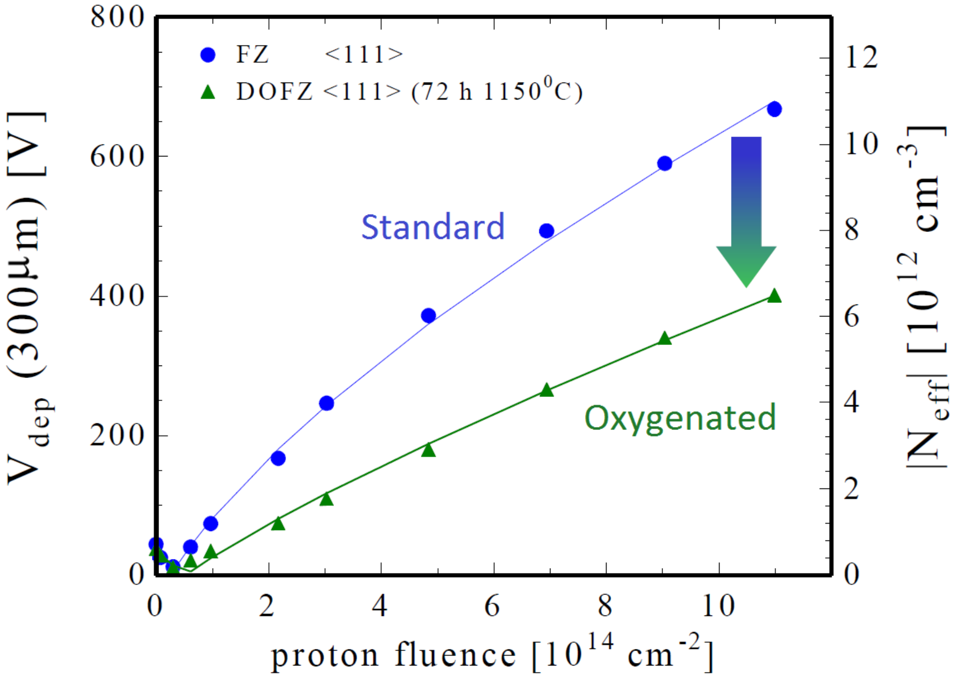
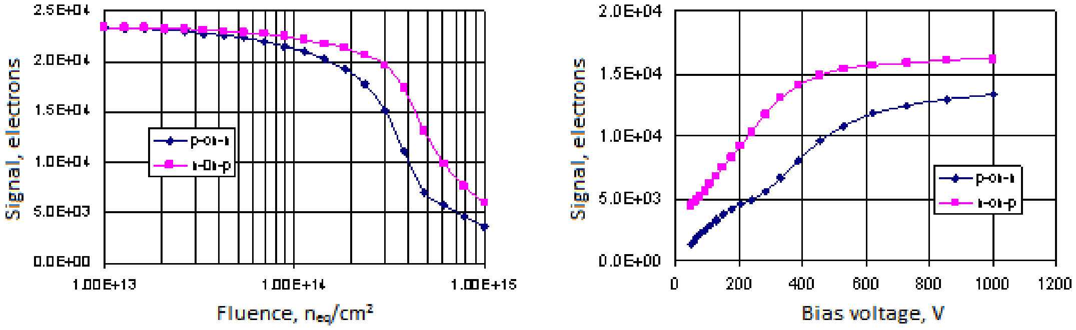


Figure 4.26: Effective doping concentration and full depletion voltage as a function of proton fluence for different wafer technologies (courtesy of M. Moll).

Performance of the single-sided sensors of p-on-n and n-on-p type have been evaluated [114] using the double peak PTI model [115]. Collected signal charge as a function of fluence is presented in Fig. 4.27a. At fluence of $4 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$ both sensor types collect enough charge to remain operational, however collected charge for the p-on-n type sensor is about 40% smaller than for the n-on-p type sensor. Observed reduction in charge collection efficiency and discrepancy between two cures can be explained in terms of a charge drift length, defined as $L_{dr} = v_{dr}\tau$, where v_{dr} is drift velocity and τ is charge carrier lifetime. At fluence around $\Phi = 10^{15}\,\mathrm{n_{eq}/cm^2}$, the drift length becomes smaller than the sensor thickness. This leads to the reduction of signal amplitude, thus both curves decline. The amplitude for the n-on-p type sensor is higher because n^+ electrodes collect electrons that have higher mobility than the holes. Voltage dependence of the signal charge is shown in Fig. 4.27b. The signal in n-on-p sensor rises with bias voltage and saturates at about 400 V, whereas signal saturation for p-on-n sensor is less pronounced.

In a sandwich detector module, bias voltage of at least 300 V will have to be provided in order to collect sufficient signal charge during the whole detector lifetime up to the fluence of $\Phi = 4 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$.



(a) (b)

Figure 4.27: Fluence dependence of signal amplitude at 300 V bias voltage (left) and voltage dependence of the amplitude for p-on-n and n-on-p sensors at irradiation fluence $4 \times 10^{14}\,n_{eq}/cm^2$.

Potential structure of a detector module based on single-sided sensors is shown in Fig. 4.28. The sensors are mounted back-to-back on the support structures. Short corner strips are interconnected via a flat microcable glued to backside of the sensor. Proposed approach offers simplification of the sensor structure by avoiding the double metallization. Simpler sensor design is beneficial to the production yield and stability of operation.

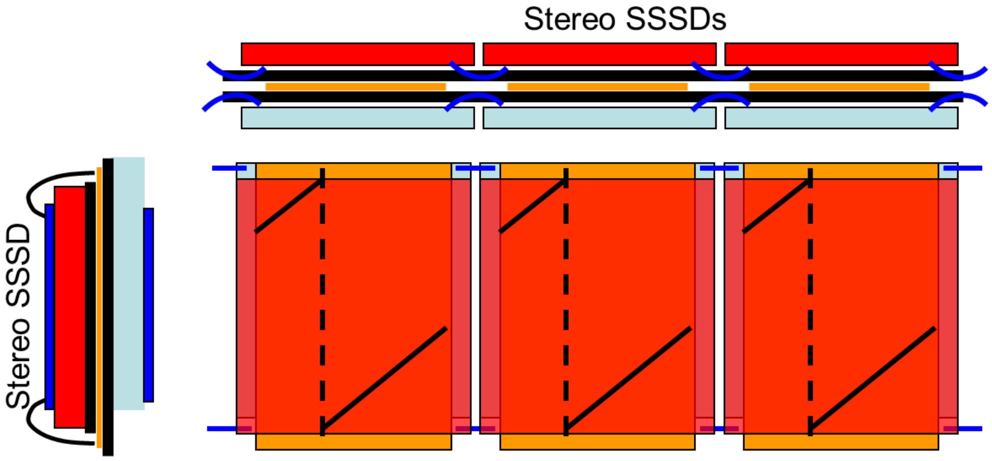


Figure 4.28: Structure of a detector module with single-sided sensors. The sensors are shown in red and light blue. Flat microcables (shown in orange) are wire bonded to the sensors.

4.4 Development of front-end electronics

The Silicon Tracking System project aims at construction of a ladder-type detector module integrated with a multi-chip block of front-end electronics. The detector module serving as a building block for the construction of the system has to fulfill the requirements coming from the desired physics performance and operation conditions. High channel density and spatial resolution of $\sim 15\,\mu\text{m}$ in the bending plane are needed to provide particle momentum reconstruction with a typical resolution of 1.5%. Associated with fixed-target collision geometry, highly non-uniform hit distribution in the plane, perpendicular to the beam axis, requires a variable channel granularity along the module. There is an additional constraint: the STS detector including sensors, analogue readout cables, front-end electronics and first stage of the data acquisition chain has to fit into the available space given by the aperture of a dipole magnet.

Timing requirements to the front-end electronics are dictated by the beam conditions and type of events to be triggered on. CBM will operate at a DC-beam that excludes the possibility to use the synchronization of electronics readout with the beam. The DC-beam offers the advantage of uniform distribution of the interaction rate in time and thus a uniform load on the data acquisition system. The decay topology of open charm hadronic decays, where secondary vertices formed by two or three daughter particles at the distance of several hundred micrometers from the primary vertex ($c\tau_{D^0} = 123\,\mu\text{m}$, $c\tau_{D^+} = 312\,\mu\text{m}$), requires full event reconstruction to select an event. Time needed for a trigger decision in this case largely exceeds the latency budget of a low-level trigger given by the front-end pipelines (typically from 0.1 µs to few microseconds, 4 µs for the LHC experiments). Thus, on-line triggering on detached secondary vertices at high interaction rates determines the requirements to the experiment and its data acquisition system. Self-triggering front-end electronics and free streaming data acquisition system running without a central trigger are needed to fulfill this task.

Since the development of an ASIC requires big effort and time, it was decided to explore an existing n-XYTER chip during the prototyping phase with subsequent modifications implemented at a later stage. Front-end electronics has been being developed using n-XYTER readout chip [133]. Sect. 4.4.1 and 4.4.2 discuss the the purpose and design of the chip and various front-end boards based on it.

Front-end electronics has been read out by data acquisition chain described in Sect. 4.4.3. Performance evaluation of the first detector systems has provided important feedback on the module design with respect to the sensor structure, connectivity of sensor and electronics, grounding, etc. Application of the prototype systems in the laboratory and beam measurements is presented in Chapt. 5 and 6.

Outlook on the further development of readout ASIC and front-end electronics is provided in Sect. 4.4.4.

4.4.1 The self-triggering n-XYTER front end chip

The n-XYTER chip, developed within the EU FP6 NMI3 project DETNI [134] dedicated to neutron applications, has been taken as a basis for the STS prototype front-end electronics. The chip is self-triggering and data driven due to the statistical nature of neutron signals. It comprises 128 channels with low-noise design. Every channel has two shapers with different shaping times (fast and slow) optimized for obtaining timing and energy information. The peak detect and hold circuit attached to the slow shaper provides amplitude measurement using an external ADC. A time stamp generator provides time walk corrected temporal reference to the signal. Timing and amplitude information allow to correlate signals in different channels in order to relate adjacent hits to a cluster, hits on different sides of a sensor to a space point and, finally, space points in different stations to a track. The chip features test modes for calibration and testing, such as test trigger mode and test pulse mode with variable pulse amplitude.

Originally developed for readout of microstrip detector employed for neutron signal measurement at high rates, n-XYTER chip (see Fig. 4.29) was well suited for construction of first prototype front-end boards due to its self-triggered architecture. The chip provides time and amplitude for signals of both positive and negative polarity. High channel count of the chip at 50.7 µm pitch matches reasonably well that of the prototype microstrip sensors – 50–58 µm. Dynamic range of the chip is 120 ke$^-$ that corresponds to about 5 MIP signals generated in 300 µm of silicon.

The final version of the readout ASIC for the STS will be better adapted for the CBM requirements. This includes reduced power consumption, moderate radiation tolerance, compatibility with a multi-chip front-end-board design (8 chips per front-end board) as well as operational scenario for overload situations that defines behavior of the front-end buffers in case of data lost.

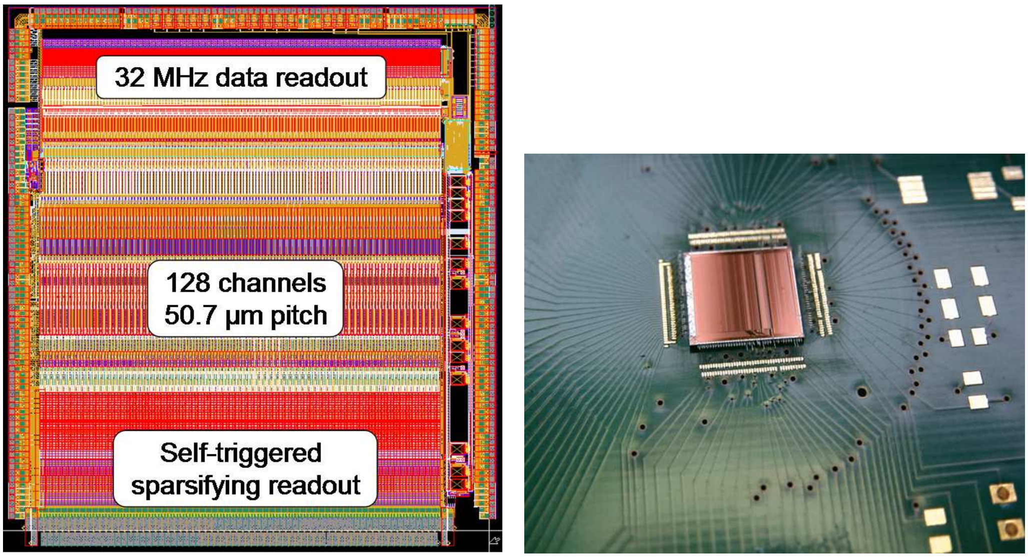


Figure 4.29: Layout (left) and photo (right) of the n-XYTER readout chip.

Chip design

The n-XYTER chip implemented in 0.35 µm CMOS process is a mixed signal ASIC that comprises 128 channels with a common analogue and digital back-end interface driven by a token ring arbitration circuit. The self-triggering front-end architecture is implemented using fast and slow signal branches where analogue signal triggers the time and amplitude measurement. Block diagram of an individual channel is shown in Fig. 4.30. Charge sensitive preamplifier based on a folded cascode circuit splits the signal into the fast and the slow branches optimized for time and amplitude measurement, respectively.

Fast shaper with 18.5 ns peaking time drives the timing-critical path where temporal reference to a signal is created. A discriminator followed by a time walk compensation circuit generates a trigger pulse that latches the time stamp and amplitude of the pulse. Amplitude and time stamp are stored in a 4-cell deep analogue and digital FIFOs (“first-in first-out” buffers) present in every channel. Fast trigger pulse derived from the time walk compensation circuit is used additionally to reset the peak detect and hold circuit, eliminating the need for external reset. Thus, the system operates in a self-triggered mode.

Slow branch is driven by the two-stage slow shaper with 139 ns shaping time that is a result of a tradeoff between the noise performance and pile-up probability. Second stage features fully differential design in order to feed a pulse of proper polarity to the peak detect and hold circuit that accepts signals of positive polarity only.

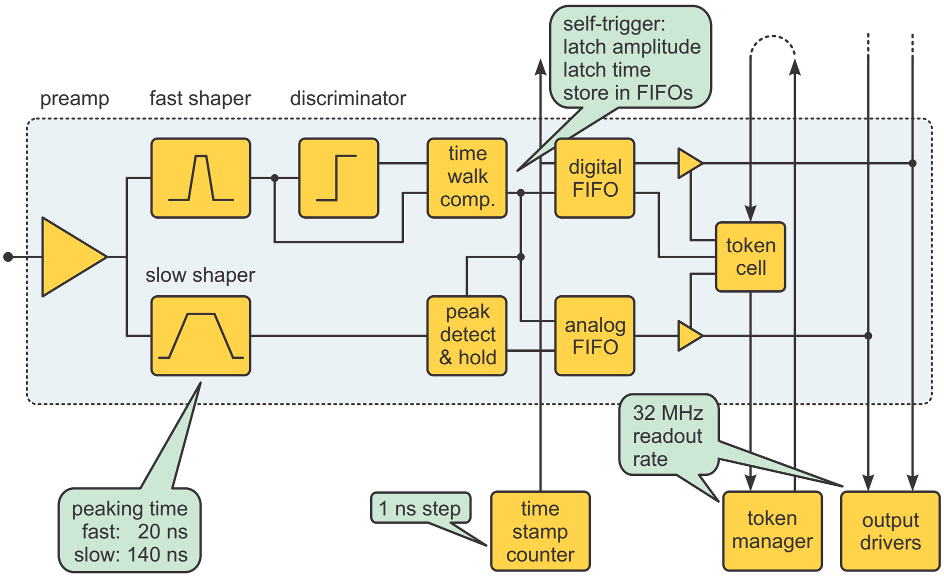


Figure 4.30: Architecture of the n-XYTER readout chip.

Token ring readout process

All 128 channels are read out by a single data readout channel using the token ring concept (see Fig. 4.31). A token can be understood as an exclusive right of a channel to use the data transmission channel at a given moment. The channels with data are read out in a clock synchronous manner at 32 MHz rate, whereas empty channels are skipped asynchronously. Combination of the token ring and individual channel FIFOs fulfills the derandomization of statistical signals that arrive at random times allowing to use efficiently the full bandwidth. The inherent features of a token ring readout are automatic zero suppression (sparsification) and bandwidth focussing on the firing channels. Token ring readout provides significant reduction of data volume and hence gives access to higher input data rates.

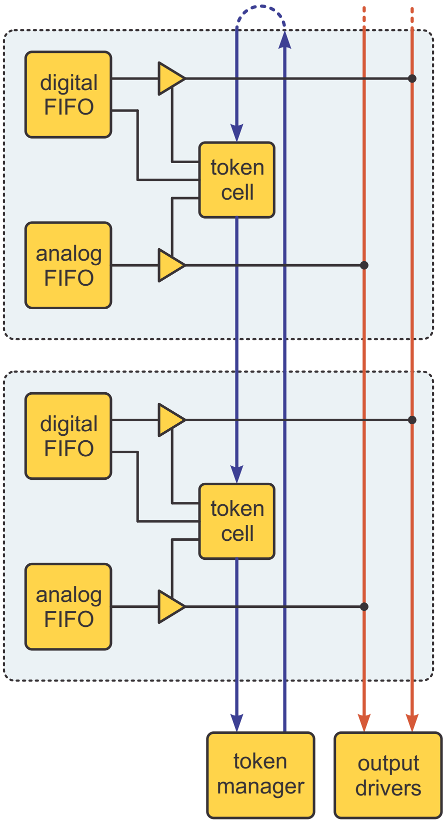


Figure 4.31: Token ring readout concept for automatic data sparsification.

A token is generated once the data appears in at least one channel. It starts from the token manager circuit, goes through the channels and arrives back at the token manager. When token stops at the channel that contains data, it generates the read signal and transports the analogue (pulse amplitude) and digital data (time stamp, channel number, data valid, pile up status, overflow signal) from the FIFO buffers to the output drivers. In the next readout cycle token goes to the next channel with data until it reaches the token manager. The token is released again and procedure is restarted once token manager identifies the data in the FIFOs.

The chip architecture with individual channel FIFOs and token ring readout scheme is able to process Poisson-distributed data at 32 MHz average input rate with dead time not exceeding 4%.

Slow control of the chip

The n-XYTER slow control is done via I^{2}C interface. There are 46 8-bit registers that can be read or written. The purpose of the registers is listed below:

- 16 mask registers with a mask bit for every channel
- 14 front-end adjustment registers for setting voltages and bias currents in the analogue part of the chip
- 2 configuration/status registers
- 2 diagnostic counters: missing token counter and FIFO overflow
- 2 test-delay registers to generate delay of test pulse and test trigger
- 1 shift register 129 bytes deep for local channel threshold trimming (bit 0 to 4) and individual selectable analogue channel shutdown (bit 5)
- 3 clock delay registers

Front-end architecture of the n-XYTER is designed to accept pulses of both positive and negative polarity. Slow shaper consists of two stages, with its second stage being fully differential. The subsequent block in the slow channel branch – peak detect and hold circuit – accepts only positive signals. Regardless of the polarity of the input pulses, the output pulses of positive polarity are fed into the peak detector using the switches. The switches are controlled by the configuration registers. In addition to that, the DC-levels have to be adjusted to provide the dynamic range for a pulse of a given polarity.

Change in the DC operating level in the slow shaper manifests itself as a shift of the pedestal position. Since fast shaper is AC-coupled to the discriminator, position of its DC level is of less importance and only has to fit the analogue window to avoid clipping of the pulse. Position of the DC levels in fast and slow shapers are controlled by several registers. Among them *VbiasS* and *VbiasF* are of importance to configure the front-end of the chip during the routine usage.

4.4.2 Front-end boards

The first n-XYTER based front-end board (FEB) was developed to provide readout for prototype detector systems of different types. A front-end board was designed to be applied with silicon detectors as well as with gas detectors (GEM, RICH), provided that the signal was attenuated to fit into the n-XYTER dynamic range. Signal amplitude from a gaseous detector may vary depending on the chosen high voltage amplification and reaches up to $\sim 10^6\,e^-$.

A general purpose board is equipped with one n-XYTER chip, one 12-bit ADC and necessary power supplies to provide standard operating voltages of 3.3 V and 1.8 V to the electronic components. There are three separate power supplies for analogue circuits, digital circuits and ADC in order to reduce interference between different domains due to shared signal paths. The back-end communication of the FEB contains control and data lines. High-speed LVDS connections are used for data transfer, while SPI and I^2C interfaces are used for slow control of the n-XYTER and ADC, respectively.

Connectors on the FEB are compatible with those on the prototype readout controller SysCore V2. Combined together, readout controller and front-end board form a full data acquisition chain for testing the detector systems in the laboratory and in the beam of particles.

Figure 4.32: n-XYTER front-end board (revision D) mounted on the cooling block for temperature stabilization.

Production of the general purpose n-XYTER FEB has undergone several iterations to improve manufacturability, stability of operation and introduce monitoring tools. Front-end board revision D shown in Fig. 4.32 is an 8-layer printed circuit board with physical size of $(10.5 \times 9)\,\mathrm{cm}^2$. Some of the features implemented in FEB rev. D based on the experience from the previous revisions are listed below:

- increased bond pitch
- 0.3 V drop linear voltage regulators (LDOs) used

- separate power supply regulators (analogue, digital, ADC)
- PT100 temperature sensor
- alternative connector pinout for separated LVDS and common mode signals
- test points for monitoring of signals and voltage levels
- I^2C and SPI spike filter

Monitoring capability has been added for temperature, various supply currents as well as reference voltages for fast and slow shapers in the test channel. Serial non-volatile memory (EEPROM) has been added for storing data, e.g., unique ID of the FEB, list of introduced modifications etc.

In order to stabilize the temperature of the chip at a constant value of 20 °C, a massive aluminum cooling block with internal water circulation has been designed complementary to the FEB. A small copper plate is fixed on the bottom of the PCB to bring the chip into a thermal contact with the cooling block.

4.4.3 Data acquisition chain

Some of the CBM physics cases, e.g., in-medium modification of hadrons and indications for deconfinement at high baryon densities require measurement of signals with low cross section such as D-mesons or J/ψ [139]. In order to measure them with reasonable statistical significance, reaction products of heavy ion collisions have to be measured at typical interaction rates of 10 MHz. With up to 600 charged particles created in the detector acceptance, a significant part of the CBM detectors, including STS, will have hit rate exceeding $10\,\mathrm{kHz/cm^2}$. In addition, triggering on detached vertices of D-meson signals requires transport of large data volumes from the detector to a trigger system over relatively large distance (tens of meters). This calls for a high-throughput data acquisition system with data push architecture.

In order to acquire data from the front-end boards, a readout controller with basic DAQ functionality was required. The readout controller (ROC) is an interface board between front-ends of different detectors and data transport lines. The ROC is based on FPGA (field-programmable gate array), that enables gradual development of the ROC functionality as opposed to ASIC (application-specific integrated circuit) that requires long development time. The current version of the ROC and its layout are shown in Fig. 4.33. Due to the radiation environment conditions, FPGA-based ROCs cannot be used in all detector subsystems, therefore ASIC-based solutions will be provided for the part of the setup. However, for laboratory applications, including beam tests with moderate beam intensities, FPGA-based controllers provide a readout solution with high flexibility and relatively short development times.

Up to now, several generations of readout controller have been developed [140], [141]. The controller is based on the Virtex 4 FPGA and equipped with modular firmware that provides the following functionality:

- configure front-end electronics via I^{2}C (n-XYTER) and SPI (ADC) interfaces
- readout the data from up to 4 n-XYTER chips and an ADC or alternatively GET4 chips
- transfer data to the PC via copper (Ethernet) or optical connection using special CBM-net protocol [142]
- perform time synchronization with other readout controllers: in case of Ethernet connection via the exchange of synchronization messages with a subsequent correction of time stamps in the offline analysis; in case of optical lines by synchronizing the data bus
- accept logical signals (LVDS) and detect their edges with 2 ns resolutions.

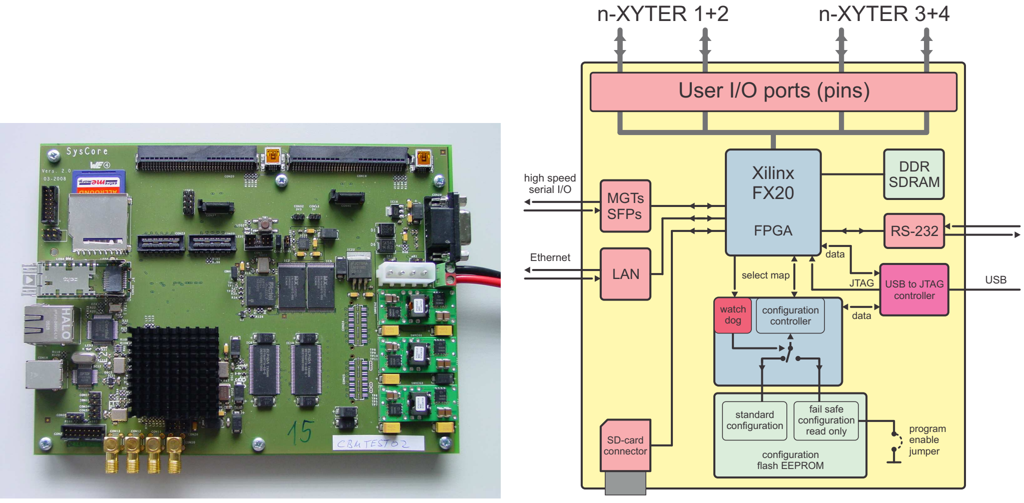


Figure 4.33: Photo (left) and layout (right) of the SysCore V2 readout controller.

The key component of the ROC is its firmware. The firmware has modular structure and consists of the *front-end module* with a chip-specific logic and the *transport module* that implements a communication logic. The interaction of modules is implemented according to the requirements of the CBM-net protocol and provides a FIFO interface for data transport, slow control interface, and a deterministic latency message mechanism needed for the synchronization of ROCs in large-scale systems.

The first implementation of the firmware contained front-end module for n-XYTER readout and transport module based on the embedded PowerPC core for Ethernet communication. Later developments included GET4 front-end module and transport module for communication via optical links. It was oriented at early availability for the users and does not require any additional hardware components. The data can be acquired on a standard Linux PC.

The firmware module for the optical link communication implements a more complete set of features. Running ROC with optical module requires additional hardware – Active Buffer Board (ABB) [143]. The ABB is based on Xilinx FPGA and features 4 optical connectors with 2.5 Gbps data rate each. The board is connected to a PC via PCI express interface and requires additional custom driver software.

In order to scale up the data acquisition system and concentrate the data transfer to the uplink, the Data Combiner Board (DCB) [144] has been developed. Data acquisition software and on-board firmware are in continuous development. Its main components Data Acquisition Backbone Core (DABC) [145] and ROClib [150] library for low-level hardware communication have been developed and tested in the laboratory measurements and beam tests. DABC software accept data independently of the transport module installed in the ROC.

4.4.4 Outlook on the development of the CBM specific front-end electronics

The requirements to the front-end ASIC are driven by the system design of the STS. The challenges are related to the high channel density of the system and noise load on the electronics due to detector module structure with long traces in the microcables and strips in the daisy-chained microstrip sensors. In the final ASIC, a tradeoff has to made between the power consumption, noise performance, amplitude resolution and speed of operation.

A prototype ASIC utilizing the time-over-threshold method offered a solution optimized for low power consumption [151,152]. The simple front-end architecture of the chip, based on the charge sensitive amplifier of the folded cascode type and a discriminator circuit, provided amplitude measurement at power consumption of 1.2 mW per channel.

In order to maintain the hit reconstruction efficiency at the required level $\varepsilon > 95\%$, it is crucial for the detector modules to operate with the lowest possible threshold. Such operation mode has been found incompatible with the developed ASIC prototypes due to the long time-over-threshold response (few µs) at low threshold which compromised the requirement of the high rate operation.

The design of the next prototype ASIC STS-XYTER with 128 channels has been started with focus on a particularly low-noise performance. The block diagram of a channel is shown in Fig. 4.34. The architecture implements separate channels for time and amplitude measurement optimized independently for time stamp precision and low-noise performance. For the reduction of noise occupancy at low threshold, information from the slow shaper with better noise performance is used to validate the hit occurrence in the fast shaper. The working specifications for the currently designed ASIC include power consumption better than 10 mW per channel, linear range of input charge 1–12 fC and detector capacitance up to 30 pF. The submission of the STS-XYTER chip for production is expected in summer 2012.

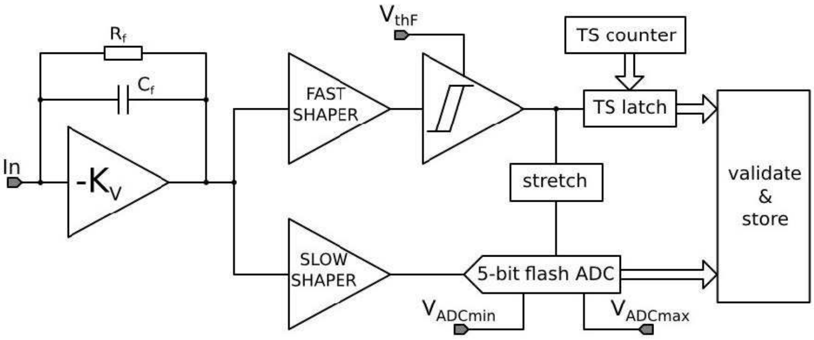


Figure 4.34: Block diagram of a single channel of the proposed STS-XYTER ASIC. The time measurement is validated by the energy measurement with higher threshold ($V_{thF} < V_{ADCmin}$).

The design options for the proposed architecture have been implemented in separate ASICs exploring the design of shapers, discriminator, time walk compensation circuit and trimming DAC circuit [153]. The FSDR16 test chip dedicated for the silicon strip detectors was among them. The chip has been manufactured in the UMC 180 nm CMOS process. The design includes two different shaper types (CR-(RC)^5 and nearly true Gaussian) with programmable shaping times.

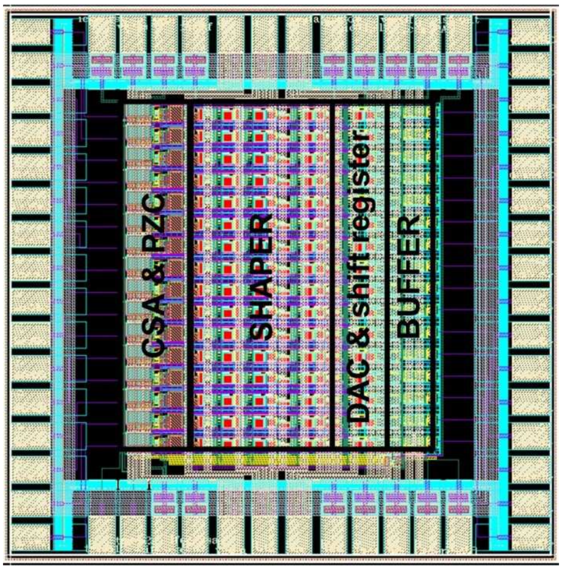


Figure 4.35: Layout of the prototype ASIC FSDR16 for studying the design options for the front-end architecture.

The FSDR16 block diagram and channel architecture are shown in Fig. 4.35. Each of the 16 channels of the chip is built with an analogue part comprising charge sensitive amplifier, pole-zero cancelation circuit and a shaper as well as digital part with shift register, 7-bit trimming DAC register for correcting the DC voltage spread in the shaper output and output buffer. Measurement of the chip has shown adequate operation of both shaper designs in fast and slow mode with power consumption below 5 mW per channel.

Currently considered architecture with separate channels for time and amplitude measurements is expected to deliver better noise performance and timing precision than the time-over-threshold approach at the expense of higher power consumption.

The STS front-end chip will be compatible with the experiment DAQ chain that is being developed for the readout of self-triggering front-end electronics and online event selection without the use of low-level triggers. The implementation of the final configuration of the DAQ chain requires new hardware developments so as to implement the functionality of the DAQ system: data acquisition, transport, processing and storage. The system concept is sketched in Fig. 4.36. Parts of the system will be separated among three experimental sites. Front-end electronics and data aggregation boards will be located next to the detector subsystems. The copper data lines from the front-end links are combined by the HUB ASIC responsible for data aggregation, synchronization and rate conversion [154]. The data form the copper lines for clock distribution, data and control are translated into the optical signals in the optical converter board that sends the data further to the service building via multi-mode optical fibre lines.

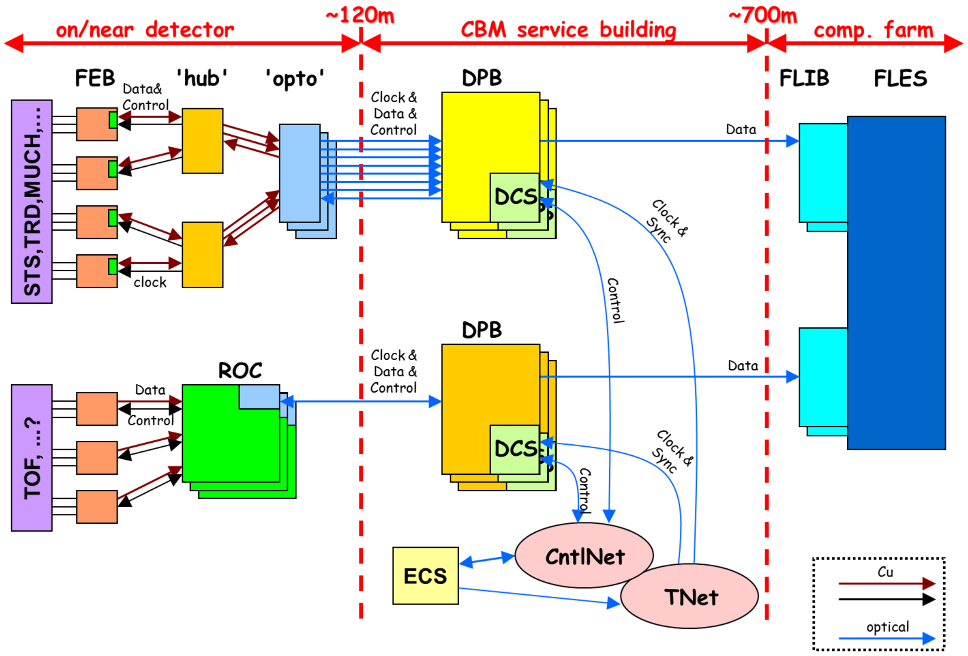


Figure 4.36: Architecture of CBM data acquisition chain. Dashed lines separate the experimental sites. Copper and optical connections are marked with different colours.

The aim of the data acquisition node located in the service building about 120 m away from the detector is further data aggregation as well as detector specific data processing. The Data Processing Boards (DPB) based on the FPGA can be (re)programmed to access the local data, for instance, within one FEB or a sensor, in order to change the data representation, e.g., by applying mapping, sorting, cluster finding and other feature extraction algorithms. Data Control System (DCS) is responsible for controlling the data flow from the detector to the computing farm. The clock distribution, synchronization and control lines come from the Experiment Control System (ECS). After the service building, the data are transmitted to the First Level Event Selector (FLES) [155] over the distance of about 700 m via single-mode fibre optic cables. By design, FLES is a supercomputer based on the hardware with a multi-core architecture for the parallel processing of massive data sets. The bandwidth and computing power of the FLES has to be high enough to enable full event reconstruction and selection online. The FLES is interfaced to the data lines from the service building via First Level Interface Boards (FLIB).

In the course of studies described in Chapt. 4 requirements to the components of the detector module have been formulated. Double-sided silicon microstrip sensors with radiation hard design connected with a microcable to the readout electronics have been chosen as a basic structure of the STS detector module. For module support structure, carbon fibre has been chosen as a low-mass material. Few iterations in development of front-end boards have been done in order to achieve finally its stable production quality and analogue response. Experience with different modifications of front-end boards and results of testing have been taken into account in the subsequent modifications.

4.5 Development of a low-mass detector module for the CBM environment

Prototype microstrip cables have been manufactured as patterned aluminum layers on polyimide carrier foils. Line pitches down to a few tens of micrometers are feasible depending on the length of the cable to be realized. TAB bonding to a sensor or readout electronics is done via openings in the polyimide foil.

First demonstrators manufactured with 14 µm thick, 20 µm wide aluminium traces have been manufactured with 100 µm pitch and successfully tested in the beam as a part of a prototype detector module.

Due to manufacturability reasons and for reduction of trace capacitance, signal paths must be arranged in a staggered manner across two signal layers. Design of the cable has been optimized using RAPHAEL package of Synopsis TCAD framework yielding trace capacitance of about 0.3 pF/cm and material budget between $0.10\%X_0$ and $0.17\%X_0$ [146]. The structure of the cable layers and material description is shown in Fig. 4.37.

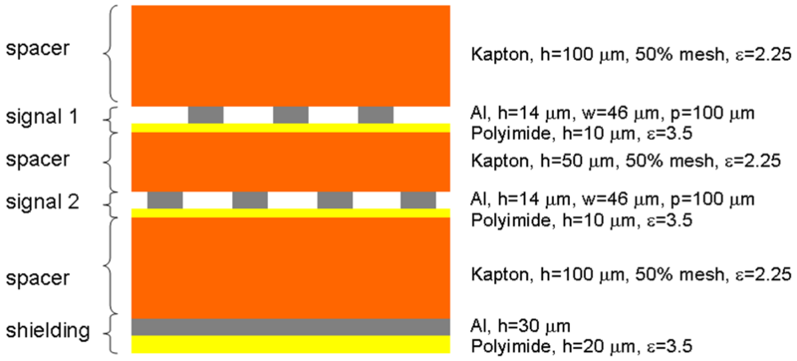


Figure 4.37: Detailed structure of the multilayer microcable with two signal layers and a shielding layer.

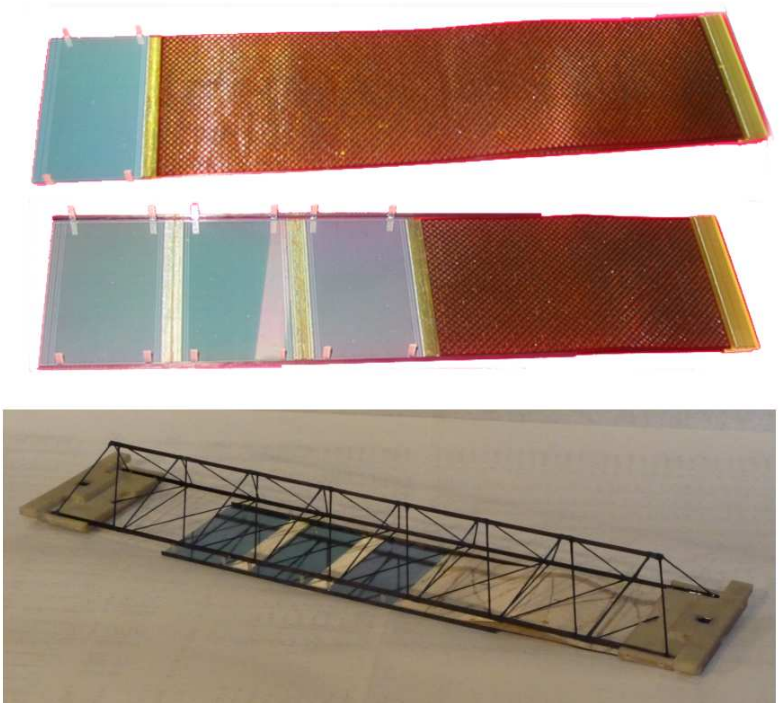


Figure 4.38: Prototype module components. (Above) Microcables with 1024 channels and effective pitch of 58 µm are TAB bonded to the microstrip sensors. L-shaped legs are attached to the sensors for mounting on the support structures. (Below) Ladder with mounted daisy-chained sensors and microcable.

Produced detector module components are shown in Fig. 4.38. The goas was to demonstrate the feasibility of TAB bonding with microcables attached to a single sensor or a set of tree daisy-chained sensors. Similarly, daisy chain interconnects are done using short TAB-bonded microcables. Ratio of defect connections was below 1% [147]. The sensors are fixed on carbon fibre support ladders with glass-fibre L-shaped miniature fixtures. Sensor and cable assembly mounted on the optimized version of the frame is shown in the same figure.

Crucial requirement to the support structures is mechanical rigidity to provide precise and stable sensor position. The frames fabricated with the use of the precision molds are linear within 100 µm. Their sides are flat within 50 µm. A frame of 1000 mm has a mass of 14 g.

An alternative design of the detector module for the STS with low mass design has been proposed in [148]. Module prototypes have been manufactured by AEROPLAST (Kiev). A support structure is a three-layer frame composed of two flat carbon fibre plates (0.25 mm thick) with foam layer in between. The foam layer with 1 mm thickness has a density of $0.7\,\mathrm{g/cm^3}$. The prototypes have been manufactured in three types to match sizes of sensor prototypes CBM01, CBM01-B1, CBM01-B2 (described in Sect. 4.3.1).

Chapter 5

Quality assurance of the STS prototype components

Characterization routines for double-sided silicon microstrip detectors are described in this section. These are the elements of quality assurance program that aims at establishing selection criteria of detectors for the STS based on radiation hardness requirements and STS system design including front-end electronics and data acquisition system. Parameters and performance of a silicon sensor have to be controlled over the whole life-time: after multistage production process, after module construction and between the experiment physics runs to control the effects of radiation damage to the sensors.

As a part of development of the quality assurance system for the detector modules, prototype tests have been performed for double-sided silicon sensors (current-voltage and capacitance voltage characterization), laser test stand for module readout tests as well as trigger system for characterization of the readout ASIC [116–121].

5.1 Characterization of double-sided silicon microstrip sensors

The task of the quality assurance is to check the correspondence of the sensors to their specification that ensures their proper manufacturing and future operation as a part of the detector module.

Silicon microstrip sensors for the STS are complex objects with their design driven by the experimental requirements. Operation in the heavy-ion collision environment at high interaction rates creates highly non-uniform track density across STS detector planes that demands high granularity sensors with low material budget. In addition, operation beyond the point of type inversion leads to ever increasing full depletion voltage and thus ever increasing heat dissipation of the silicon sensors. The main task of a microstrip sensor is to provide sufficient coordinate resolution in the mixed radiation fields with normalized fluence of up to $4 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$ and ionizing dose of up to 2 Mrad. The optimal value of a strip pitch, that serves as a main geometrical parameter of a sensor defining its position resolution, is obtained from the STS detector performance simulations. Furthermore, successful accomplishment of this task is conditioned by a number of parameters that depend on the sensor material and design, fabrication technology, front-end electronics and detector module integration as well as irradiation conditions and annealing scenario. These parameters include signal-to-noise ratio, full depletion voltage V_{FD}, interstrip capacitance C_{int} and backplane capacitance C_{back}, interstrip resistance R_{int} and number of dead channels, leakage current, breakdown voltage, width-to-pitch ratio of a strip, coupling capacitance, biasing resistors, etc.

Some of these parameters (e.g., full depletion voltage, interstrip capacitance and resistance) depend on irradiation, the others are determined by the design or technological process (e.g., number of dead channels). *Signal-to-noise ratio* S/N is a property of a detector module rather than of a sensor. In the final version of the STS during the long-term operation, operating temperature, grounding and shielding will have influence on the noise performance of a system and thus on the S/N ratio. Thorough optimization of these issues affects the module design and poses an appreciable challenge to the system integration.

Full depletion voltage of a sensor is directly proportional to the effective doping concentration N_{eff}. This, combined with a fact that V_{FD} is easy to measure via current-voltage (IV) or capacitance-voltage (CV) scan, makes V_{FD} a convenient parameter to monitor the radiation induced changes and annealing effects in the detector. Also, full depletion voltage is related to the bulk resistivity that can be calculated knowing the nominal wafer thickness using formula 4.1:

$$\rho = \frac{w^2}{2\varepsilon\mu V_{FD}}, \tag{5.1}$$

keeping the same denotation as in Eq. 4.1. Resistivity calculated in such a way reflects an average value over the wafer or sensor area disregarding the intra-wafer resistivity variation that may reach up to 10-15% [122] unless special measures like thermal treatment or neutron doping are taken [123].

Interstrip capacitance and backplane capacitance contribute to the total capacitance “seen” by the input preamplifier of the front-end electronics. Since noise of the preamplifier is proportional to the input capacitance, interstrip and backplane contributions have to be kept as low as possible in order to achieve optimal noise performance. Backplane capacitance of strip is given by the geometry and material, namely sensor thickness and silicon dielectric constant. Backplane capacitance C_{back} contribution doesn’t depend on irradiation. On the contrary, interstrip capacitance is sensitive to the ionizing irradiation that modifies the state of the surface dielectric layer by depositing positive charge into it. In addition for the n-strips, interstrip capacitance and its evolution, as the ionizing dose increases, is dependent on the type of strip isolation employed. According to different values of total strip capacitance for the p- and n-side of the sensor, the design values for the coupling capacitance have to be adjusted in order to satisfy the requirement $C_{coupl} > 10 \times C_{int}$. This rule of thumb ensures that the signal charge flows mainly into the preamplifier of the readout chip and not into the parasitic capacitances. Strip isolation techniques and their impact on interstrip capacitance are described in Sect. 4.3.1.

Interstrip resistance is a measure of electrical isolation between the neighboring strips that affects charge sharing. For a double-sided microstrip sensor, the value of DC interstrip resistance differs significantly for the n- and p-side due to the presence of electron accumulation layer at the interface between the silicon bulk and the surface oxide. On the p-side, electron layer is advantageous for strip isolation whereas for the n-side it would short-circuit all the strips unless special isolation structures are applied. Interstrip resistance on the n-side depends on the type and particular implementation of isolation structures. Their effectiveness in turn depends on the irradiation.

Due to many factors that may lead to a defect detector channel, such as a broken coupling capacitor, broken bias resistor or broken metal strip, particularly important is the *yield of the coupling capacitors* formed by the strip implant and readout electrode separated by the dielectric layer. In certain double-sided readout schemes, high DC bias potential is applied to the strip implant, whereas readout electrode has a potential of virtual ground set by the preamplifier of the front-end chip. In this case, significant voltage stress is applied to the dielectric material and capacitors show significant leakage current or electrical shorts. Such defects may disrupt a readout channel or even a whole front-end chip. Therefore, all the coupling capacitors in the sensor have to be tested for high-voltage compatibility before detector module assembly. Another requirement to the coupling capacitors is to have high capacitance value in order to provide good coupling of the signal into the front-end preamplifier. A natural way to increase the capacitance is to decrease the thickness of dielectric layer. This, however, conflicts with the high-voltage tolerance of the capacitors.

Characterization routines to control the device parameters can be divided into several groups:

- individual: to be controlled for every sensor
- collective: to be controlled for a few sensors out of the batch
- strip-wise measurements to determine operational channel yield
- destructive: conducted on a limited number of sensors of a given batch or on test structures to determine breakdown voltage V_{BD} of the sensor itself or breakdown voltage of the coupling capacitors V_{BD}^{AC}
- supplementary measurements performed on test structures to characterize process quality, e.g., determination of the flat-band voltage V_{FB}[1] that allows

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[1] Flat band voltage V_{FB} is a voltage applied to a MOS structure to reach the condition when

to extract oxide charge density Q_{ox} or surface current that are measures of SiO_2 and Si–SiO_2 interface quality, respectively. Also, measurement of the implanted strip resistance, metal strip and double-metal interconnect resistance may be related to the supplementary measurements that are not necessarily needed for every batch. These measurements are usually addressed during failure analysis to investigate the mistakes in technology process.

The quality assurance procedure defines a set of criteria that every sensor has to comply with in order to be accepted for further integration into a detector module and undergo readout tests. In order to compare the criteria with actual sensor parameters, following measurements have to be performed:

- on every sensor:
    - ◇ sensor leakage current I_{leak} vs. bias voltage (IV-curve) up to the onset of soft (reversible) breakdown
    - ◇ total backplane capacitance C_{tot} vs. bias voltage (CV-curve) to measure the V_{FD}
    - ◇ voltage stress test of coupling capacitance
    - ◇ strip leakage current I_{strip} measured at operational voltage V_{op} (different from V_{FD})
- on a few sensors out of a batch or test structures:
    - ◇ interstrip resistance R_{int}
    - ◇ interstrip capacitance C_{int}
    - ◇ strip backplane capacitance C_b
    - ◇ coupling capacitance C_{AC}
    - ◇ resistance of a polysilicon resistor R_b; alternatively: effective resistance of a punch-through biasing structure R_{eff} as a function of sensor bias voltage
    - ◇ breakdown voltage of the dielectric material of the coupling capacitors V_{BD}^{AC} (destructive)
    - ◇ strip implant resistance R_{p+}, R_{n+}
    - ◇ metal (readout) strip resistance R_{Al}
    - ◇ double metal interconnect resistance R_{DM}

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bands adjacent to the semiconductor-insulator interface remain flat as opposed to accumulation, depletion and inversion conditions or when no voltage is applied across the MOS structure. Physically, flat band voltage corresponds to the situation when no net charge is induced in the semiconductor.

Some of the above mentioned parameters such as I_{leak}, V_{FD} and V_{BD} or yield of coupling capacitors depend on the properties and quality of a particular silicon wafer and local defects introduced during the photolithographic steps. Although a silicon wafer after production represents a single mechanical entity, images are translated onto the wafer reticle per reticle. Therefore, possible defects have to be checked for every individual sensor.

Other parameters reflect the quality of patterning, diffusion and deposition that are the three classes of technological processes, usually same for all the wafers within a batch. Such parameters as C_{tot}, R_{int}, C_{int}, C_b, C_{AC}, R_b, V_{BD}^{AC} depend on wafer doping and its uniformity, implantation of the readout strips and interstrip isolation structures, patterning and doping of polysilicon to form a bias resistor, growth of coupling dielectric layers and passivation with subsequent etching. These measurements may be performed on a few sensors randomly selected from a batch.

5.1.1 Requirements, infrastructure and software for characterization of microstrip sensors

Testing of the microstrip sensors requires specific environmental conditions typical for testing of microelectronic components with additional requirements arising from the peculiarities of the sensor structure. Measurements have been performed in a clean room at constant temperature of 22 °C and relative humidity of 20%. Test setup has been placed in a light-tight enclosure shielded from electromagnetic interference.

Stable temperature is a particularly important requirement for current measurements, since reverse bias current of a *pn*-junction depends on the temperature as $I_R(T) \propto T^2 \exp(-E/kT)$, where activation energy E equals the band gap energy in silicon $E_g = 1.12$ eV for preirradiated sensors and 1.2 eV for the irradiated ones [124]. This semiconductor property is used to renormalize the current measured at different temperatures to the one at standard temperature of 20 °C for comparison purpose.

The basic element of the test stand for sensor characterization is a probe station with moving chuck that allows strip-by-strip sensor testing in a (semi-)automatic mode. Measurements presented in this work have been conducted on a probe station Süss PA300 featuring full electromagnetic/RF shielding as well as a chuck movable in X, Y, Z directions and rotatable by up to 7.5°. For contacting the sensor pads, probes equipped with tungsten needles with 8 µm tip radius have been used. Such probe needles provide a reliable contact (low contact resistance) with metal surface and enough probe force to break through the pad oxide layer without damaging the surface too much. For the low-ohmic measurements where needle contact resistance is critical (e.g., metal trace resistance measurement), four-terminal sensing (also known as Kelvin sensing) is advisable in order to avoid measurement errors due to the impedance contribution of the wiring and contact resistance. Some of the measurements are performed on the sensor strips with bias voltage applied when both sensor sides have to be contacted. For this purpose, special printed circuit boards have been developed that allow sensor biasing. The assembly consists of two PCBs with openings for a sensor and bias traces on one side only. Openings have a balcony milled out such that a sensor can be nested between the two boards without using a glue. Bias traces on the PCB are wire bonded to the sensor pads with 1-2 bonds per side leaving the sensor under test virtually intact after testing. During the tests on a probe station the assembly is fixed on a chuck and bias voltage connection is provided to it inside of the station via feedthroughs. Strips under test are contacted by the needle probes.

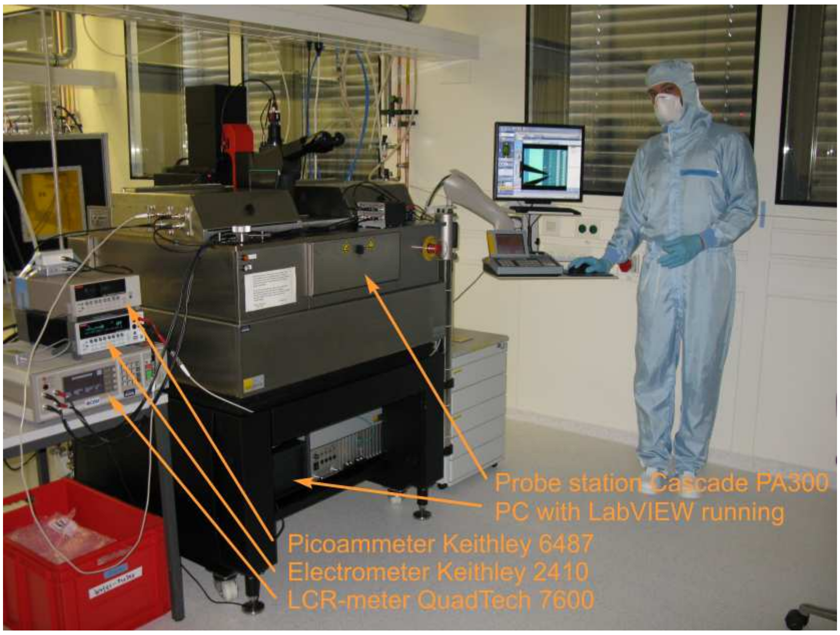

Figure 5.1: Laboratory infrastructure for microstrip sensor characterization in the clean room including shielded probe station, picoamperemeter, electrometer, LCR-meter and an instructed operator.

A complete set of measurement devices for sensor characterization includes:

- high voltage power supply for detector bias with voltage up to 500 V
- low voltage power supply for DC resistance measurement with voltage up to 10 V (bipolar)
- LCR-meter for capacitance measurement in the range from 0.1 pF to several nF at frequencies between 100 Hz and 1 MHz
- amperemeter for current measurement in the range between 0.1 nA and 10 mA
- crossbar switch suitable for high voltage and low-capacitance applications in order to reconfigure the setup without the need for re-cabling

Current results have been obtained with a set of devices that include:

- Keithley 6487 picoammeter/voltage source with 10 fA resolution and HV bias up to 500 V
- Keithley 2410 high-voltage source-meter that measures current in 10 pA to 1 A range with 0.012% basic measure accuracy and sources voltage up to ±1100 V
- QuadTech 7600 LCR-meter with AC test voltage from 20 mV to 5 V at frequency from 10 Hz to 2 MHz and external DC bias voltage up to 200 V

Measurement routines have been implemented in NI LabVIEW[2] and combine the functionality to control multiple devices, visualize the measurement and store the data in text format and as an image for quick reference. The devices are controlled via GPIB or RS-232 interface for the reason of handling and programming simplicity as opposed to high speed, that is usually not required for the laboratory measurements.

Processing of the stored data has been done within ROOT[3] analysis framework using macros. This approach is helpful to tackle large amounts of data acquired for different sensors and measurement routines. In particular, it allows to plot and fit the data as well as to extract the curve features and store them in a separate file.

5.1.2 Measurement routines and extracted parameters of double-sided microstrip detectors

Current-voltage characteristic measurement

Leakage current of a microstrip detector comes largely due to the applied reverse bias with additional contributions arising from the bulk generated, surface generated and avalanche breakdown current. It is, therefore, an important observable to characterize overall electrical performance of the device. From the quality assurance point of view, adequate current-voltage characteristic is a prerequisite for a sensor to be accepted for further tests and vice versa allows to discard a sensor at early stage in case of deviations from the expected behavior.

Device connection scheme for the measurement of sensor leakage current versus bias voltage (IV-curve) is shown in Fig. 5.2. By contacting the terminals of the measurement circuit to the bias pads on both sides of the sensor, total current through all strips is measured. Current limiting 1 MΩ resistances are introduced into the circuit in order to protect the sensor from breakdown in case of uncontrolled increase of current.

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[2] LabVIEW by National Instruments is a graphical programming environment used to develop measurement, test, and control systems (`http://www.ni.com`)

[3] ROOT is an object oriented framework for large scale data analysis (`http://root.cern.ch`)

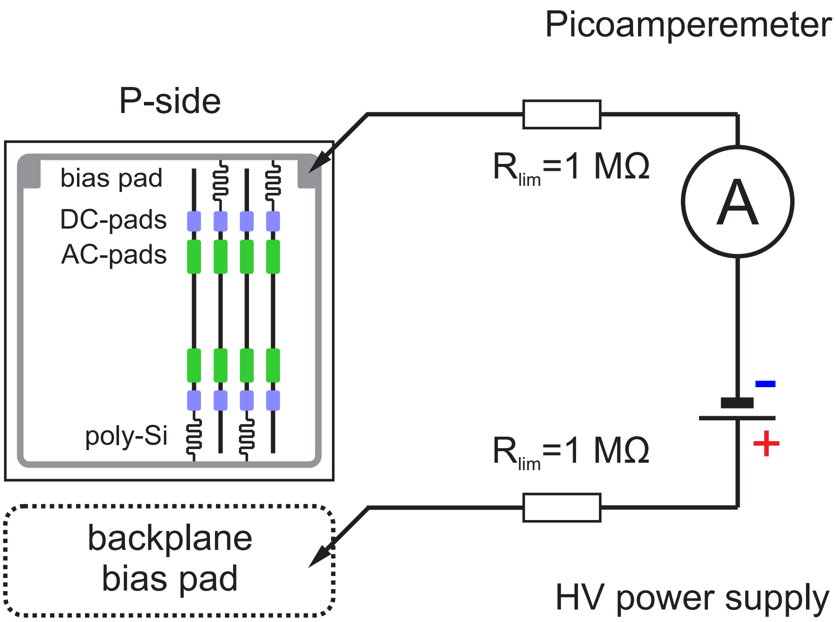
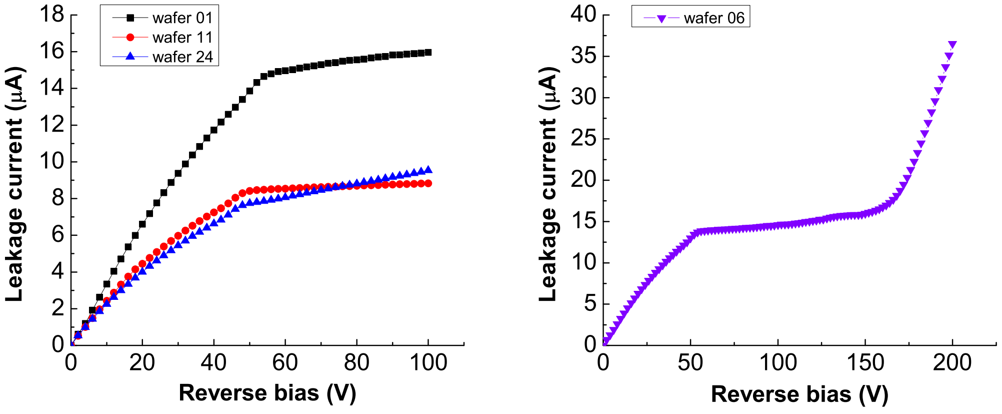


Figure 5.2: Connection scheme for total leakage current measurement.

Typical IV-curve measured for the sensors from different wafers of the CBM03 type are shown in Fig. 5.3. At bias lower than full depletion voltage V_{FD}, space charge region expands from the junction side towards ohmic side and leakage current follows a $\propto \sqrt{V_{bias}}$ dependence. As the depleted region touches the structured backplane of a sensor, additional small contribution from surface current adds to the current (this effect is barely distinguishable at the plots). After reaching full depletion condition, the current saturates or exhibits a small rise. Further increase of the bias voltage leads to an avalanche breakdown that manifests itself as an increase of the current by many orders of magnitude. At this point, breakdown starts in high-field regions (e.g., *pn*-junction curvature or surface mechanical damage) and is reversible (see Fig. 5.3b). In case of severe overvoltage, hard breakdown occurs and leads to the destruction of the device.

One may extract two parameters out of the IV-measurement of a microstrip detector: full depletion voltage V_{FD} and breakdown voltage V_{BD}. However, due to a certain risk involved in V_{BD} determination, one usually tests the detectors up to a certain voltage that exceeds the expected operation voltage. Selection of optimal operation voltage becomes a significant issue after irradiation that leads to an increase of leakage current and decrease of charge collection efficiency. Increase of leakage current may be dangerous for the device due to the thermal runaway. In addition, local electrical breakdowns at high bias voltage increase the amount of noisy channels. Thus, optimal operation voltage is determined by the power dissipation and noise performance considerations.

Determination of V_{FD} from an IV-curve is not always clearly visible or even not possible, although leakage current may comply with sensor acceptance criteria.



(a) (b)

Figure 5.3: Current-voltage characteristics of the CBM03 type sensors (a) and example of breakdown behavior at overvoltage condition (b).

In this case, V_{FD} is obtained from the measurement of total detector capacitance versus bias voltage.

Capacitance-voltage characteristic measurement

Capacitance-voltage characteristic (CV-curve) is used for a determination of full depletion voltage V_{FD} and for determination of backplane capacitance C_b contribution for a single strip along with the other methods of measuring C_b. Capacitance of a pn-junction below V_{FD} depends on the bias voltage as $C \sim V_{bias}{}^{-1/2}$ and stays constant above full depletion voltage. This kind of voltage dependence is monotonous and thus doesn't clearly show the point of full depletion. Dependence $1/C^2\,(V_{bias})$ algebraically obtained from the CV-curve is linear below V_{FD} and constant above it. Full depletion voltage is then defined as a point of intersection of two lines fitted to the linear regions of the dependence. Strictly speaking, this argumentation is only applicable to a planar pn-junction. Due to the patterned backside, CV-curve of a double-sided microstrip sensor shows additional features that are translated to a $1/C^2$ plot. Nevertheless, $1/C^2$ technique allows unambiguous determination of the full depletion point for double-sided sensors. Device capacitance has been measured using an LCR-meter based on the AC impedance technique where a device under test is probed with AC voltage and resulting AC current amplitude and phase are measured.

Measurement frequency should be selected carefully. This is particularly important for irradiated sensors, where charge carrier concentration in the undepleted bulk becomes relatively low and charge mobility decreases. In this case, free charge carriers contribute less to the measured capacitance that manifests itself as weak bias dependence of the bulk capacitance. For this reason, irradiated sensors have to be measured at lower frequencies down to 100 Hz.

A measurement scheme for total backplane capacitance is shown in Fig. 5.4. A high voltage power supply and a capacitance meter are connected to the bias pads of the sensor in order to apply both DC bias voltage and AC test signal will to the sensor. In this configuration, devices may interfere with each other, i.e., unexpected current paths may be established: AC current will flow through the high voltage power supply and DC current will flow through the capacitance meter. In order to avoid interference, capacitors have been introduced into the leads of the capacitance meter in order to block the DC current and resistors have been introduced into the power supply leads in order to block the AC current. Thus, both AC and DC currents will flow through the device under test.

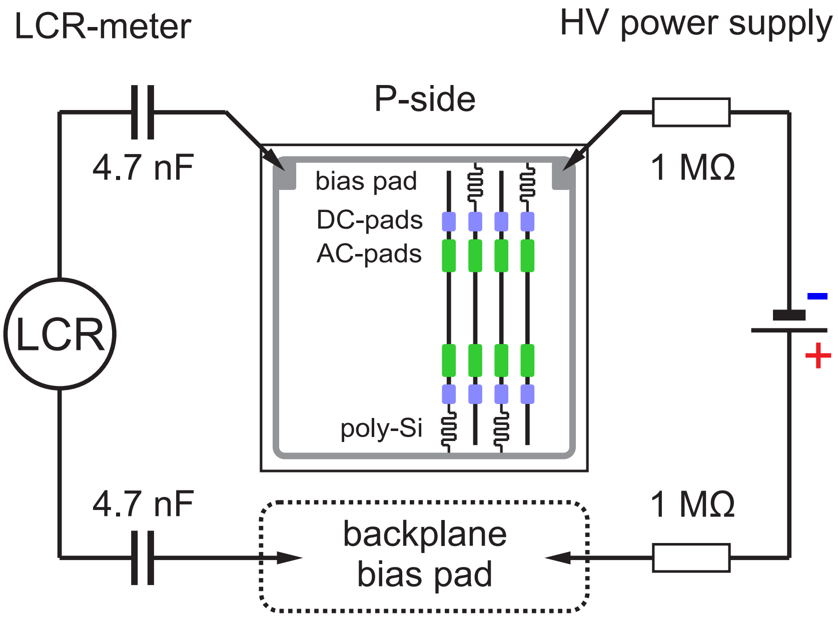
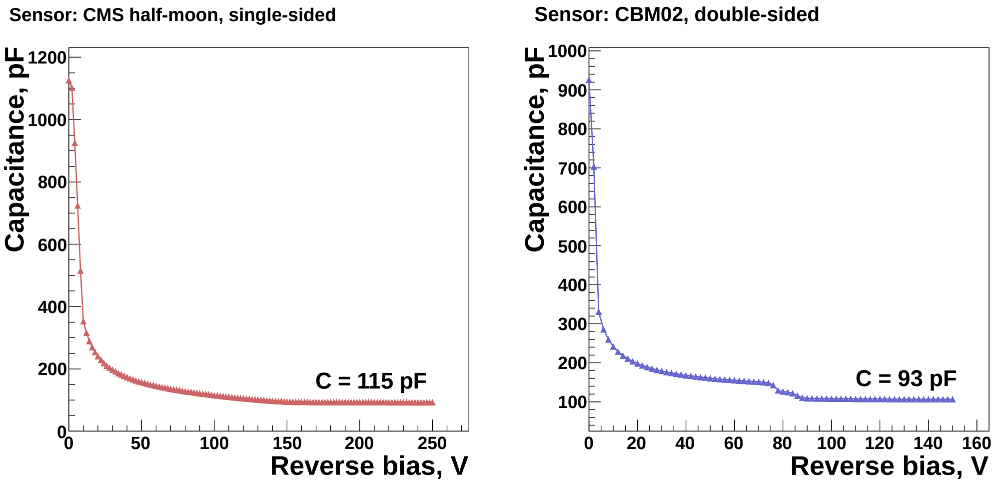


Figure 5.4: Connection scheme for a total backplane capacitance measurement. HI and LO terminals of the capacitance meter can be exchanged, that is why they are not labeled on the scheme.

Bias voltage dependence of total backplane capacitance of microstrip detectors is shown in Fig. 5.5 for a single-sided test detector (CMS baby sensor) and a double-sided one (CBM02 baby sensor). For the single-sided sensor (see Fig. 5.5a), capacitance is a monotonous function of bias voltage and saturates at the value of $\sim 115\,\text{pF}$. Similar behavior is observed for a double-sided sensor (see Fig. 5.5b) below the full depletion. At a voltage close to V_{FD} an additional drop in the measured capacitance occurs when space charge region touches the backplane. This effect is related to the fact that n-side is structured. Above V_{FD} capacitance saturates at $\sim 93\,\text{pF}$. The capacitance plot for two sensors shown in Fig. 5.5 should not be compared quantitatively due to their unequal area and thickness.

Full depletion voltage can be determined from the $1/C^2$ plot shown in Fig. 5.6. In case of a single-sided sensor (see Fig. 5.6a), V_{FD} is obtained from the intersection



(a) single-sided (b) double-sided

Figure 5.5: Examples of capacitance-voltage characteristics for single-sided and double-sided sensors. Monotonous for single-sided sensors, voltage dependence of total backplane capacitance for double-sided sensors exhibits an additional drop at full depletion voltage.

of two straight lines fitted to the branches of the curve. Due to complex structure of the $1/C^2$ plot for double-sided sensors (see Fig. 5.6b), similar approach to extract V_{FD} is difficult to apply and bias voltage after which the curve saturates should be considered as V_{FD}.

Full depletion voltage is often monitored during the lifetime of experiment because it depends on the substrate doping concentration N_D. Doping concentration is strongly modified during the irradiation and annealing process. It has to be monitored in order to operate the detector at optimal conditions, i.e., at minimal full depletion voltage. The following expression relates V_{FD} to the effective doping concentration and wafer thickness:

$$V_{FD} = \frac{eN_D d^2}{2\varepsilon_0 \varepsilon_{Si}}$$

where ε_0 is the vacuum permittivity, ε_{Si} is the relative permittivity of silicon ($\varepsilon_{Si} = 11.68$), N_d is the effective doping concentration and d is the sensor thickness.

Capacitance obtained from the CV-measurement can be used to extract the bulk thickness applying the formula for a parallel plate capacitor:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}$$

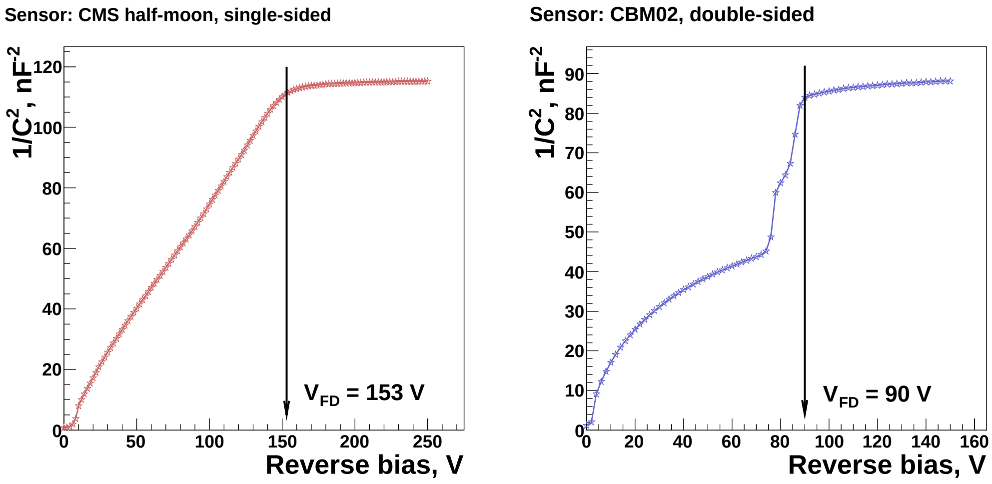
where A is the area of the capacitor plate.

Assuming that the actual wafer thickness and V_{FD} are known one may calculate the bulk resistivity:

$$\rho = \frac{d^2}{2\varepsilon_0\varepsilon_r\mu_e V_{FD}}$$

where μ_e is the electron mobility and ρ is the material resistivity.

The parallel plate capacitor formula doesn't take into account the fringe field effects and can be applied only for orientation to the microstrip sensors, where both capacitor plates are highly segmented. For this reason, the aforementioned method of resistivity determination is often applied not to the sensors but to the test structures (planar diodes) with well defined area.



(a) single-sided (b) double-sided

Figure 5.6: Examples of 1/C^2-V plots for single-sided and double-sided sensors. (a) For a single-sided sensor V_{FD} corresponds to a point, where linear dependence of 1/C^2 on bias voltage changes to a constant value. (b) For a double-sided sensor the curve makes a step-like change at V_{FD}.

Interstrip capacitance

Interstrip capacitance comprises the main contribution to the input capacitance of the front-end electronics and thus defines its noise performance. The ratio of interstrip capacitance C_{int} to strip backplane capacitance C_b affects the charge collection efficiency across the interstrip gap and thus position resolution of a microstrip sensor. The actual value of the C_{int} depends on the sensor geometry as well as on the material and fabrication process. Moreover, interstrip capacitance depends on the irradiation that modifies the state of the Si–SiO_2 interface at the detector surface. Therefore, interstrip capacitance has to be measured in order to estimate the noise performance of the system and its evolution during the lifetime of the experiment.

Capacitance has been measured using balanced bridge type LCR-meter and a probe station with up to four connections to a detector via needle probes.

QuadTech 7600 LCR-meter provides a DC contact to the measured impedance. During the measurements, strips on the n-side have been contacted via DC-pads, although AC-pads are suited equally well for this task .

In order to avoid voltage drop in the cables, four-terminal sensing has been employed and allowed using long cables between capacitance meter and device under test without compromising the measurement accuracy. Close to the device under test, terminals of the capacitance meter are connected to a high voltage isolation box, inside which four wires are combined into two and passed through capacitors to block the DC voltage from the sensor power supply. The value of the blocking capacitance 4.7 nF is chosen such that is doesn't influence the measured value in the range of 1–100 pF. After the capacitors, HI and LO terminals are branched and can accommodate up to tree probes each.

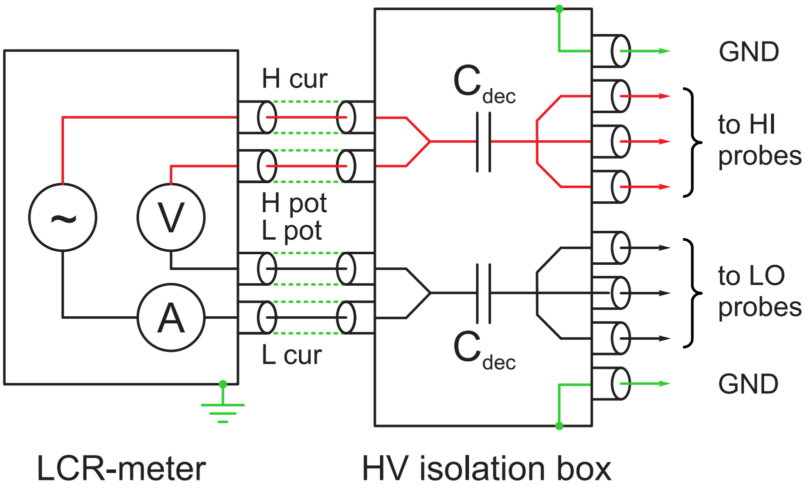


Figure 5.7: Scheme of the LCR-meter connection via high voltage isolation box. Decoupling capacitance $C_{dec} = 4.7\,\text{nF}$ is used. HI and LO terminals are branched to allow up to tree probe connections each. Two ground connections are used in some of the measurement schemes.

The measurement frequency was 10 kHz and the amplitude of the AC signal was 50 mV and 1 V. LCR-meter sources an AC-signal and measures the resulting current, voltage and phase shift between them to obtain the active and reactive components of the impedance. These values do not provide an unambiguous description of the real object under test. For an adequate interpretation, measurement model has to be chosen that reflects the underlying impedance model. The use of a series or parallel capacitor model depends on the capacitance value and test frequency (i.e., on the reactance value $\frac{1}{i\omega C}$). Series equivalent circuit is more adequate for low-impedance loads and parallel is suitable for high-impedance ones [125]. For interstrip capacitance measurement, "C_P–D" model has been chosen, that corresponds to a capacitance C_P connected in parallel with resistance (parasitic component that denotes dielectric leakage resistance) and dissipation factor $D = R_S/X_S$ (reciprocal of the quality factor that relates active and reactive impedance of the circuit to each other or ratio of the energy lost to the energy stored in the capacitor).

Capacitance-voltage characteristics have been measured as a function of bias voltage up to 150 V bias that is approximately twice higher than the full depletion voltage of the studied CBM02 type sensor. Connection of the high voltage power supply to the sensor corresponds to that on the scheme in Fig. 5.2. Resistors in the bias connections block the high frequency signals such that impedance of the power supply does not distort the capacitance measurement. The value of the blocking resistors has to exceed the impedance of the capacitance at a given frequency. For example, impedance of a 1 pF capacitor at 100 kHz frequency is about 1.6 MΩ.

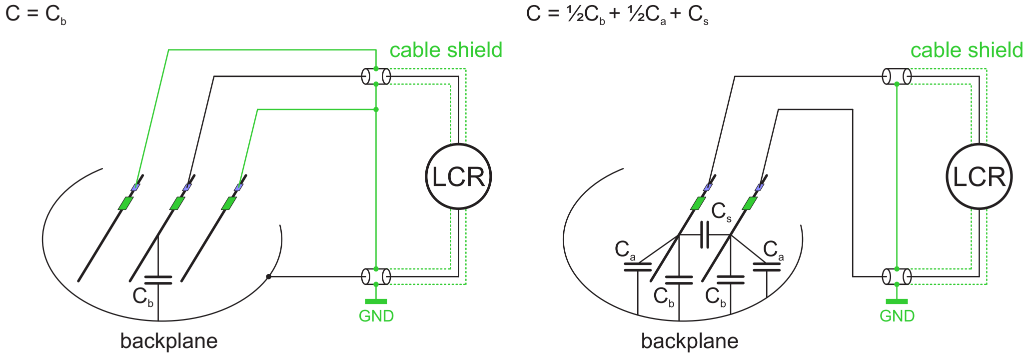
A single strip of a sensor is capacitively coupled to its neighbors and to the backplane both directly and via neighboring strips. The task of the measurement is to distinguish interstrip capacitance from different parasitic contributions to the observed capacitance value or to eliminate the effect of those contributions. There are two approaches to this problem:

- using grounding probes that compensate the effect of additional capacitance contributions.
- conducting several measurements without grounding probes but with different number and configuration of connected strips. An equivalent scheme can be assigned to every configuration. A set of equations can be solved with respect to the unknown capacitance contributions.

The model to describe capacitance contributions for a particular strip includes three values: capacitance to an immediate neighbor C_s, capacitance of a strip to the backplane C_b and capacitance to the backplane via neighboring strips C_a. Both approaches with and without grounding probes allow to estimate the corresponding contributions. Thus, a “straightforward” measurement of interstrip capacitance, where terminals of the capacitance meter are connected to two neighboring strips as shown in Fig. 5.8b gives a value

$$C = C_s + 1/2C_b + 1/2C_a$$

that is higher than the actual interstrip capacitance C_s provided that parasitic contributions C_b and C_a are not negligible. A measurement scheme for backplane capacitance C_b using grounding probes is shown in Fig. 5.8a. Capacitance contributions C_s and C_a are suppressed by connecting the grounding probes to the neighboring strips. Ground connection is provided by the shields of the LCR-meter terminals. These shields are internally connected to an input of an operational amplifier (virtual ground) and are kept at constant potential. Thus, any grounded electrodes will not affect the phase and amplitude of the probing AC signal, i.e., will not contribute to the measured capacitance. The drawbacks of the measurement method with grounding probes are that its quality depends on the active resistance connected to the virtual ground leading to an incomplete compensation of the capacitance. Apart from that, not all strips that do not participate in the measurement can be grounded. An assumption that the effect of the ungrounded strips is small leaves room for a systematic uncertainty.



(a) with grounding probes (b) without grounding probes

Figure 5.8: Schemes for capacitance measurement with (a) and without (b) grounding probes. Grounding probes are used to compensate for parasitic components in the measurement.

In this work, interstrip capacitance has been measured using a method without grounding probes [126]. Six different connection schemes implemented in the measurements and their corresponding measured capacitance contributions are shown in Fig. 5.9. Equivalent circuits of all schemes, except scheme #1, use parallel combination of capacitors that is preferable because electrostatic field in the detector is not localized inside of the separate capacitors and neighboring strips affect each other. Thus, in case of serial connection, individual conductors may distort the measurement results.

Interstrip capacitance can be measured via AC or DC-pads. In general case for an AC-coupled microstrip detector, there is a complicated capacitive network that consists of capacitance between metal strips, between strip implants, between metal of a given strip and implant of its neighbor as well as coupling capacitance. Due to the fact that coupling capacitance is much larger than the other capacitive components, its impedance vanishes in the frequency range of interest. As pointed out in [132], this condition simplifies the equivalent circuit between adjacent strips and has an important effect: capacitance measured via AC and DC-pads become equal. For convenience, measurements have been conducted via AC-pads.

Figure 5.10 shows examples of bias voltage dependence for capacitance measured according to scheme #1 and scheme #6. The corresponding values of capacitance

$$C_{scheme1} = C_s + 1/2C_b + 1/2C_a$$

$$C_{scheme6} = C_s + C_b + C_a$$

are dominated by the interstrip capacitance C_s and therefore should have close

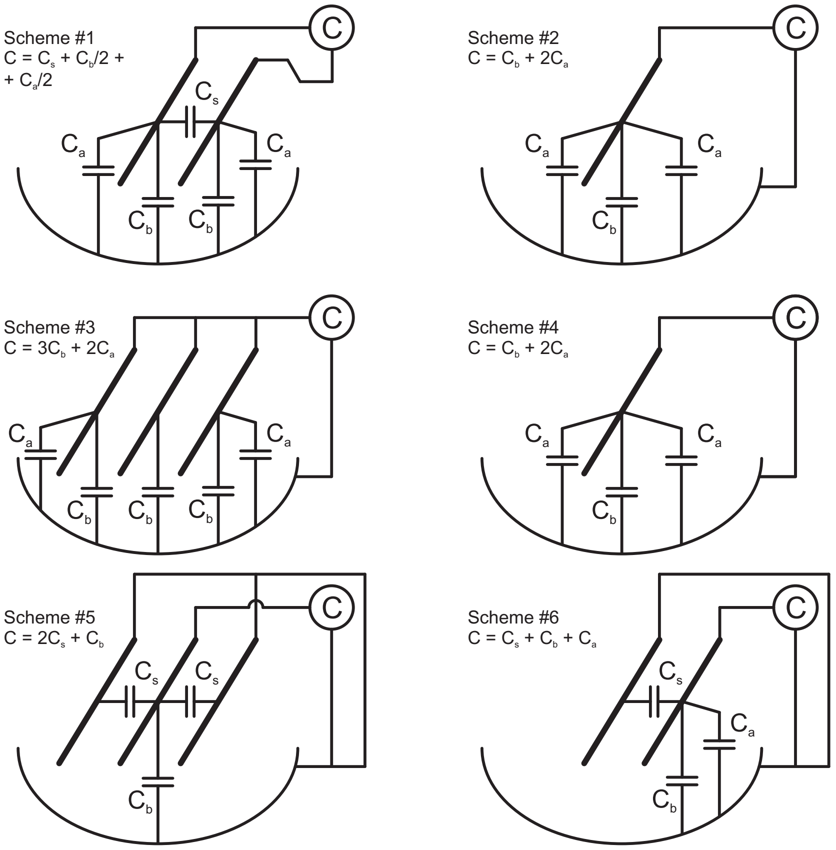


Figure 5.9: Measurement schemes used for determination of interstrip capacitance and its parasitic contributions.

values. Instead of this, values are different almost by a factor of 2. For this reason, scheme #1 has been excluded from the procedure of extracting the contributions C_s, C_b, C_a.

Results of the measurements are summarized in Table 5.1. Every scheme was measured on three different strips. Average values are shown in the table. Residual capacitance of the LCR-meter after calibration procedure that takes into account the effect of cables comprises $\sim 50\,\mathrm{fF}$.

Table 5.1 contains an overdefined system of equations for finding three values C_s, C_b, C_a. Spread of the values obtained from different equation sets served as an estimate of the measurement error. Described method gives the following values for capacitances per unit length:

$$C_s = 0.57 \pm 0.02\,\mathrm{pF/cm}$$

$$C_b = 0.11 \pm 0.04\,\mathrm{pF/cm}$$

$$C_a = 0.04 \pm 0.04\,\mathrm{pF/cm}$$

Extracted value for C_a is comparable with zero within the measurement error.

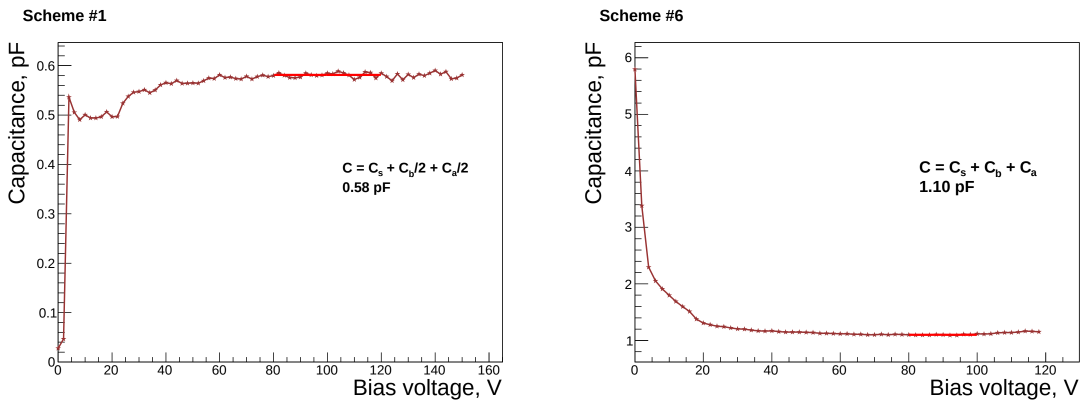


Figure 5.10: Measured capacitance vs. detector bias voltage for two connection schemes involving different parasitic components.

Scheme #	Equivalent scheme	C, pF
1	$C_s + C_b/2 + C_a/2$	0.58
2	$C_b + 2C_a$	0.24
3	$2C_b + 2C_a$	0.45
4	$3C_b + 2C_a$	0.62
5	$2C_s + C_b$	1.81
6	$C_s + C_b + C_a$	1.10

Table 5.1: Summary table for interstrip capacitance measurement.

Such a low value is not expected for microstrip detectors with a CBM02 type geometry (width-to-pith ratio $w/p = 0.36$) and requires further investigation.

Interstrip resistance

The interstrip resistance is a parameter that determines the integrity of a signal charge induced in a particular strip. Presence of finite interstrip resistance allows the charge to flow to the neighboring strips and leads to the signal reduction. Signal contribution that appear in the neighboring strips due to the charge transfer through the interstrip resistance should be distinguished from the one due to the *charge sharing* (physical signal caused by the ionizing particles and shared between several adjacent strips) and *crosstalk* (signal contribution that emerges at the transmission stage due to capacitive and inductive coupling). Apart from the interstrip resistance, the amount of charge that escapes from the strip depends on the shaping time of the preamplifier. Thus, for short shaping times the effect is less significant than for the long ones.

The interstrip resistance is usually different for the p and n-side of the sensors and additionally depends on the irradiation. Typical value of this parameter for a preirradiated sensor is of the order of GΩ. With irradiation, interstrip resistance decreases and, therefore, serves as one of the end of life criteria for microstrip sensors. for microstrip sensors. For this reason, knowing the dependence of the interstrip resistance R_{int} on the irradiation is necessary in order to predict the sensor performance according to the irradiation scenario.

Device connection scheme for the interstrip resistance measurement is shown in Fig. 5.11. Test voltage V_{test} is applied between adjacent strips in the range from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$ in steps of $0.1\,\mathrm{V}$. At the same time, detector under test is biased to the operating voltage (beyond full depletion). Interstrip resistance defined as

$$R_{int} = \Delta V_{test}/\Delta I$$

is extracted from the slope of the test voltage sweep. Not all sensors are suitable for the R_{int} measurement. Only sensors with strips biased via punch-through structures allow a correct measurement due to their effective bias resistance of $\sim$GΩ and higher. Alternatively, specially prepared polysilicon biased sensors with segmented bias rails [128] can be employed for the R_{int} measurement. An attempt to measure R_{int} for the normal sensor with polysilicon biasing results in a value that is equal to $2 \times R_{bias}$, where R_{bias} is a bias resistor value. Another important detail shown in the scheme is a ground connection of the two devices in order to provide a reference potential for the low-voltage power supply. In general case, LO terminal of the LV power supply should be connected to the bias rail of the side, on which R_{int} is being measured.

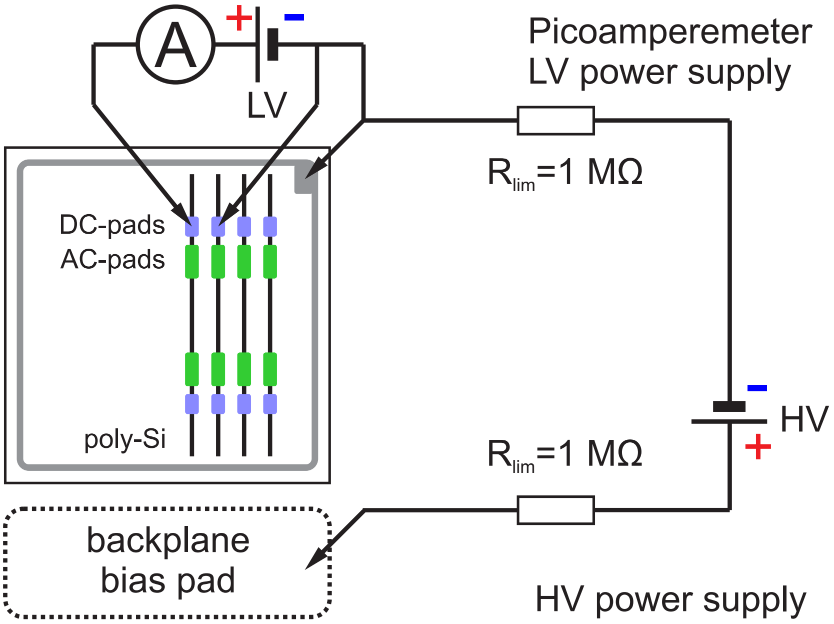


Figure 5.11: Connection scheme for interstrip resistance measurement.

Bias voltage dependence of the interstrip resistance measured on the ohmic side (n-side) of the sensor is shown in Fig. 5.12. For bias voltage below full depletion, R_{int} is low due to the presence of the free charge carriers in the undepleted bulk region. As the free charge carriers are removed at full depletion, R_{int} shows a steep increase. At bias voltages higher than V_{FD} interstrip resistance doesn't necessarily saturates at a constant value. As seen from the plot, at bias voltage of 70 V interstrip resistance increases to $\sim 200\,\mathrm{M}\Omega$, whereas V_{FD} for this particular sensor has been determined to be ~ 45 V.

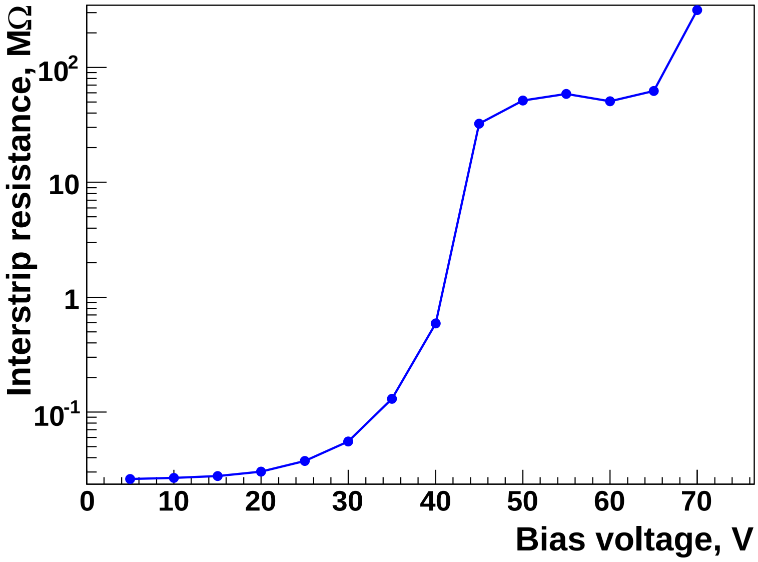


Figure 5.12: Interstrip resistance vs. bias voltage measured on the ohmic side of the sensor. At low bias voltages, resistance is determined by the free charge carriers present in the interstrip region. As the bias voltage reaches full depletion condition, interstrip resistance develops a steep rise up to several tens of MΩs.

For the junction side (p-side) of the sensor, proper interstrip isolation is reached already at low bias voltage (several Volts) and retains high value at higher bias voltages.

Coupling capacitor yield

Microstrip detectors often have integrated coupling capacitors in their surface in order to prevent the leakage current from flowing into the front-end chip. Readout in the AC-coupled mode increases the complexity of the sensor but on the other hand reduces complexity of the front-end chip that otherwise would have to include leakage current compensation circuit. Coupling capacitors need to have high dielectric strength (maximum electric field the dielectric material can withstand without breakdown), high capacitance value that largely exceeds parasitic capacitance contributions of the strip (e.g., interstrip, backplane etc.) and low dielectric leakage current. The requirement to have high dielectric strength is especially important in case of using grounded electronics when sensor bias voltage is applied across the capacitor. An electric short in a single channel that appears during the sensor operation may lead to a failure of the whole readout chip or even the detector module. In case floating electronics is used, this requirement is quite relaxed, except failure modes when capacitors have to endure up to half the bias voltage for a short time (i.e., beam splash accidents). This leads to the stringent requirements to the capacitor yield [127] according to which not more than a few percent of broken capacitors can be accepted. From the manufacturability point of view, complying with the requirement of high capacitor yield means that almost a defect-free dielectric layer has to be created and patterned over the area of 20–30 cm^2 which is a challenging task.

Measurement scheme for testing of the coupling capacitors is shown in Fig. 5.13. A fixed voltage difference of 10 V is applied to a DC and an AC-pad of a strip under test (thus to the plates of a capacitor formed by the metal strip and implant) and leakage current is measured by a picoamperemeter. The key element of the measurement scheme is a probe station that allows the probe needles to step through the pads of the strips in an automated fashion. Every time the voltage step is applied, picoamperemeter will measure the capacitor charge current that usually lasts up to a few seconds. That is why a measurement delay has to be introduced. After the delay, measured current drops below 1 nA, provided that a coupling capacitor under test has no defects.

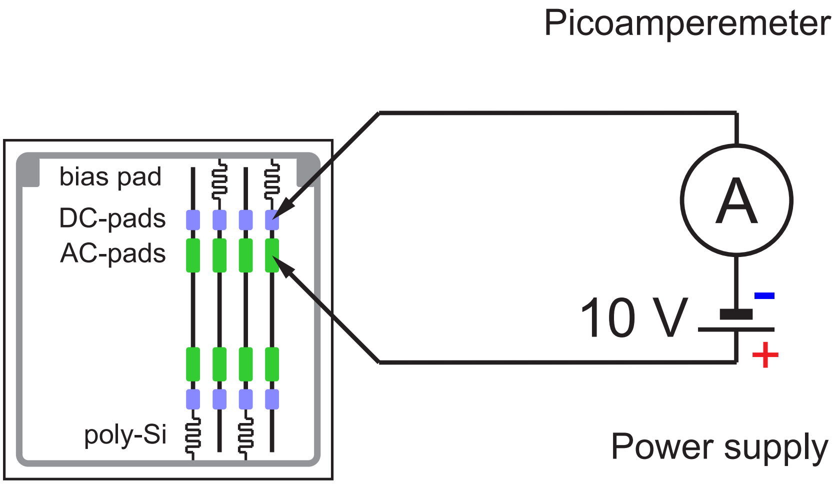


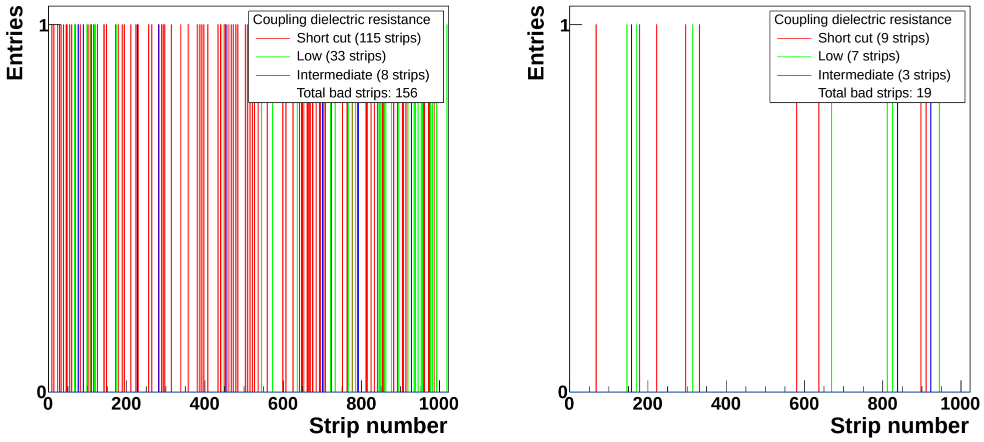
Figure 5.13: Connection scheme for determination of coupling capacitor yield (dielectric stress test).

Resistance of the defective capacitors with voltage applied across them may vary in a broad range: from relatively low resistance to electrical short cut (pinhole). In order to give an impression about the resistance of the dielectrics, measurements have been conventionally sorted into four groups:

- short cut: $I > 150\,\mu\mathrm{A}$
- low resistance: $10\,\mathrm{nA} < I < 150\,\mu\mathrm{A}$
- intermediate resistance: $1\,\mathrm{nA} < I < 10\,\mathrm{nA}$
- no defect: $I < 1\,\mathrm{nA}$

Results of the defect search in coupling capacitors of the CBM03 type sensor are shown in Fig. 5.14. The X-axis of the plots shows the strip number, found defects are color coded (see legend) and good strips are left blank. It can be seen that the *p*-side has a lot more defects than the *n*-side. On both sides, short cut is a dominant defect type. The reason for the observed situation might be in the failure during production at the stage of depositing the dielectric layers or further layers on top of them.

It is worth mentioning, that despite the visual effect produced by the figures, defective strips comprise 15.2% on the *p*-side and 1.9% on the *n*-side.



(a) *p*-side (b) *n*-side

Figure 5.14: Defect map of the coupling capacitance dielectric in CBM03 sensor (wafer #11). Insulation defects of different severity are marked with different colors. Any color means a defective channel.

More information about the defects can be obtained from the current-voltage scan of the coupling dielectric. Current measured in this way shows a weak dependence on the applied voltage until dielectric breakdown voltage V_{BD}^{AC} is reached. In case stacked dielectric is used to form coupling capacitors, the value of V_{BD}^{AC} may provide information on whether some particular layer is broken, both layers are broken or V_{BD}^{AC} corresponds to the design value based on the thickness of the layers and dielectric strength of the materials. Electrical reliability of the coupling capacitors produced out of stacked dielectrics of different types (oxide-oxide, oxide-nitride and oxide-nitride-oxide) is discussed in [129].

The problem of the coupling capacitor yield has been addressed in the sensor generation CBM03'. The proposed solution explored the options of thicker coupling dielectric layers as well as additional layers, e.g., polysilicon buffer layer and oxide-nitride-oxide (ONO) stacked dielectric. A batch of sensors with various combinations of the design parameters has been produced. The introduced changes resulted in an improved capacitor yield (better than 1% broken capacitors) for 50% of the sensors (i.e., parameter combinations). The successful combinations of the design parameters will be used in the further sensor prototypes.

Coupling capacitance

In order to provide a good coupling of signal to the readout electronics one needs to maximize the coupling capacitance of the strips which can be increased by reducing the thickness of dielectric material between a metal strip and a strip implant as much as the productions yield allows. Once generated in the bulk, the signal charge is divided between the preamplifier and parasitic capacitance. In order to make sure that sufficient fraction of the signal is collected by the preamplifier, the relation $C_{AC}/C_{int} > 10$, where C_{AC} is a strip coupling capacitance and C_{int} is an interstrip capacitance, has to be fulfilled. In order to ensure this, the value of the coupling capacitance has to be controlled on a few strips of several detectors form the batch.

A measurement scheme for the coupling capacitance is shown in Fig. 5.15. Terminals of the LCR-meter have been applied to the AC and DC-pads of a strip under test. The measurement is performed at different frequencies between 500 Hz and 500 kHz.

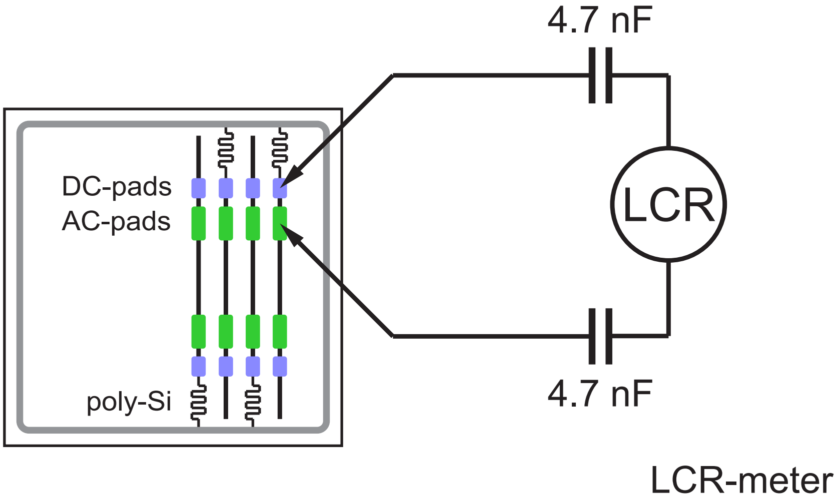
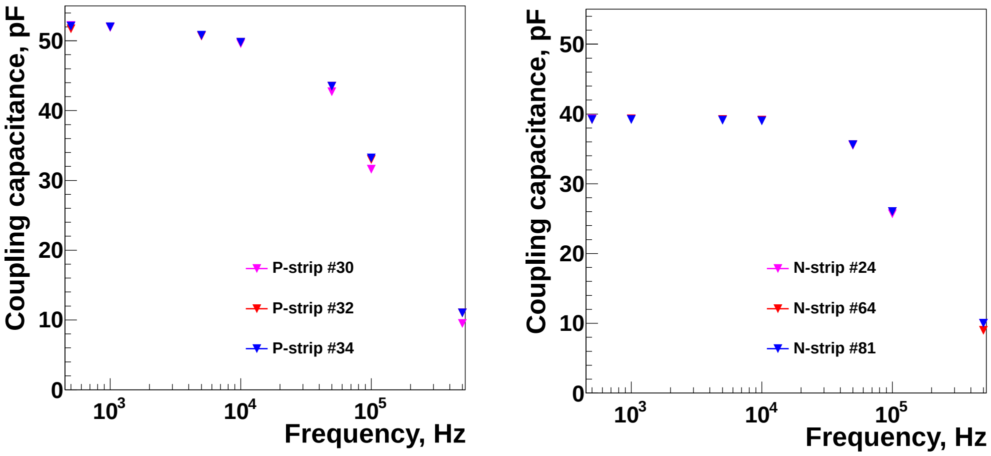


Figure 5.15: Connection scheme for coupling capacitance measurement.

The present method is prone to measurement errors, especially close to the boundaries of the frequency range of the device. The reason for this is a distributed resistance of the strip implant with typical values of 60 kΩ/cm for p^+-strips and

30 kΩ/cm for n^+-strips. As a result, coupling capacitance in the equivalent scheme is connected in series with implant resistance. Presence of this relatively high resistance reduces the quality factor of the scheme and leads to poor measurement accuracy. According to an alternative method described in [130] terminals of the capacitance meter are connected to an AC-pad of the strip under test and a bias pad of the backplane. In this scheme, capacitance meter measures a coupling capacitance and a backplane capacitance connected in series. In order to exclude the contribution of the backplane capacitance C_b detector has to be biased in forward direction to $\sim$1 V. Thus, the backplane contribution C_b becomes much higher than C_{AC} and their series combination is practically equal to C_{AC}. Since forward biased sensor conducts high current, the use of 1 MΩ limiting resistor ($R_{lim} = 1\,\mathrm{M}\Omega$) is advised.



(a) p-side (b) n-side

Figure 5.16: Coupling capacitance of 1.5 cm long strips of CBM04-FSD sensor as a function of frequency. Notice that coupling capacitance for the p- and n-side of the sensor are different by design.

Coupling capacitance measured as a function of frequency in several strips of a CBM04-FSD type sensor are shown in Fig. 5.16. Observed capacitance shows no significant frequency dependence below 10 kHz and falls off at higher frequencies. In [131], position of the knee in the frequency dependence of C_{AC} is related to the $R_{imp}C_{AC}$ time constant with C_{AC} being a coupling capacitance in the low-frequency limit and R_{imp} resistance of the strip implantation. The values that correspond to the plateau regions in Fig. 5.16 amount to $\sim$51 pF for the p-side and $\sim$39 pF for the n-side for the strip length of 1.5 cm or 34 pF/cm and 26 pF/cm for the p and the n-side respectively.

5.2 Performance of the front-end electronics

Characterization results for the n-XYTER chip are presented in this section. Some of the design flaws have been revealed and studied in depth in order to be addressed in the next production run. These include high temperature coefficient of the analogue baseline, layout related powering problems that cause baseline shift across the chip, non-linearity of the analogue response, etc.

5.2.1 ADC calibration

Characterization of the analogue response of the chip has become possible after acquiring a minimal set of hardware to complete the data acquisition chain and developing the necessary software. For this, an n-XYTER font-end board has been connected to a single-sided silicon microstrip detector [135]. Test sensor had DC-coupled strips with 10 mm length. Due to the strip pitch of 300 µm the probability of events with charge sharing between the neighboring strips was negligible. Signals have been generated in the sensor using a sealed ^{241}Am γ-source. Its spectrum contains several lines with the energy below 1 MIP signal deposited in 300 µm of silicon. This makes the source well suited for quantifying the analogue response of the chip in the most relevant part of the dynamic range.

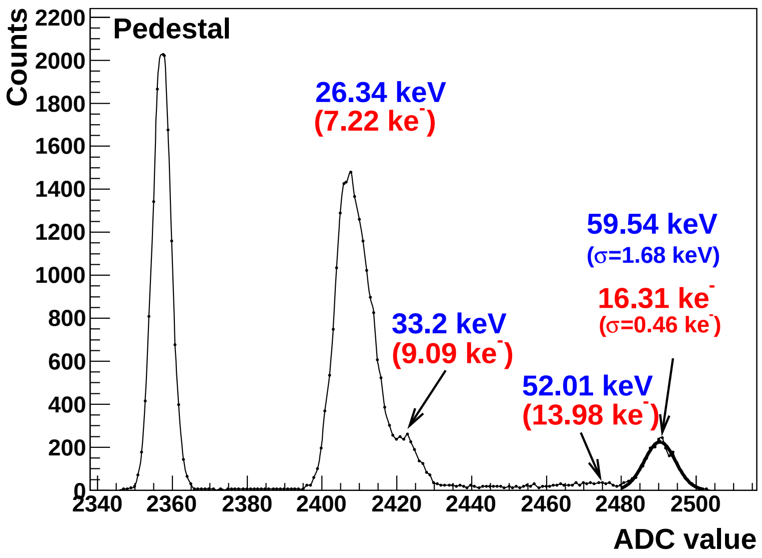


Figure 5.17: ^{241}Am gamma spectrum measured with the n-XYTER chip in self triggered mode on a 300 µm microstrip detector. Several characteristic lines are seen, the rightmost one corresponding to 59.5 keV. The fit of a Gaussian to it reveals a resolution of 460 e$^-$. The pedestal was added for reference through a random trigger in the n-XYTER test trigger mode, which may be employed for an alternative, triggered operation of the chip.

Figure 5.17 shows the measured spectrum with identified γ-lines marked on it. Four peaks have been identified with the strongest two being 26.3 keV (7.2 ke$^-$ in silicon) and 59.5 keV (16.3 ke$^-$ in silicon). The ENC noise of the system has been estimated from the width (sigma) of the peak with the highest energy and comprised 460 e$^-$ which is in agreement with simulation considering a detector capacitance on the order of 6 pF, but imprecisely known.

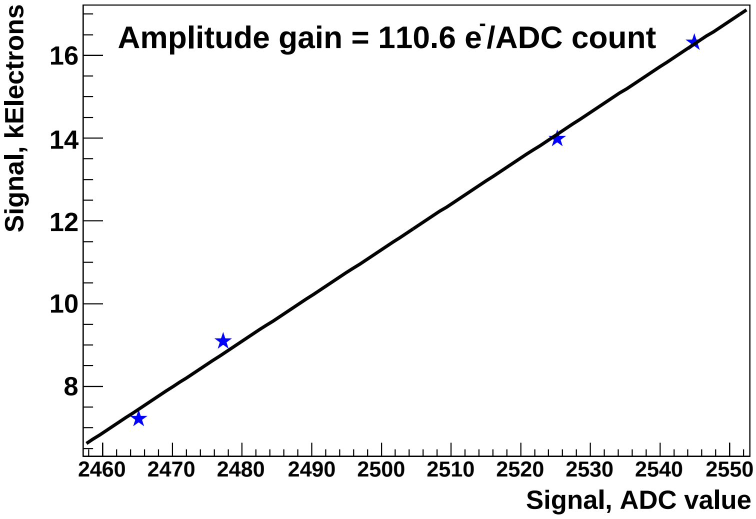


Figure 5.18: ADC calibration line. Slope of the line gives an ADC conversion gain of 110.6 e$^-$/ADC count.

The calibration line shown in Fig. 5.18 is derived from the peak positions of the γ-lines and their corresponding energy. The slope of the line fitted to the data points gives a conversion gain of 110.6 e$^-$/ADC count. The gain calibration procedure described here has been done under assumption of uniform conversion gain within the dynamic range. Using the obtained numbers charge collection efficiency (CCE) for an unirradiated sensor comprises only 60%. Later measurements have shown that energy gain dependence on the input charge has a structure, particularly around 1 MIP charge ($\sim$ 6.2 ke$^-$). More accurate calculation of signal in strip clusters with revisited gain calibration yielded 95% charge collection efficiency [136].

5.2.2 Dynamic range scan

In order to scan the dynamic range of the n-XYTER, signals of known amplitude have been passed through attenuation circuit and a known capacitance. Thus, calibrated voltage signals from a pulse generator have been converted into short current pulses with known charge. The amount of the charge ΔQ generated by a pulse edge with amplitude ΔV passed through a capacitance C equals

$$\Delta Q = C\Delta V$$

The major challenge of this method applied to the n-XYTER comes from the small amount of charge to be generated. Thus, generation of 1 fC charge requires to pass a 1 mV voltage step through a 1 pF capacitance connected in series. The output pulses with 1 V amplitude have been attenuated using external passive BNC attenuators by a factor of 1000 to produce pulses of the desired amplitude and preserve their initial signal-to-noise ratio. The small value of the capacitance was likely to be affected by parasitic contributions. With nominal value being 1 pF, the actual capacitance value of 1.2 pF has been measured with a precision LCR-meter.

The amplitude of the signals measured by the ADC versus corresponding signal charge is shown in Fig. 5.19. Signals with charge between 1.3 fC and 50.4 fC have been produced to scan the dynamic range. The range of amplitudes around 1 MIP signal has been scanned in fine steps. The dependence is linear up to about 35 fC and deviates from linear trend outside of the dynamic range.

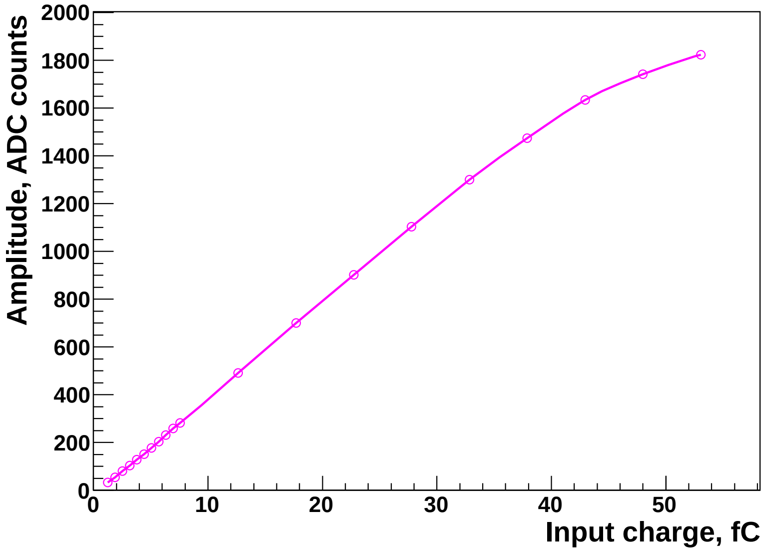


Figure 5.19: Amplitude of the peaks fed into the n-XYTER with a pulse generator versus their corresponding charge.

Derivative of the dependence shown in Fig. 5.19 gives analogue-to-digital conversion gain as a function of the input charge (see Fig. 5.20). In the interval 0–30 fC average value of conversion gain is 40.0 ADC counts per fC. However, strong non-uniformity is observed below 10 fC. This property of the chip may lead to incorrect amplitude determination, in particular when summing up the amplitudes in the strip cluster.

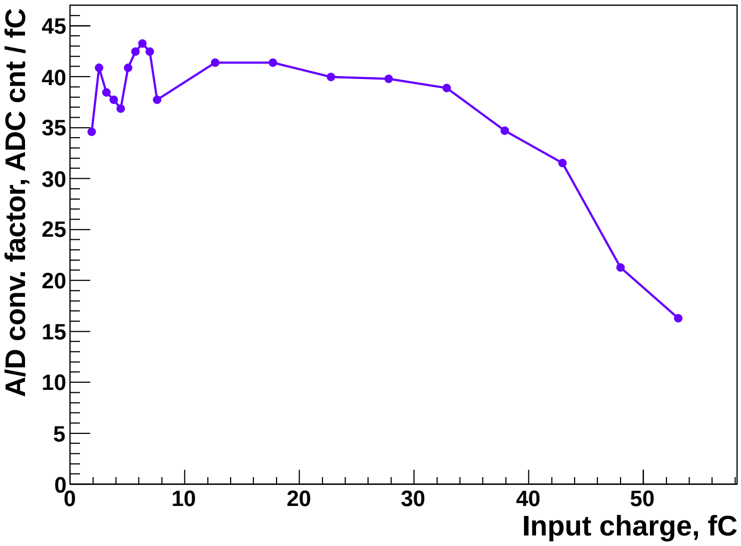


Figure 5.20: ADC conversion factor versus input charge. Strong inhomogeneity is observed in the region of 1 MIP charge (∼ 4 fC). Outside of the dynamic range (∼ 30 fC) conversion factor declines.

5.2.3 Global threshold calibration

Operation of front-end electronics with the lowest possible threshold is crucial for the physics performance of the STS, where sharing of the signal charge between several strips is observed and degradation of the signal-to-noise ratio is expected during the detector lifetime. As reported in [137], threshold value as low as 4 ke$^-$ may be required in order not to compromise the physics performance. Threshold calibration has been done to express the threshold level in units relevant for physics analysis – electrons (e$^-$) or femtocoulombs (fC).

The hardware setup with external pulse generator (see Sect. 5.2.2) was well suited for global threshold calibration. Several individual channels of the chip have been tested with calibrated charge pulses in the full threshold operating range up to about 10 fC. Threshold position was determined using the S-curve method where trigger efficiency is measured as a function of threshold level. Trigger efficiency is defined as the ratio of the discriminator trigger rate to the input signal rate. Point of 50% trigger efficiency allows to relate threshold level to the input charge.

The fast and slow branches of a channel in the n-XYTER chip are two parallel signal processing paths with different shaping times. The slow branch with long shaping time is optimized for accurate pulse height determination with low electronic noise. The fast branch with short shaping time is a time critical path optimized for generation of a trigger signal and pileup detection. In the fast branch noise manifests itself as spurious triggering activity and in the slow one as counts in the low-amplitude part of the spectrum. During the calibration, threshold S-curve scans have been performed for pulses of different amplitude, i.e., threshold response has been characterized using the information from the fast branch of the channel.

The measured dependence of the threshold position expressed in arbitrary Vth register units defined as a bending point of the S-curve is shown as a function of the input charge in Fig. 5.21. The dependence is linear in the region of interest (around 4 fC) with a slope of 21.2 Vth DAC register units per fC.

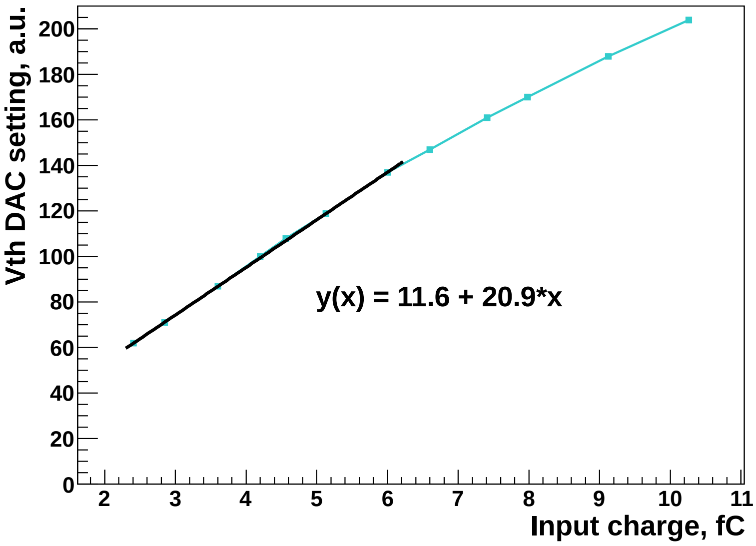
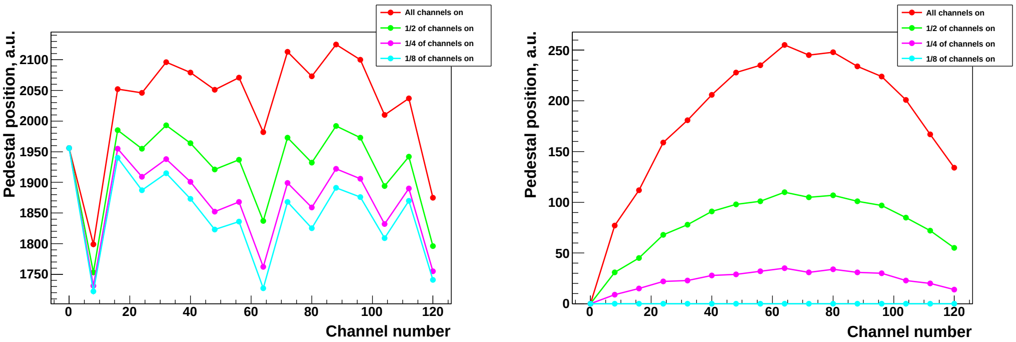


Figure 5.21: Threshold calibration line measured in the fast channel of the chip using the S-curve scans. Chip threshold setting is plotted versus input charge. For orientation: 1 fC ≈ 6.2 ke^-.

5.2.4 Pedestal position variation

Several defects identified during the work with the n-XYTER chip were observed in positions of the pedestals. This includes large channel-to-channel variations as well as a general trend of the pedestal positions over 128 channels of the chip. The latter problem was assumed to originate from the layout aspects of the chip and needed to be studied in detail. Particular suspicion fell on the power line for analogue part of the chip. The line had to be designed with small cross section due to space limitations in the chip layout, thus leading to high metal trace resistance. As a result, substantial voltage drop may develop when high current flows through the power line, e.g., at high triggering activity in the channels. Such a voltage drop that increases from the periphery of the chip towards the inner channels would lead to a corresponding shift of the channel pedestal positions.

The way to check the described hypothesis is to observe the pedestal positions in the channels of the chip in cases with different total power consumption. Power



(a) (b)

Figure 5.22: Pedestal profiles over the n-XYTER channels with various power consumption. Fraction of channel front-ends has been shut down thus reducing the chip power consumption. Raw pedestal profiles (a) and differences relative to the curves corresponding to the lowest power consumption at the lower power consumption (b) are shown.

consumption in the chip has been manipulated by shutting down part of the channels via shut-down bits in the control registers. Pedestal position profiles have been measured for four power consumption scenarios: with all channels on, with 1/2, 1/4 and 1/8 of the channels on. Measured profiles are shown in Fig. 5.22a. For convenience, all four profiles start from the same point. In the figure, power consumption increases from the bottom to the top, but due to high channel-to-channel variations it is hard to draw any certain conclusion on the pedestal profiles. To make the picture clear, relative differences of the pedestal positions are shown in Fig. 5.22b with respect to the profile with the lowest power consumption (in cyan). The figure allows to conclude that the “sag” in the pedestal positions profile clearly depends on the power consumption. Also, the highest deviation is reached for the central channels which proves the assumption of the design deficiency of the analogue power line.

The discovered flaw in the chip design has been reported to the chip development team and successfully eliminated in the engineering run.

5.2.5 Pedestal thermal drift

Stability of the n-XYTER parameters has been studied in a setup with several chips operated simultaneously [138]. In this configuration with the total power dissipation of 20 W, thermal stability of the electronics becomes an important issue and readout chips have to be cooled in order to keep the temperature reasonably low. The chips have been sandwiched between the cooling blocks with internal water circulation. Initially, due to periodic switching of the water chiller, temperature of the cooling blocks exhibited a sinusoidal time dependence with a period of ~ 20 minutes and amplitude of ~ 3 °C. Temperature of the cooling blocks recorded within a span of several periods is shown in Fig. 5.23. Observed temperature variation causes a drift of baseline in the read-out chip, revealing its high temperature coefficient. Fig. 5.24 shows time dependence of the baseline position as a result of temperature variation. The peak-to-peak amplitude of the baseline drift comprises about 200 ADC counts, exceeding the signal amplitude of a MIP particle. After this observation, the cooling system was exchanged with a more stable device – Lauda[4] RE 304 calibration thermostat. After thermal stabilization, variation of pedestal position has been reduced to 4 ADC counts (∼ 3 % of the MIP signal in 300 µm of silicon). High temperature coefficient of the front-end chip has been addressed in the n-XYTER engineering run and successfully eliminated.

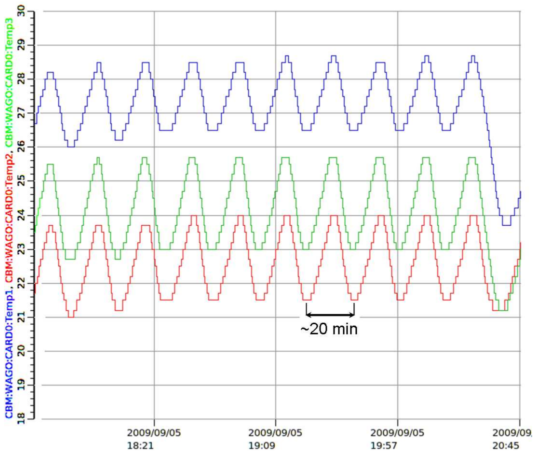


Figure 5.23: Thermal cycling of the n-XYTER chip due to periodic switching of the water chiller recorded during several periods.

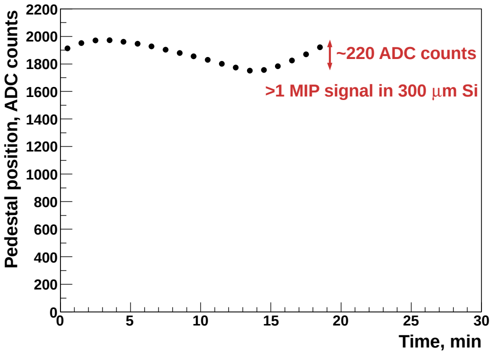


Figure 5.24: Sinusoidal drift of the baseline position in the chip related to the high temperature coefficient.

Characterization studies presented in this chapter have demonstrated expected performance of silicon microstrip sensors connected with a low-mass microcable to the n-XYTER readout chip. Quality assurance procedure for double-sided microstrip sensors have been developed both in hardware and software manner. Routines for measurement of the leakage current, total backplane capacitance, interstrip resistance and capacitance, coupling dielectric quality check, etc. have been automated.

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[4] http://www.lauda.de

Chapter 6

In-beam characterization of the STS prototypes

Testing of the prototype system components has started with a small proof-of-principle device [156]. Two detector boards with the CBM01 sensor were partially read out with two n-XYTER front-end boards. Sensors and front-end boards have been connected with a ribbon cable. Readout chain has been completed with a SysCore V2 readout controller for communication between front-end boards and DABC data acquisition system. The whole system has been commissioned using radioactive source. Amplitude spectra as well as correlations between equally oriented (i.e., vertically or horizontally) strips of the two stations have been obtained. Acquired data have been stored in binary list-mode data (LMD) files as well as in a format compatible with FairRoot analysis framework. The beam test has demonstrated operation of a full readout chain run in the self-triggered mode. An important outcome of the test was identification of the shortcomings, such as thermal stability of the system and stability of operation of the readout electronics available by that time.

6.1 Prototype reference tracking telescope

The first attempt to develop a reference tracking telescope started with a prototype tracking station featuring full readout of a $1.5 \times 1.5\,\mathrm{cm}^2$ sensor with front-end electronics integrated on the board. A compact object of $10 \times 10\,\mathrm{cm}^2$ size placed between the cooling plates comprised a beam tracking station – a constituent part of a reference tracking telescope.

The reference tracking telescope consisting of three stations based on the double-sided silicon microstrip detectors has been constructed and tested in a 2 GeV proton beam experiment in “Cave C” experimental site at GSI, Darmstadt. This proof-of-principle device designed for charged particle track measurement with high spatial resolution closely integrates silicon sensors with self-triggering front-end electronics. Each station features the full double-sided readout of a CBM02B2 prototype sensor with 2×256 strips of orthogonal orientation and 50 µm strip pitch (see Fig. 6.1). Four self-triggering n-XYTER readout chips have been directly wire bonded to the detector. A tracking station is realized on an 8-layer printed circuit board. The detector is glued into a squared opening in the board resting on a machined-in balcony structure of about 100 µm width. Two chips read out one detector side. The 10 cm by 10 cm board also houses an external ADC and DC power converters. The beam tracker board is connected to a CBM readout controller with two high-density flat/twisted-pair cables. The detector bias is provided through a coaxial cable.

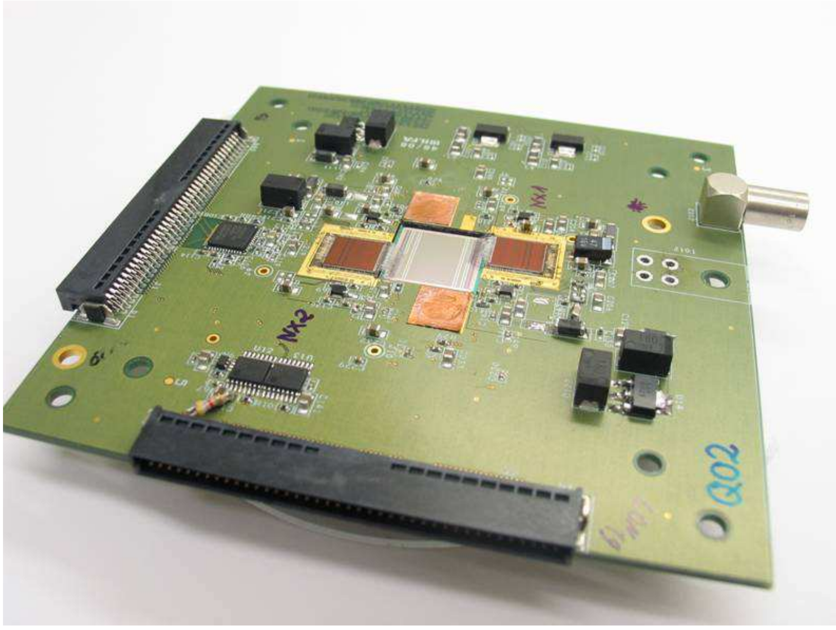


Figure 6.1: A beam tracker board comprising a double-sided CBM02B2 prototype detector wire-bonded to four n-XYTER readout chips, two per side.

The four readout chips dissipate up to 20 W. The tracker board has therefore to be cooled so as to avoid excessive temperature of the chips and silicon sensor that would result in an unstable operation, high leakage current and noise, particularly in a limited space like in an experimental setup. On the tracker board, the readout chips are brought into a thermal contact with a copper inlay reaching to the back side of the board. The board is then sandwiched between two aluminum plates with built-in water cooling pipes as shown in Fig. 6.2. A compact object is created.

Advanced tools have been developed for offline analysis. As a first step, the raw binary data files have been converted to the ROOT files. After conversion, ROOT files are compatible with the current STS digitization and STS hit finding algorithm, developed for the simulation of the full CBM setup. The hit finding tools include charge sharing between neighboring strips, which provide position resolution better than 15 µm [157]. As an example of reconstruction of the hit distribution, the beam profile reconstructed in one of the detector stations is shown in Fig. 6.3.

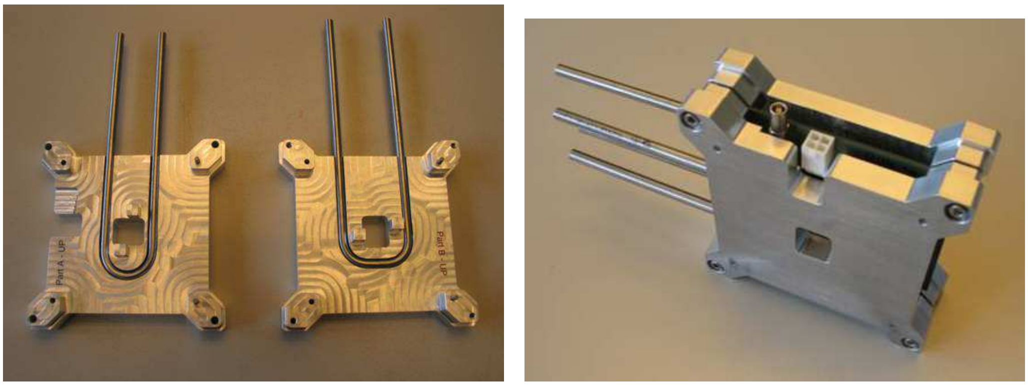


Figure 6.2: Tracker board mounted between cooling plates.

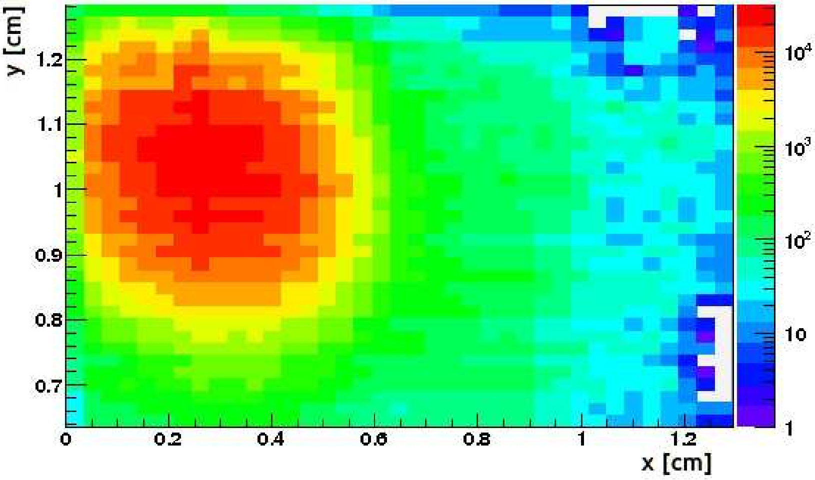


Figure 6.3: Beam spot reconstructed in a tracker board.

Development and commissioning of the beam tracker boards has been impeded by a number of issues. Among them are cooling that required a precision thermostat and manufacturing complexity of a multilayer printed circuit board with high density interconnects and production yield issues related to it. These aspect have affected the stability of operation during the beam test. Thus, despite the measured beam spot, no reasonable amplitude response could be obtained due to the lack of thermal stability.

An important outcome of testing the tracking telescope in the beam was a full-fledged test of the system that demonstrated operation of the whole data acquisition chain including double-sided microstrip sensors, thermally significant amount of the front-end chips, readout controller with chip specific firmware as well as online monitoring tools for primary evaluation of the setup performance.

6.2 Next generation of the prototype tracking telescope

Experience with the first prototype tracking telescope resulted in changes in the next telescope design. As learnt from the telescope operation, microstrip sensor to be integrated into a printed circuit board of a tracking module has to pass the quality assurance criteria and remain functional during routine operation and maintenance. Since silicon sensor is wire bonded to the PCB, its replacement in case of damage or poor performance is not feasible in practical terms. That is why the second prototype telescope has been developed with a modular design. Complexity of components integration within a tracking station is avoided by separating a detector board from readout electronics. A station in this case consists of individual modules with separated services, e.g., low/high voltage, water cooling, etc. Thus, a telescope station is created with flexible design featuring replaceable electronics and sensor thermally decoupled from the heat sources (readout chips).

A tracking station comprises double-sided silicon microstrip detectors, ultra-thin readout cables, and self-triggering readout electronics (see Fig. 6.4). The detectors SPID-CBM02 (see Sect. 4.3.1) originate from a cooperation with CiS, Erfurt, and have 256 orthogonal strips per side with 50 µm strip pitch. The detectors were integrated into the carrier boards at SE SRTIIE, Kharkov, Ukraine [158]. A detector board is a combination of a rigid carrier structure with a flexible board on top of it. Flexible board is made of aluminized Kapton (polyimide film). Aluminum traces are connected to the sensor pads using ultrasonic TAB bonding. The contact areas are additionally glued with a two-component epoxy for bond protection. The front-end boards developed at GSI based on the self-triggering n-XYTER chip are described in detail in Sect. 4.4.2. Double-sided readout has been implemented using floating electronics, so as to exclude the high voltage being applied across the coupling capacitors. That is why for safety reasons, readout controllers have been enclosed into isolated metal cages.

For thermal stability, aluminum blocks attached to the front-end boards are cooled with water and kept under constant temperature. Digital and high-voltage lines may be a source of noise for the front-end inputs due to signal pickup from digital lines or electromagnetic interference coming from the mains. Therefore, high-voltage line for sensor bias and digital lines for the n-XYTER data and control (FEB-ROC cable) have been shielded.

The prototype Silicon Tracking System consisting of two stations has been tested in the beam in December 2010 along with other CBM prototype detector systems [159]. The test was focused on characterization of individual components and their fine tuning. The activities included noise optimization, study of the amplitude response and development of the online monitoring tools.

After testing of individual tracking stations the setup was ready to be extended to three stations and to include tracking information from the other detector systems and beam monitors.

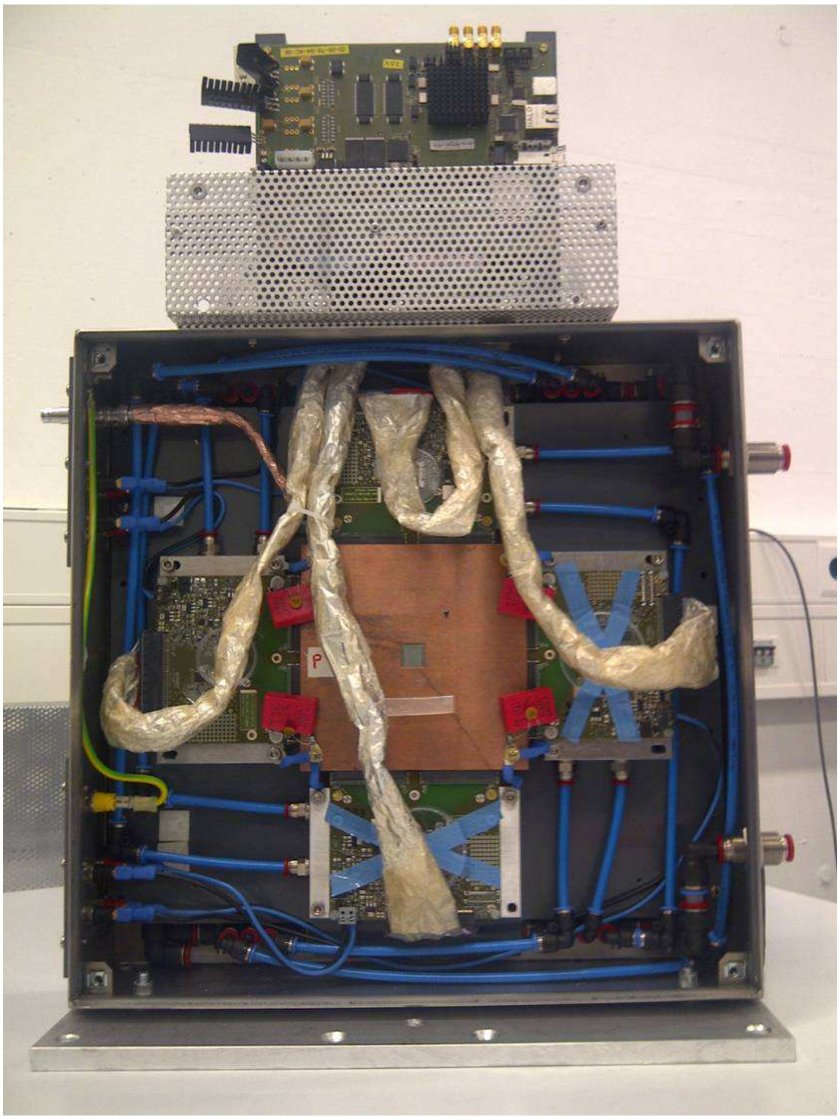


Figure 6.4: Prototype tracking station with detector board and readout electronics. Readout controllers are mounted on top.

6.3 Beam test at COSY, Jülich in January 2012

The beam test of January 2012 took place at COSY storage ring in Forschungszentrum Jülich, Germany. Silicon Tracking System and readout electronics have been tested in a 3 GeV/c proton beam. Present test was dedicated to the study signal formation in the irradiated FSD prototype detectors. Since telescope configuration included three stations, it was possible to do the particle tracking after incorporating information from the other detector systems under test.

Apart form the explicit goal of radiation tolerance assessment of silicon sensors, the use of new strip isolation technique on the *n*-side of the FSD sensors required thorough validation and thus called for a beam test. The main observables for this are charge collection efficiency and cluster shape as a function of neutron fluence. The sensors have been irradiated with fast neutrons at research reactor facility in Ljubljana, Slovenia and stored at $-20\,^{\circ}\mathrm{C}$ temperature afterwards. During integration into detector modules and operation in the beam, sensors have been kept at room temperature. Prepared detector boards with irradiated sensors are shown in Fig. 6.5. The samples have accumulated fluence between $10^{12}\,\mathrm{n_{eq}/cm^2}$ and $10^{14}\,\mathrm{n_{eq}/cm^2}$ – values representative for the CBM irradiation scenario. One of the samples was non-irradiated to provide reference for the measurements.

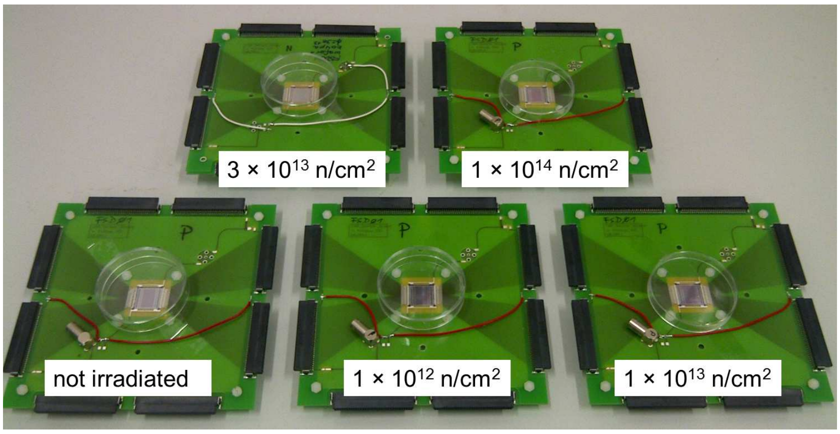


Figure 6.5: Detector boards with irradiated FSD01 sensors. Charge collection efficiency and cluster properties are to be studied as a function of fluence and incident angle.

The experimental area "Jessica" was equipped with infrastructure from GSI, shown in Fig. 6.6, foreseeing the forthcoming CBM in-beam tests there on a regular basis. Two stations (STS1 and STS3) equipped with previously tested CBM02 sensors were movable along the beam. The middle station (STS2) comprised one of the several detector boards with irradiated FSD01 sensors and was additionally rotatable, thus enabling the beam incidence angle scan. The detector boards with irradiated sensors have been exchanged during the test to allow measuring sensor properties as a function of neutron fluence. In order to provide additional reference points for tracking, hit information from two fibre hodoscopes has been included into analysis. Information from the neighboring systems under test such as a gas electron multiplier (GEM) detector and a paddle scintillator was available for analysis and could be used optionally.

By implementing proper shielding and grounding techniques, the electronic noise was reduced to about $600\,\mathrm{e}^-$, which is dominated by the preamplifier noise. The n-XYTER temperature was stabilized with water cooling, which abated the problem of the baseline drift significantly. In addition, an automatic baseline calibration was implemented in the data acquisition software and run between the beam spills. A detector control application based on the EPICS [161] framework

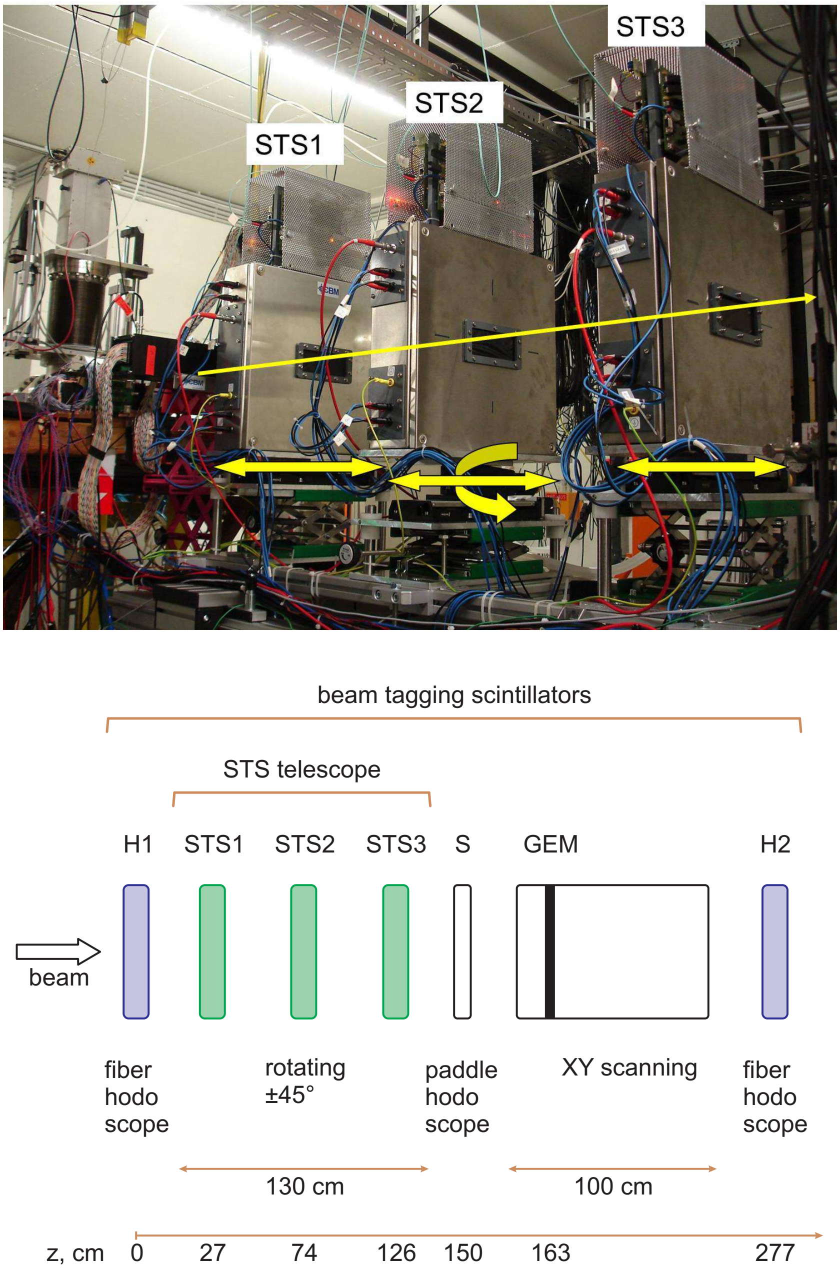


Figure 6.6: Beam tracking telescope (above) consisting of three stations and beam hodoscopes (one of the hodoscopes is seen in front of the STS1 mounted on the scissors lift). Stations STS1 and STS3 are built with reference detectors with studied properties. Detector under test is integrated into station STS2. Layout of the beam test setup (below) is shown with indicated positions of the tracking stations, beam hodoscopes and GEM detector setup tested in parallel.

was developed and ran on a dedicated PC. All the auxiliary hardware, including power supplies, stepping motors and the beam monitoring detectors, water cooling units and temperature sensors were operated and monitored remotely. Some of the measured process variables (STS bias voltages, positions of the stations, temperatures) were periodically inserted into the data stream to study the detector response as a function of those values and to allow for temperature and high-voltage corrections in the on-line and off-line data analyses.

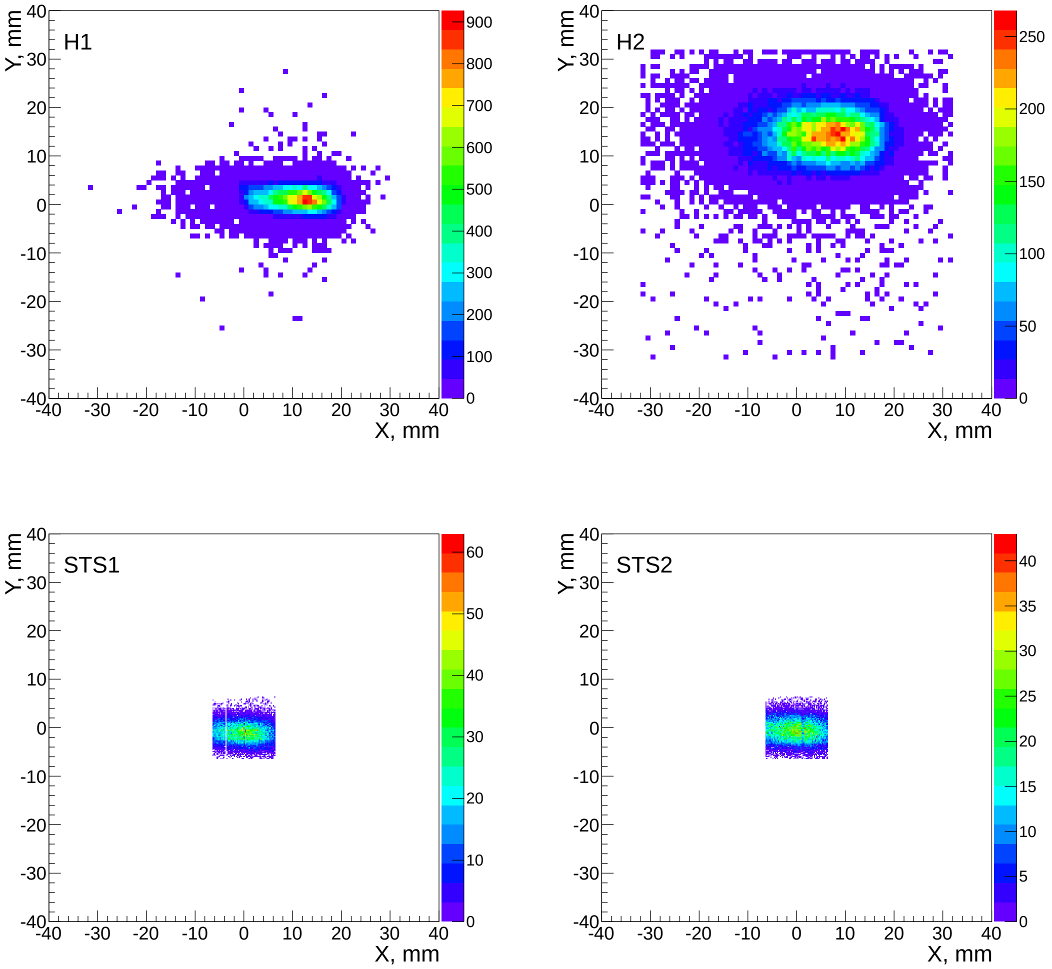


Figure 6.7: Beam spots as measured by the scintillation hodoscopes (above) and two reference tracking stations (below). The spots in the hodoscopes are bigger due to larger fiducial volume.

Test beam data yield inter alia two-dimensional beam profiles. Figure 6.7 shows beam spots as measured by the fibre hodoscopes and two tracking stations (station labels are in the figures). Transverse size of the beam spots in the STS stations is limited by the sensor size $1.5 \times 1.5\,\mathrm{cm}^2$ that is much smaller than that of the hodoscope $6.4 \times 6.4\,\mathrm{cm}^2$. Difference in sizes of the beam spots in the hodoscopes illustrates beam divergence enhanced by multiple scattering in the the upstream detectors. In particular, size of the beam spot in hodoscope H2 is affected by a massive GEM station standing in front of it. Hit positions shown in histograms are associated with tracks as opposed to hits measured by individual stations.

Test of the detector systems in the beam was compromised by the accelerator operation in the first days. After a maintenance period that preceded the beam test, accelerator went into operation with improper settings. This caused spontaneous horizontal movement of the beam by up to several centimeters. Monitoring of the beam hit positions as a function of time reveals unstable beam conditions. Beam hit coordinates in one of the hodoscopes measured during several spills are shown in Fig. 6.8. The beam position in the Y-coordinate remained unchanged during the operation, whereas instabilities have been observed along the X-coordinate.

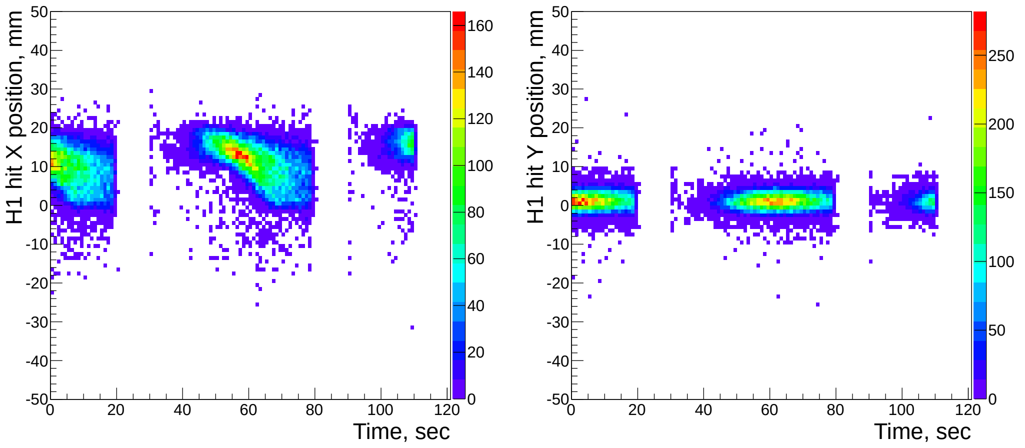
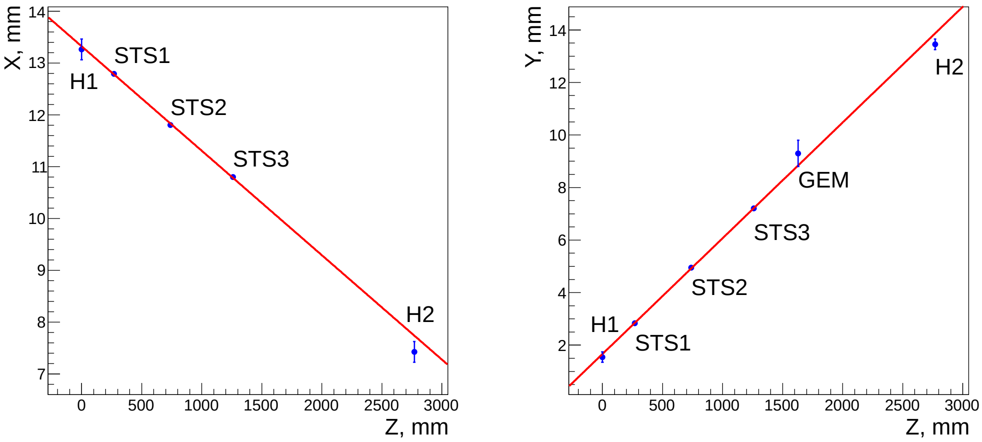


Figure 6.8: Beam spot position in X and Y projection as a function of time. The beam was unstable and showed horizontal oscillations within spills.

The discovered problem in the accelerator operation has been reported and solved after clearing the quadrupole magnet failure, so the beam test could proceed in normal mode.

Data analysis in the Go4 framework included elements of the tracking software from the CbmROOT analysis framework that is used for offline simulations and physics performance evaluation. Tracking has been implemented using information from three STS stations and two beam hodoscopes. Occasionally, hit information form the GEM detector has been used. With moderate beam intensities and without magnetic field the problem of tracking is essentially reduced to the linear fit problem. For simplicity, track finding criterion required a single hit in all stations and hodoscopes. Examples of the obtained straight tracks in X and Y-projections are shown in Fig. 6.9. Shown projections belong to different tracks, therefore the left figure (6.9a) is missing a hit that belongs to the GEM detector. Error bars assigned to the hit positions reflect the intrinsic resolution of the detectors. Since channel pitch for the fibre hodoscopes largely exceeds that of the silicon microstrip detectors (1 mm vs. 50 µm), error bars associated with STS stations are much smaller than the error bars for hodoscopes. Alignment procedure and evaluation of position resolution for individual tracking stations are described in the next section 6.4.



(a) XZ-projection (b) YZ-projection

Figure 6.9: Projections of the tracks reconstructed in the setup consisting of three tracking stations, two scintillation hodoscopes and GEM detector.

6.4 Beam setup alignment and tracking

Tracking stations have been aligned along the beam based on the assumption of straight tracks. For a 2.5 GeV proton beam and reasonable amount of material in the beam, this assumption may be considered realistic. Straight charged particle tracks create spatially and temporally correlated signals in the detector planes. For a misaligned detector setup, spacial correlation is broken. Therefore timing constraint on the detector hits has to be applied. Selection of hits within a certain time window with respect to a low noise reference signal (beam tagging scintillator) serves as a track finding criterion and allows to reduce the number of spurious hits for identified tracks.

Initially, errors of the track hit positions are taken large due to misalignment. As soon as tracking information is available, further step towards reducing the coordinate errors is done by calculating the track residuals – difference between the assumed hit position and the one obtained from the track fit. Ideally this value has to be around zero. In practice, distribution of residuals has a Gaussian shape peaking around the offset coordinate. Offsets measured in this way may be removed by the mechanical adjustment of the sensor positions, however they are commonly taken into account in the data analysis software.

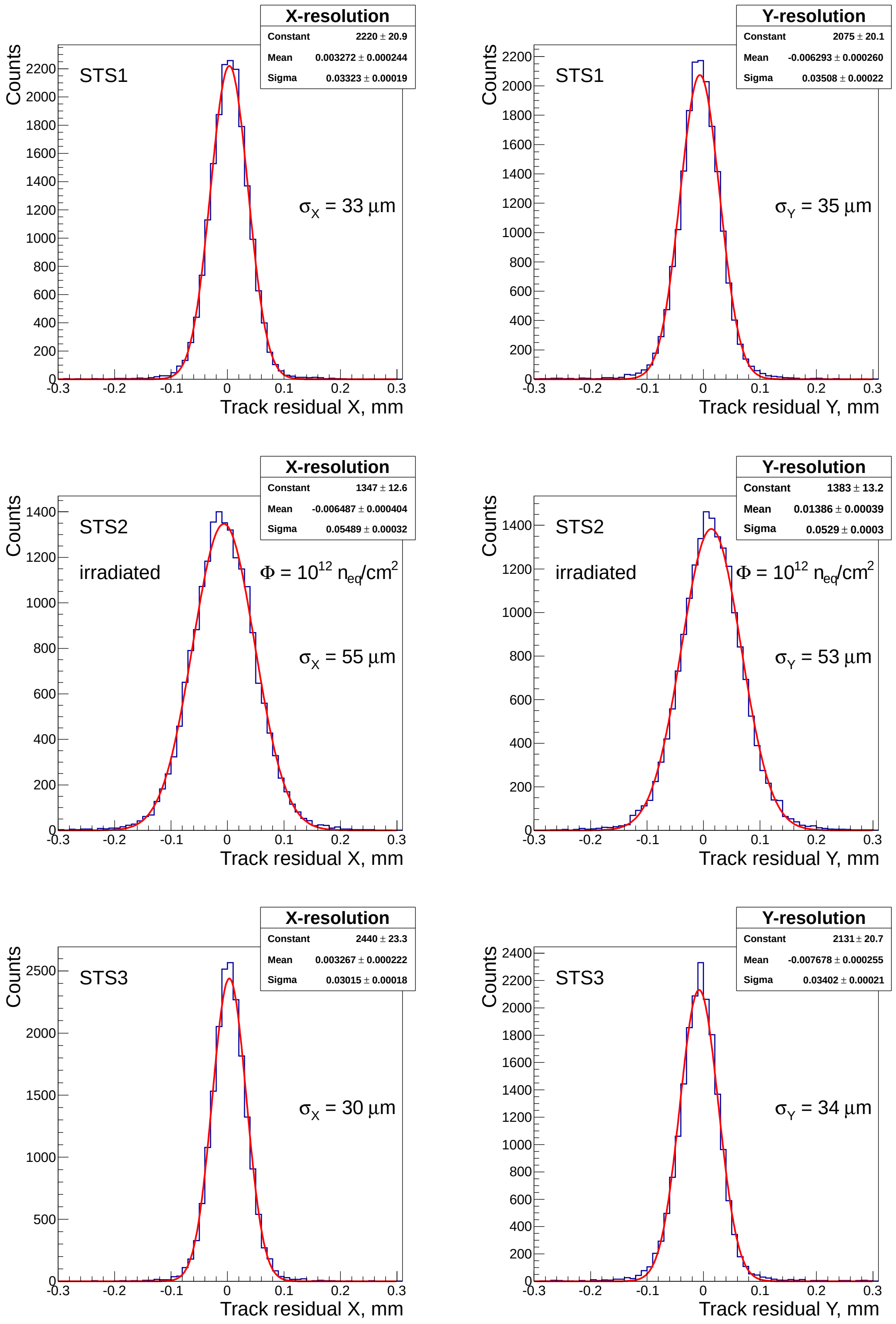


Figure 6.10: Track residuals for X (left) and Y-coordinates (right) measured by the STS stations after removing the offsets with respect to the beam position in the analysis software. Width of the distributions is attributed to the intrinsic resolution of the detector and track fitting precision (minor contribution). Fit parameters indicate worse resolution for the irradiated detector.

Residual plots for the X and Y-coordinates of the first STS station are shown in Fig. 6.10.

After finding the hits associated with a track, the alignment procedure for the STS stations relied on the coordinates measured by the beam hodoscopes. A straight line is drawn through the space points in two hodoscopes and residuals are calculated for the three STS stations. In the next iteration space points in the STS can be taken as a reference to align the hodoscopes. Intrinsic resolution of the hodoscopes obtained in this way was $\sim 220\,\mu m$. Track residuals for the stations STS1 and STS3 show position resolution of 30–35 µm that is approaching the intrinsic resolution of the sensors. Irradiated sensor in STS2 station shows worse position resolution of about 50–55 µm for a sensor with accumulated fluence of 1×10^{12} 1-MeV n_{eq}/cm^2.

The alignment quality may be visualized and verified by plotting the two-dimensional correlation plots. In the case shown in Fig. 6.11a, horizontal position in station STS1 is plotted against horizontal position in station STS3. Similar distribution is presented for the vertical strips (Y-coordinates). The distributions have been obtained after software alignment. That is why both of them are located on the diagonal of the plot. The length of the distribution along the diagonal is attributed to the beam size, in case beam spot size is smaller than the sensor. Locus length for the X-coordinates (Fig 6.11a) is much greater along the diagonal then the locus for Y-coordinates. This observation is related to the shape of the beam spot.

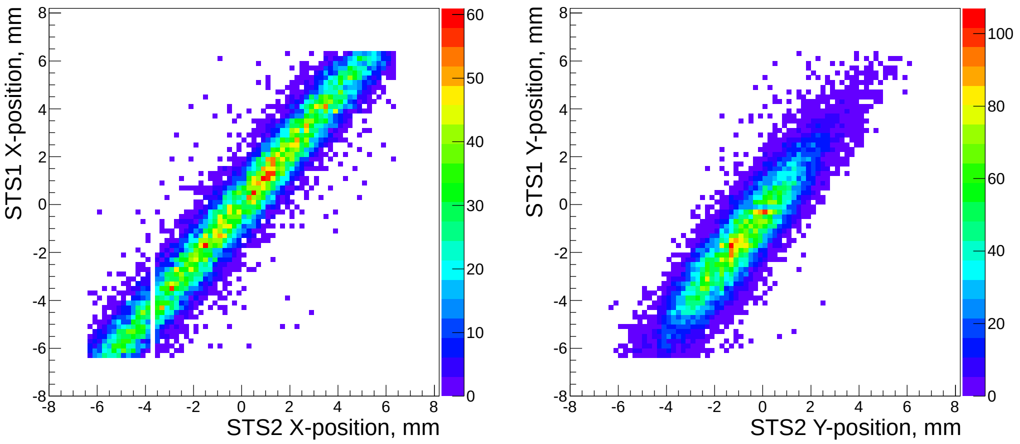


Figure 6.11: Correlation between horizontal (left) and vertical (right) strips in the stations STS1 and STS2. The vertical blank stripe in the left figure indicates a dead channel.

6.5 Analogue performance of the prototype detector modules

Amplitude response defines the lifetime a microstrip detector module and quality of the delivered data. Due radiation damage accumulated during the experiment operation, signal measured by a silicon detector degrades due to a reduction of the charge collection efficiency and noise increases due to the increase of leakage current. This leads a reduction of the signal-to-noise ratio. For an operational module, S/N ratio has to be above 10. One of the goals for the beam test, was to study the analogue response in order to measure the charge collection efficiency and the signal-to-noise ratio. Noise has been estimated for the detector modules composed of the n-XYTER frontend electronics, analogue microcables and sensors of different length in [162].

For the STS2 station of the tracking telescope, amplitude response has been studied in the triggered mode. This method allows to trace the signal down to the lowest amplitudes and estimate noise in the slow channel of the readout chip. Obtained amplitude spectra are shown in Fig. 6.12. High amplitudes correspond to the signal from a charged particle. Low amplitudes result from the baseline sampling forced by a trigger signal. Trigger signal is derived form the beam hodoscopes.

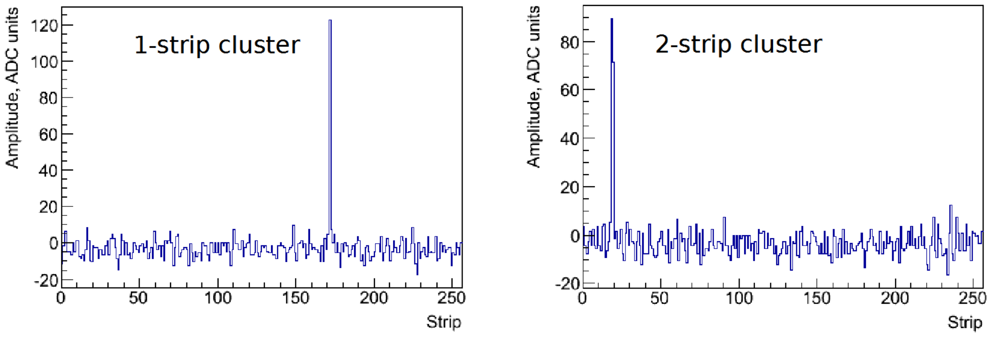


Figure 6.12: Examples of 1-strip and 2-strip cluster event measured by detector in triggered mode. The amplitude as a function of channel number is shown in 256 sensor channels. In case of a 2-strip cluster, signal amplitude is shared between two neighboring channels.

Signal charge that is spread between several strips creates a hit clusters. For a given channel within cluster, signal sharing means reduction of signal-to-noise ratio. On the other hand, with analogue readout hit position resolution can be improved by using cluster amplitude information as opposed to binary readout, where precision is given by the channel pitch:

$$\sigma_X = \frac{pitch}{\sqrt{12}}. \tag{6.1}$$

The effect of digital and analogue readout on the position resolution and efficiency of the silicon microstrip detectors are elaborated in [163].

Hit clustering information has been extracted from the amplitude distributions. A cluster is defined as a group of hits correlated in space and time (hits in the neighboring channels that appear within a time window of 50 ns). The aim of the study was to quantify the collected signal charge and to study the width of the signal clusters as a function of the beam incidence angle. The amplitude spectra for single-hit clusters are shown in Fig. 6.13 for the p- and n-side of the sensor. The signal generated by a MIP particle traversing the detector volume is proportional to the deposited energy. For thin absorbers, energy deposited by minimum ionizing particles varies according to the Landau–Vavilov distribution with asymmetric shape. Apart form that, the measured charge experiences additional Gaussian fluctuations due to the electronic noise and fluctuation of the number of charge pairs. The Gaussian smearing results in a minor broadening of the distribution and shift of the most probable value (MPV), i.e, the peak position.

After the data analysis, clustering information has been extracted that allowed to quantify the collected signal charge. The amplitude distributions for single-hit clusters as measured on the p- and n-side are shown in Fig. 6.13. The distributions have been fitted with Landau-Gaussian convolution to extract the MPV values. Obtained peak positions correspond to the collected charge of $22.6 \pm 2.3\,\mathrm{ke}^-$ and $21.6 \pm 2.2\,\mathrm{ke}^-$ for the p- and n-side, respectively. The expected amount of charge is $22.8\,\mathrm{ke}^-$ that comes from the specific energy loss of 80 electron-hole pairs per µm in silicon for a MIP and the sensor thickness of 285 µm.

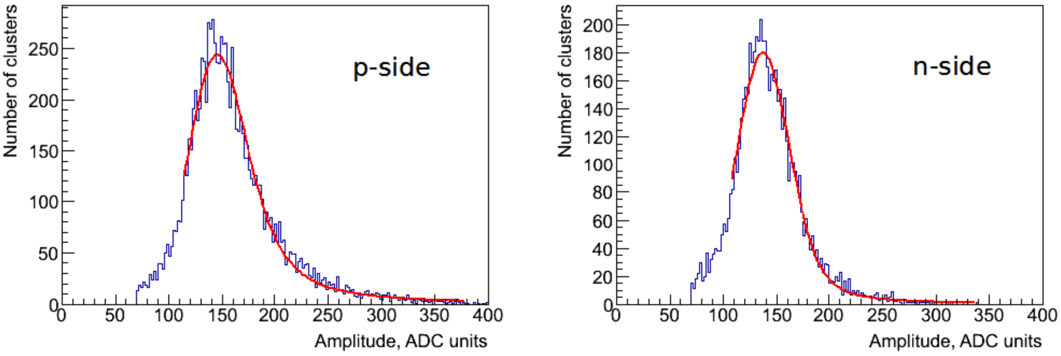
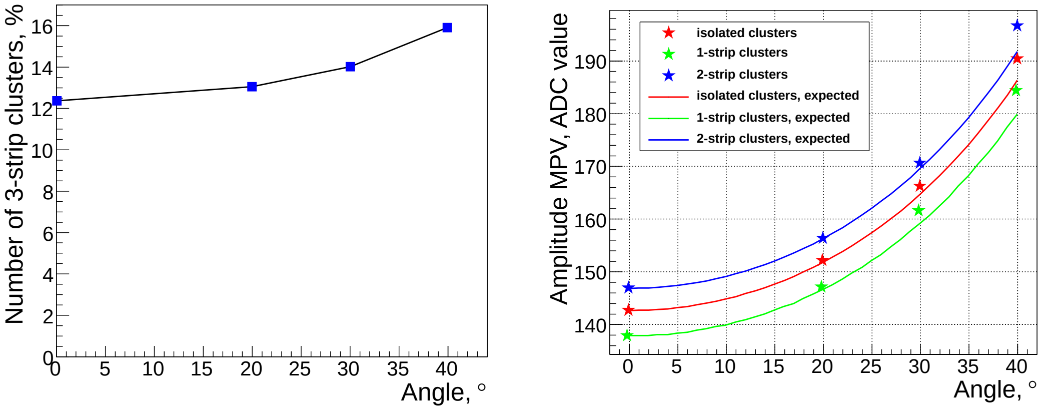


Figure 6.13: Amplitude distributions for single-hit clusters measured on the p and n-side of the sensor. The fit function is Landau-Gaussian convolution.

The cluster size distribution is important to estimate how much the signal is shared between the neighboring channels. During the beam test, particles have hit the sensors under approximately normal incidence angle. This condition doesn't favour the charge sharing as opposed to the measurement of inclined tracks. Thus, most of the hits produced single-hit clusters.



(a)

(b)

Figure 6.14: Beam incidence angle scan for the STS2 station: (a) percentage of 3-strip clusters and (b) total cluster amplitude.

In order to estimate the effect of the track incidence angle on the charge sharing, the percentage of the 3-strip clusters has been estimated (see Fig. 6.14a). As the tracking station changes its orientation form the normal one to 40° with respect to the beam axis, the percentage of the 3-strip clusters changes from 12% to about 16%. Inclined tracks effectively traverse thicker layer of the detector material. This leads to an increase of the cluster amplitude. In Fig. 6.14b, the MPV of the amplitude distributions for 1-strip and 2-strip clusters is shown. Clusters labeled as isolated, have been reconstructed with a threshold condition on the neighboring strips in order to exclude the effect of highly asymmetric charge sharing. Theoretical curves show the amplitude dependence expected from the amount of material traversed by the beam particles. Also, it can be seen that the total amplitude in the 2-strip clusters is systematically higher than that of 1-strip clusters, whereas the amplitude of the isolated clusters has intermediate values.

6.6 Online monitoring and slow control

Detector and readout hardware development for the experiment requires testing of individual components (e.g., for new hardware revisions) as well as performance evaluation of the whole prototype data acquisition chain from a detector to data storage. Apart from hardware, analysis procedures and data acquisition process itself need to be tested and monitored. Online monitoring software compatible with the CBM prototype data acquisition chain has to fulfill the following functions:

- select events of interest, e.g., by filtering the DAQ messages with respect to a time window around reference message (beam tag)
- display detector specific information (hit geometry, correlations, tracking)

- provide fast online monitoring, interactive analysis tuning

Software used in the beam test consisted of two parts for data acquisition and online monitoring. Data acquisition backbone core (DABC) [164] is a universal modular DAQ system developed at GSI, Darmstadt to provide a common tool for typical data acquisition tasks such as event building, data transport and connectivity to external applications. It is compatible with various front-ends and suited for high-throughput distributed event building networks. Online monitoring tool Go4 [165] is an object oriented analysis framework based on ROOT with graphical user interface based on Qt library (Nokia). Go4 provides services and interfaces for the user-written analysis code and can be run in a batch mode (compiled or interpreted) as well as in an interactive mode, both online and offline.

The mostly used, interactive mode offers the following key features:

- a non-blocking graphical user interface (GUI) to control and steer the analysis
- live monitoring (asynchronous graphics update from the analysis)
- adding user-specific GUIs using “Qt designer” tool

The software framework has found extensive application during the beam test with experimental setup consisting of several detector prototypes in the same beam line and various DAQ hardware components. Different detector groups contributed to the collaborative software development with detector specific analyses.

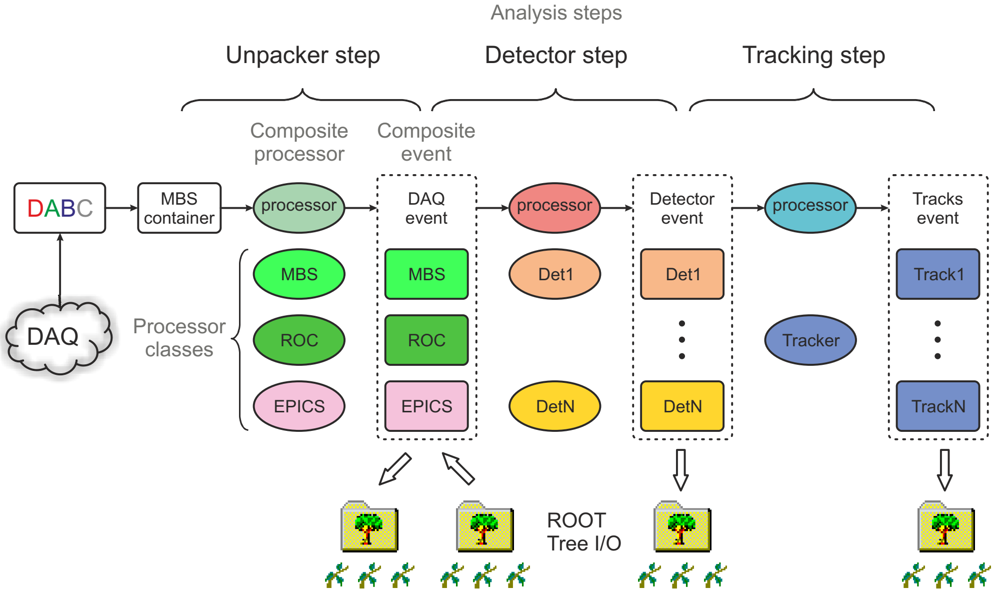
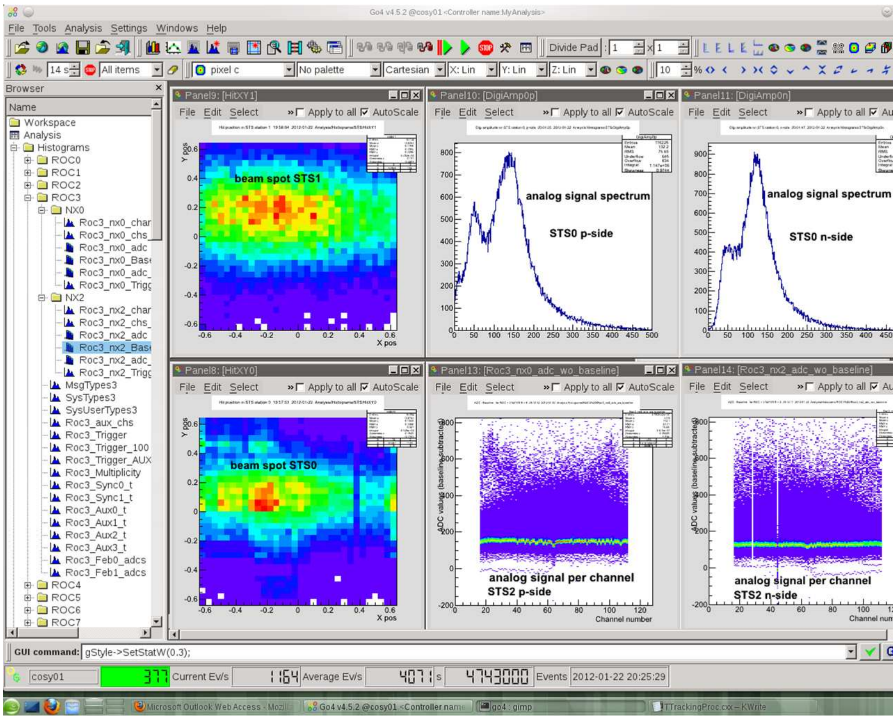


Figure 6.15: Analysis structure implemented in the Go4 monitoring tool. Data processing is subdivided into steps. Event and processor classes are implemented for every step.

Software analysis structure used for the CBM beam tests is shown in Fig. 6.15. Subsequent data generations are separated into analysis steps. Every step produces a data structure (output event) that serves as an input for the next step in the analysis chain. Event processors are implemented by a user and contain data processing code. Composite event processors combine a code for individual front-ends or detector systems.

The CBM beam test software consists of three steps. The "Unpacker" step accepts data from DABC combined from different sources and transmitted in generic data containers that are adopted from the legacy Multi Branch System (MBS) [166] framework. Typical data sources are readout controllers, MBS-based trigger system or EPICS slow control system. In the "Detector" step, system-specific histograms are filled for the STS, GEM and hodoscope subsystems, signal clustering information is extracted and channel mapping is applied. In the final step, spatial and temporal correlations between different stations are calculated. Tracking procedure is applied to the identified correlated space points. Trajectory fits provide alignment information and allow to estimate a spacial resolution of individual detector stations.



GUI command: `gStyle->SetStatW(0.3);`

cosy01 377 Current Ev/s 1164 Average Ev/s 4071 s 4743000 Events 2012-01-22 20:25:29

Figure 6.16: Go4 monitor graphical user interface. Individual analyses and sets of histograms are available for different detectors taking part in the beam test.

The Go4 graphical user interface (GUI) is shown in Fig. 6.16. It offers a convenient way to browse the data structures filled during the analysis. Visualized results can be updated asynchronously or with a given time period. The GUI contains results of all steps and for all components of the beam setup. Conditions, i.e., cuts can be applied to the histograms, thus implementing event an selection. Interface screenshot shows beam spot in two STS stations as well as amplitude spectra measured on both sides of the sensor in the first station.

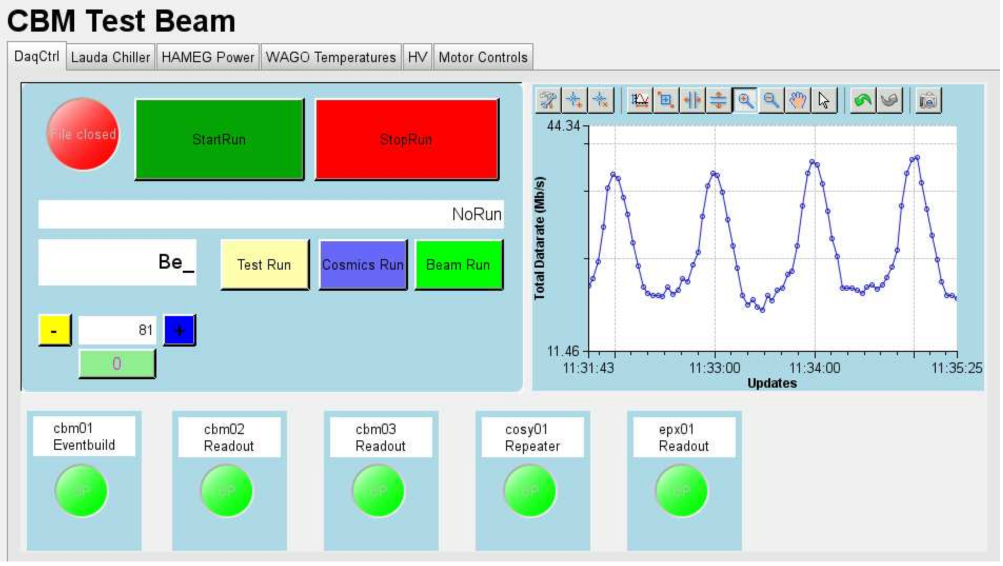


Figure 6.17: EPICS slow control interface. Upper left graph shows variation of data rate correlated with beam spill structure.

Another important component of the test beam software is slow control. EPICS framework, designed for building distributed control systems to operate devices, was used to control the detectors and infrastructure hardware. Visualization has been implemented using the Control System Studio [167].

EPICS graphical user interface (see Fig. 6.17) integrates tools for run control, temperature sensing as well as steering high/low voltage power supplies, step motors and cooling system. In order to be able to correlate detector data to slow control events (e.g., for position, voltage or temperature scans) EPICS data are included into the DAQ data stream and are available for online and offline analysis.

Beam tests described in this chapter and performed on a 2.5 GeV proton beam, have demonstrated feasibility of the module concept and operation of the detector modules within specifications.

Chapter 7

Summary and outlook

Within this work, a prototype of the STS detector module has been evaluated including sensors, readout microcables, front-end electronics and preliminary support structure. The module is conceived as an ultra-light support structure that holds the silicon sensors, microcables and front-end electronics. Minimal material budget between $0.3\%X_0$ and $1.0\%X_0$ is strived for in order to provide track momentum measurement with precision $\delta p/p \sim 1\%$. Methods have been developed to assess the parameters of the module components. The prototypes of silicon microstrip sensors and self-triggering front-end electronics have been used for the construction of the detector modules. The modules have been employed for the space-point measurement and track reconstruction in the beam test.

According to the physics goals described in Sect. 4.1, requirements to the components of the detector module have been formulated. Silicon microstrip sensors with radiation hard design provide double-sided readout with strips oriented at stereo angle of $\pm 7.5°$. Additional metallization layer has been introduced to interconnect the short corner strips such that a given sensor side can be read out from one edge only. Test of the irradiated sensors has demonstrated the radiation tolerance up to $3 \times 10^{13}\,\mathrm{n_{eq}/cm^2}$.

Multilayer microcable prototype with aluminium traces and polyimide base has been manufactured with material budget of about $0.1\%X_0$ and effective channel pitch of 58 µm matching that of the current sensor design (see Sect. 4.5). The cable was designed to minimize material budget as well as noise contributions from trace capacitance and series resistance. The cable prototypes have been used for construction of a demonstrator module and tested in the beam.

The n-XYTER readout chip (see Sect. 4.4.1) used in the prototyping phase featured a self-triggering architecture and shaping times of 18.5 ns and 139 ns for fast and slow channel, respectively.

Carbon fibre has been chosen as a material for the module support structure. A low mass support structure has been designed and produced to hold up to 5 detector modules.

One of the main objectives of this work was the development of quality assurance procedures for the double-sided silicon microstrip sensors. For this, a test stand for sensor characterization has been created. Measurement setup includes hardware (electrometers and an LCR-meter) and LabVIEW-based software. Routines for the most of the required measurements have been developed, e.g., leakage current, total backplane capacitance, interstrip resistance and capacitance, coupling dielectric quality check, etc.

Characterization has been done for 4 sensor modifications, 1 n-XYTER readout chip modification and 3 front-end board modifications based on it. Development of several sensor generations was based on the performance characterization and implementation of the radiation tolerant design features as well as the sensor geometry optimized for the ladder-type detector modules. Iterations in the front-end board production were necessary to achieve a stable production quality and analogue response. Measurements include electrical characterization of the sensors, readout chip calibration and detector module readout tests with radioactive sources and proton beams. Experience with different modifications of front-end boards and results of testing have been taken into account in the subsequent modifications.

The final assessment of the system has been done by estimating the tracking performance of the detector modules. Beam tests conducted on a 2.5 GeV proton beam have demonstrated operation of the detector modules within specifications. This means that the aim of the work has been achieved.

After the assessment of the very first prototype components, definition of the module concept can be started. The assessment of the design concept for the detector modules and overall system was outside of the scope of this work. The activities on system integration are now starting. They will address cooling and powering of the detector modules and stations, design of the beam pipe in the STS region and its integration with the Micro Vertex Detector inside of the magnet.

The project timeline includes writing of the technical design report (TRD) by the end of 2012 as the first milestone. The appendices to the TDR the are to be finished in 2013. The production and quality assurance of the STS components is scheduled for 2015-2016. The construction of the CBM experiment is expected in 2017-2018.

Zusammenfassung

Motivation

Das Compressed Baryonic Matter Experiment (CBM), des zukünftigen Beschleunigeranlage FAIR, ist ein Fix-Target-Experiment, mit dem Ziel der Erforschung der Eigenschaften von stark wechselwirkender Materie, erzeugt in den Kollisionen der Schwerionen bei ultrarelativistischen Energien. Der Zustand dieser nuklearen Materie wird in einem Phasendiagramm mit Bezug auf Temperatur und Nettobaryonendichte dargestellt. Ergänzend zu den Physik-Programmen der Experimente am RHIC (BNL) und LHC (CERN), werden bei CBM die Messungen im Bereich moderater Temperaturen und höchster Nettobaryondichten durchgeführt.

Ein Betrieb bei Strahlenergien von 10–45 AGeV wird die Untersuchung des Bereichs des Phasendiagramms, in dem der Phasenübergang von Quark-Gluon-Plasma zu hadronischer Materie vorhergesagt wird, ermöglichen. Die Aufgabe besteht darin, Hadronen und Leptonen, darunter seltene Sonden wie Open-Charm-Teilchen und Leptonenpaare, mit hoher Statistik und Präzision zu messen. Dafür müssen die Ereignisse von physikalischem Interesse in Kern-Kern-Kollisionen mit Multiplizitäten von rund 1000 geladener Teilchen pro Kollision bei der Reaktionsrate von bis zu 10 MHz selektiert werden. Solche Messungen erfordern einen schnellen und strahlungsharten Detektor zum Auslesen durch eine selbstgetriggerte Elektronik. Das freilaufende Datenaufnahmesystem mit hohem Durchsatz wird die volle Online-Rekonstruktion und Selektion der Ereignisse bieten.

Die zentrale Komponente des Experiments – Silicon Tracking System (STS) – wird für die Spurenrekonstruktion und Impulsmessung von geladenen Teilchen in einem Magnetfeld entwickelt. Das System, bestehend aus acht Tracking-Stationen basiert auf doppelseitigen Silizium-Mikrostreifendetektoren, wird sich in der öffnung eines Dipolmagneten mit 1 T Feld befinden um für Tracking der geladenen Teilchen mit Impulsauflösung von etwa 1% zu sorgen. Die wichtigsten Voraussetzungen dafür sind hohe Ortsauflösung in der Größenordnung von 10 µm, sowie ein niedriges Materialbudget um die Mehrfachstreuung zu minimieren. Ein Betrieb bei hohen Interaktionraten und großen Teilchenmultiplizitäten erfordert strahlungstolerante Mikrostrieifensensoren und Front-End-Elektronik mit adäquaten Auslesezeiten.

Der Schwerpunkt dieser Arbeit lag in der Entwicklung von Prototyp-Komponenten für das STS und deren Integration. Ein Detektor-Modul ist eine grundlegende funktionelle Einheit, die einen Sensor, Analogmikrokabel und Front-End-Elektronik, montiert auf einer Trägerstruktur, umfasst. Diese Prototyp-Komponenten mussten charakterisiert werden, um ihre Eignung für die Konstruktion eines Detektormoduls aufgrund der gewünschten Physikleistung des Systems und der Anforderungen eines langfristigen Betriebs festzustellen. Dafür wurden Studien bezüglich Qualitätssicherung und analoger Signaleigenschaften von Sensoren, Kalibrierung selbstgetriggerter Front-End-Elektronik und Systemintegrationsaspekte durchgeführt. Dieses Modulkonzept musste durch den Bau eines Demonstrators sowie der Auswertung seiner Leistung mit radioaktiven Quellen und Beschleunigerstrahlen validiert werden.

Entwicklung der Prototypkomponenten

Das STS-Stationen müssen modular aufgebaut sein, es werden dort einzelne Detektormodule in Leitern kombiniert. Eine Reihe von Leitern ergibt eine Station. Das Layout der STS wurde, bezüglich der Anzahl von Tracking Stationen, deren Positionen und Granularität, für eine effiziente Spurrekonstruktion optimiert. Für eine hohe Impulsauflösung sorgt das minimierte Materialbudget der Station. Um die Serienfertigung der Leiter und die Wartung des Systems zu vereinfachen, wurde die Anzahl der verschiedenen Leiter-Typen minimiert. Das STS, ausgestattet mit doppelseitigen Silizium-Mikrostreifen-Sensoren, wurde auf Tragstrukturen aus Kohlenstofffaser mit sehr geringer Masse sowie hoher mechanischer Stabilität montiert. Das Auslesen dieser Sensoren erfolgt über Front-End-Elektronik, welche sich außerhalb der Detektorakzeptanz befindet, verbunden durch dünne mehrlagige flache Mikrokabel. Um sich dem Endsystem nähern zu können, muss nachgewiesen werden, dass die wichtigsten Spezifikationen durch Prototypkomponenten erreichbar sind. Für die Anschließende Integration dieser Komponenten zu einem Detektorsystem und dessen Betrieb in einem Strahl muss das Konzept eines Detektormoduls validiert werden.

Somit konnte das Mikrostreifen-Sensorlayout, kompatibel mit der Modulstruktur, hergestellt werden. Dies beinhaltet die Ausrichtung der Streifen an einem Stereowinkel und der Umsetzung der doppelten Metallisierung um die Sensorauslesung von nur einer Kante zu ermöglichen. Die weiteren Anforderungen sind das Materialbudget von $0.3\% X_0$, das Erreichen einer Anzahl der guten Kanäle von mehr als 98% sowie einer Strahlungshärte die mindestens $10^{14}\,\mathrm{n_{eq}/cm^2}$ ergibt. Die Verwendung von Mikrokabeln mit bis zu 60 cm Länge erfordert eine Optimierung der Kabelgeometrie, um das Rauschen, assoziiert mit Kapazität und Serienwiderstand der Signalspuren, zu minimieren. Außerdem musste die Durchführbarkeit eines TAB Bonden für ein solches Kabel getestet werden. Die wichtigsten Anforderungen an den Prototyp der Ausleseelektronik waren: der selbstgetriggerte sowie geräuscharme Betrieb.

Doppelseitige Silizium-Mikrostreifensensoren

Die doppelseitigen Silizium-Mikrostreifendetektoren wurden als Sensortechnologie für den STS, aufgrund der Kombination einer guten Ortsauflösung, einer zweidimensionalen (projektiven) Koordinatenmessung mit geringem Materialbudget ($0.3\% X_0$), der hohen Auslesegeschwindigkeit und ausreichender Strahlungstoleranz gewählt. Mehrere Generationen von doppelseitigen Silizium-Mikrostreifendetektoren wurden zur Untersuchung strahlenharter Konstruktionsmerkmale und des Konzepts, eines großflächigen Sensors und dessen Kompatibilität mit der Leiter-Struktur des Detektormoduls, hergestellt. Insbesondere wurden Sensoren mit 1024 Kanälen pro Seite, einem Pitch von 58 µm sowie einer aktiven Fläche von $62 \times 62\,\mathrm{mm}^2$ produziert. Doppelmetallschichten auf beiden Seiten des Sensors werden verwendet, um die kurzen Eckstreifen miteinander zu verbinden, die aufgrund der Orientierung der Streifen unter einem Stereowinkel von ±7.5° entstehen. Die elektrische Charakterisierung der Sensoren wurde durchgeführt, um die gesamte Bedienbarkeit sowie die Extrahierung der Geräteparameter feststellen zu können. Hierfür wurden unterschiedliche Kontaktflächen (Pads) mit feinen Nadeln untersucht, welche an die Messausrüstung für Strom, Spannung oder Kapazitätsmessung angeschlossen wurden. Im Rahmen der Sensorcharakterisierung wurden Gesammtsensoreigenschaften (z.B. Stromspannung, Kapazitätsspannung) sowie Intersteifen-Parameter gemessen. Das gleiche Hardware-Setup, eingesetzt auf einer halbautomatischen Probestation, ermöglichte die Bestimmung der Anzahl guter Kanäle beim Durchlaufen aller Pads.

Front-End-Elektronik

Das Auslesen der Sensoren wurde mithilfe einer selbsgetriggerten Front-End-Elektronik getätigt, bei der kein externer Trigger erforderlich ist. Eine Front-End-Board wurde auf der Grundlage eines n-XYTER-Auslesechips mit datengesteuerter Architektur entwickelt, der geeignet ist bei der Ausleserate von 32 MHz betrieben werden zu können. Die Chip-Architektur verfügt über schnelle und langsame Kanalzweige, um sowohl präzises Timing als auch Amplitude über ankommende Signale liefern zu können. Die Kanalauslesung wird gemäß dem Token-Ring-Prinzip durchgeführt, welches ein reduziertes Datenvolumen und eine effiziente Nutzung der verfügbaren Bandbreite ermöglicht. Die Front-End-Board enthält einen externen Analog-zu-Digital-Wandler (ADC). Die Kalibrierung des ADC wurde unter Verwendung von sowohl ^{241}Am Röntgenquelle als auch eines externen Impulsgenerators vorgenommen. Die Schwellenkalibrierung und Untersuchung der Temperaturabhängigkeit der Chip-Parameter wurden durchgeführt. Nach Stabilisierung der Betriebstemperatur des Chips durch Wasserkühlung wurde die Variation der elektronischen Basisline (Pedestal) in den Auslesekanälen, bis auf wenige Prozent der erwarteten Signalamplitude vom minimal ionisierenden Teilchen, reduziert. Der Temperaturkoeffizient des Front-End-Chips wurde im n-XYTER Engineering-Lauf adressiert und erfolgreich beseitigt.

Ultraleichtes Detektormodul

Halterungsstrukturen mit geringer Masse wurden aus Kohlenstofffaser hergestellt, dies hat die Steifigkeit um die Detektor-Module halten zu können. Aufgrund der geringen Kernladungszahl des Materials verwendet für den Bau, werden geladene Teilchen minimaler Mehrfachstreuung ausgesetzt, die ein wesentlicher Faktor ist, der die Impulsauflösung verschlechtert. Die Verwendung von leichten Kompositmaterialien ermöglicht es eine Masse der Tragstruktur von nur 14 g pro 1000 mm zu erreichen. Durch Ausnutzung der hohen Steifigkeit der Träger aus Kohlenstofffaser, konnten die Halterungsstrukturen mit Planheit von 50 µm produziert wurden. Die Mikrokabel übertragen die analogen Signale von den Sensoren an die Front-End-Elektronik an der Peripherie der Stationen außerhalb der Detektorakzeptanz. Aufgrund der Struktur eines Detektormoduls, wo die Mikrokabel den größten Teil der Silizium-Sensoren decken, durchqueren Partikel unvermeidlich die Mikrokabel. Deswegen ist das geringe Materialbudget eine entscheidende Designanforderung. Die Prototypmikrokabel wurden mit Aluminiumleiterbahnen auf einem Polyimidsubstrat erzeugt. Polyimid verwendet als Trägermaterial bietet eine hohe Strahlungstoleranz, gute elektrische Eigenschaften, wie z.B. eine niedrige Dielektrizitätskonstante ($\varepsilon = 3.5$) und einen hohen spezifischen Widerstand. Das Polyimid bleibt im breiten Umfang von Temperaturen mechanisch stabil, der weit über die Betriebsbedingungen des STS reicht. Aluminumleiterbahnen ergeben eine gute elektrische Verbindung bei niedrigerem Materialbudget als beispielsweise Kupfer. Die Mikrokabelstruktur enthält mehrere Lagen, optimiert für eine niedrige Kapazität der Leiterbahnen und somit geräuscharme Leistung. Das Kabel beinhaltet zwei Signallagen, Abstandhalter um kapazitives Übersprechen zu reduzieren und eine Abschirmlage für geräuscharme Leistung. Die hergestellten Kabelprototypen haben ein Materialbudget von rund $0.1\%\mathrm{X}_0$. Aufgrund der Länge bis zu 60 cm, war ein weiteres Optimierungskriterium für die Mikrokabel die Reduktion von Rauschanteil verbunden mit Kapazität und Serienwiderstand.

Charakterisierung im Strahl

Es wurde ein Tracking-Teleskop-Demonstrator gebaut und in mehreren Strahlentests, einschließlich 2.5 GeV Protonenstrahl an COSY Synchrotron (Jülich), betrieben. Drei Tracking-Stationen wurden ergänzt mit mehreren Hodoskopen, die als Strahl-Referenz für die selbstgetriggerte Elektronik dienten. Alternativ konnte die Elektronik im Trigger-Modus betrieben werden und die Szintillatorsignale als externen Trigger verwenden. Wenn Signale im Chip registriert werden, werden Zeitstempel und Amplitude der gefeuerten Kanäle aufgenommen und in der Offline- oder Online-Analyse verwendet um Tracking-Informationen und Korrelationen zwischen verschiedenen Stationen zu extrahieren. Eine der drei Tracking-Stationen wurde verwendet um den Einfallswinkel zu scannen und entsprechende Signalamplitude zu studieren. Ebenso wurde dessen Sensor gegen die bestrahlten ausgetauscht, um die potenzielle Verschlechterung der Ortsauflösung zu beobachten.

Die Datenanalyse ergab Informationen über analoge und zeitliche Signaleigenschaften. Nach der Clustersuche, wurde die Informationen über die gesammelte Signalladung erhalten. Die Ergebnisse für die p- und n-Seite entsprechen innerhalb der Fehler dem erwarteten Wert von 22800 Elektronen für ein minimal ionisierendes Teilchen, das 285 µm von Silizium durchdringt. Strahlprofile und Tracking-Performance-Informationen in drei Stationen und zwei Hodoskopen wurden erhalten. Station, die mit bestrahltem Sensor ausgestattet wurde, zeigt die Ortsauflösung von etwa 55 µm, deutlich schlechter als 30-35 µm für die unbestrahlten Sensoren. Positionsstabilität des Strahls wurde anhand speziell entwickelter Monitoring-Tools bewertet.

Schlussfolgerung

Als Ergebnis der durchgeführten Studien, wurden Microstripdetektormodulkomponenten charakterisiert. Die experimentellen Anforderungen für das STS wurden formuliert und ihre Wirkung auf Modulstruktur und seine Komponenten beschrieben. Um die Modulkomponenten validieren zu können, wurde eine Reihe von Demonstratorsystemen im Strahl charakterisiert.

Die durchgeführten Studien haben den Weg zur Integration der einzelnen Komponenten zu einem voll funktionsfähigen System dargestellt. Eine genaue Definition des endgültigen Detektormoduldesigns war außerhalb des Geltungsbereichs dieser Arbeit und muss noch erarbeitet werden. Der nächste Schritt wird die Systemintegration sein. Zu den laufenden Aktivitäten gehören Studien bezüglich der Kühlung und Stromversorgung der Detektor-Module und Stationen, Design des Strahlrohrs im Bereich von STS und ihre Integration mit dem Micro-Vertex-Detektor im Inneren des Magneten.

Bibliography

[1] D.J. Schwarz, *Evolution of gravitational waves through cosmological transitions*, Mod. Phys. Lett. A **13** (1998) p. 2771-2778.

[2] M. Hindmarsh, O. Philipsen, *WIMP dark matter and the QCD equation of state*, Phys. Rev. D **71** (2005) 087302.

[3] J.M. Lattimer, M. Prakash, *Neutron star structure and the equation of state*, Astroph. J. **550** (2001) p. 426-442.

[4] E. Shuryak, *Physics of strongly coupled quark-gluon plasma*, Progr. in Part. and Nucl. Phys. **62** (2009) p. 48-101.

[5] S. Aoki, *Lattice QCD*, Nucl. Phys. A **827** (2009) p. 145c-152c.

[6] H.H. Gutbrod, A.M. Poskanzer, H.G. Ritter, *Plastic Ball experiments*, Rep. Prog. Phys. **52** (1989) p. 1267-1328.

[7] A. Sandoval et al., *Streamer chamber experiments*, Nucl. Phys. A **400** (1983) p. 365-381.

[8] J.W. Harris, *The STAR experiment at the relativistic heavy ion collider*, Nucl. Phys. A **566** (1994) p. 277-285.

[9] S. Nagamiya, *PHENIX experiment at RHIC*, Nucl. Phys. A **566** (1994) p. 287-298.

[10] A. Sorin, V. Kekelidze, A. Kovalenko et al., *Heavy-ion program at NICA/MPD at JINR*, Nucl. Phys. A **855** (2011) p. 510-513.

[11] E. Vercellin, *The ALICE experiment at the LHC*, Nucl. Phys. A **805** (2008) p. 511-518.

[12] J. Schukraft, *First Results from the ALICE experiment at the LHC*, Nucl. Phys. A **862–863** (2011) p. 78-84.

[13] P. Senger et al., *The compressed baryonic matter experiment at FAIR*, J. Phys. G: Nucl. Part. Phys. **36** (2009) 064037

[14] FAIR Baseline Technical Report (2006),
http://www.gsi.de/fair/reports/btr.html

[15] T. Hatsuda, *The phase diagram of dense QCD*, Rep. Prog. Phys. **74** (2011) 014001.

[16] B. Friman, C. Höhne, J. Knoll, S. Leupold, J. Randrup, R. Rapp (editors), *The CBM Physics Book: Compressed Baryonic Matter in Laboratory Experiments*, Springer Verlag, 2011.

[17] M.S. Borysova, *Quark-gluon plasma signals in the CBM experiment* (in Ukrainian), J. of Phys. Stud. **14** (2010) 3203, 7 p.

[18] J. Rafelski, B. Müller, *Strangeness Production in the Quark-Gluon Plasma*, Phys. Rev. Lett. **48** (1982) p. 1066-1069.

[19] P. Koch, B. Müller, J. Rafelski, *Strangeness in Relativistic Heavy Ion Collisions*, Phys. Rept. **142** (1986) p. 167-262.

[20] M.K. Mitrovski, *Strangeness production at SPS energies*, J. Phys. G **32** (2006) p. S43-S50.

[21] E. Andersen, F. Antinori, N. Armenise et al., *Strangeness enhancement at mid-rapidity in Pb-Pb collisions at 158 A GeV/c*, Phys. Lett. B **449** (1999) p. 401-406.

[22] T. Virgili, *Recent results from NA57 on strangeness production in p-A and Pb-Pb collisions at 40 and 158 A GeV/c* // arXiv:hep-ex/0405052, 6 p.

[23] A.R. Timmins [for the STAR Collaboration], *Overview of Strangeness Production at the STAR Experiment* // arXiv:0812.4080 [nucl-ex], 8 p.

[24] S. Hamieh, K. Redlich, A. Tounsi, *Canonical description of strangeness enhancement from p-A to Pb-Pb collisions*, Phys. Lett. B **486** (2000) p. 61-66.

[25] J. Noronha-Hostler, C. Greiner, I.A. Shovkovy, *Fast Equilibration of Hadrons in an Expanding Fireball*, Phys. Rev. Lett. **100** (2008) p. 252301-1 - 252301-4.

[26] J. Aichelin, C.M. Ko, *Subthreshold Kaon Production as a Probe of the Nuclear Equation of State*, Phys. Rev. Lett. **55** (1985) p. 2661-2663.

[27] G.Q. Li, C.M. Ko, *Subthreshold kaon production and the nuclear equation of state*, Phys. Lett. B **349** (1995) p. 405-410.

[28] M. Nekipelov et al., *Evidence of kaon nuclear and Coulomb potential effects on soft K^+ production from nuclei*, Phys. Lett. B **540** (2002) p. 207-212.

[29] W. Scheinast et al., *First observation of in-medium effects on phase space distributions of antikaons measured in proton-nucleus collisions*, Phys. Rev. Lett. **96** (2006) 072301.

[30] H.W. Barz, L. Naumann, *Contribution of the nucleon hyperon reaction channels to K- production in proton nucleus collisions*, Phys. Rev. C **68** (2003) 041901.

[31] M.F.M. Lutz, C.L. Korpa, M. Moeller, *Antikaons and hyperons in nuclear matter with saturation*, Nucl. Phys. A **808** (2008) p. 124-159.

[32] L. Tolos, A. Ramos, A. Polls, T.T. Kuo, *Partial wave contributions to the anti-kaon potential at finite momentum*, Nucl. Phys. A **690** (2001) p. 547-566.

[33] W. Cassing, L. Tolos, E.L. Bratkovskaya, A. Ramos, *Anti-kaon production in A+A collisions at SIS energies within an off-shell G matrix approach*, Nucl. Phys. A **727** (2003) p. 59-94.

[34] M.C. Abreu, B. Alessandro, C. Alexa et al., *J/ψ and Drell-Yan cross-sections in Pb-Pb interactions at 158 GeV/c per nucleon*, Phys. Lett. B **410** (1997) p. 327-336.

[35] M.C. Abreu, B. Alessandro, C. Alexa et al., *Observation of a threshold effect in the anomalous J/ψ suppression*, Phys. Lett. B **450** (1999) p. 456-466.

[36] T. Matsui, H. Satz, *J/ψ suppression by quark-gluon plasma formation*, Phys. Lett. B **178** (1991) p. 416-422.

[37] M.C. Abreu, B. Alessandro, C. Alexa et al., *Transverse momentum distributions of J/ψ, ψ', Drell-Yan and continuum dimuons produced in Pb-Pb interactions at the SPS*, Phys. Lett. B **499** (2001) p. 85-96.

[38] S. Gavin, R. Vogt, *Charmonium Suppression by Comover Scattering in Pb+Pb Collisions*, Phys. Rev. Lett. **78** (1997) p. 1006-1009.

[39] A. Capella, A.B. Kaidalov, D. Sousa, *Why is the J/ψ suppression enhanced at large transverse energy?*, Phys. Rev. C **65** (2002) p. 054908-1 - 054908-8.

[40] C. Spieles, R. Vogt, L. Gerland et al., *Modeling J/ψ production and absorption in a microscopic nonequilibrium approach*, Phys. Rev. C **60** (1999) p. 054901-1 - 054901-15.

[41] W. Ehehalt and W. Cassing, *Relativistic transport approach for nucleus-nucleus collisions from SIS to SPS*, Nucl. Phys. A **602** (1996) p. 449-486.

[42] A. Andronic, P. Braun-Munzinger, K. Redlich, J. Stachel, *Statistical hadronization of heavy quarks in ultra-relativistic nucleus–nucleus collisions*, Nucl. Phys. A **789** (2007) p. 334-356.

[43] H. Stoecker, W. Greiner, *High energy heavy ion collisions—probing the equation of state of highly excited hardronic matter*, Phys. Rept. **137** (1986) p. 277-392.

[44] S.A. Voloshin, A.M. Poskanzer, R. Snellings, *Collective phenomena in non-central nuclear collisions* // arXiv:0809.2949 [nucl-ex], 56 p.

[45] S.S. Adler, S. Afanasiev, C. Aidala et al., *Saturation of Azimuthal Anisotropy in Au+Au Collisions at* $\sqrt{s_{NN}} = 62$–$200\,\mathrm{GeV}$, Phys. Rev. Lett. **94** (2005) p. 232302-1 - 232302-6.

[46] H. Heiselberg, *Event-by-event physics in relativistic heavy ion collisions* // arXiv:nucl-th/0003046v5, 44 p.

[47] J. Adams, C. Adler, M.M. Aggarwal et al., *Net charge fluctuations in Au+Au collisions at* $\sqrt{s_{NN}} = 130\,\mathrm{GeV}$, Phys. Rev. C **68** (2003) p. 044905-1 - 044905-9.

[48] B.I. Abelev, M.M. Aggarwal, Z. Ahammed et al., *Beam-Energy and System-Size Dependence of Dynamical Net Charge Fluctuations*, Phys. Rev. C **79** (2009) p. 024906-1 - 024906-14.

[49] J. Adams, C. Adler, M.M Aggarwal et al. (STAR Collaboration), *Event-wise* $\langle p_t \rangle$ *fluctuations in Au-Au collisions at* $\sqrt{s_{NN}} = 130\,\mathrm{GeV}$*, Phys. Rev. C* **71** (2005) p. 064906-1 - 064906-10.

[50] M. Stephanov, K. Rajagopal, E.V. Shuryak, *Event-by-event fluctuations in heavy ion collisions and the QCD critical point*, Phys. Rev. D **60** (1999) p. 114028-1 - 114028-32.

[51] M.A. Stephanov, K. Rajagopal, E.V. Shuryak, *Signatures of the Tricritical Point in QCD*, Phys. Rev. Lett. **81** (1998) p. 4816-4819.

[52] C. Alt, T. Anticic, B. Baatar, et al., *Energy dependence of particle ratio fluctuations in central Pb+Pb collisions from* $\sqrt{s_{NN}} = 6.3$ *to 17.3 GeV*, Phys. Rev. C **79** (2009) p. 044910-1 - 044910-11.

[53] Ultrarelativistic Quantum Molecular Dynamics model (UrQMD), http://urqmd.org/

[54] V. Friese, *Simulation and reconstruction of free-streaming data in CBM*, J. Phys. Conf. Ser. **331** (2011) 032008.

[55] P. Senger, *The Compressed Baryonic Matter experiment at FAIR*, Nucl. Phys. A **862–863** (2011) p. 139-145.

[56] M. Deveaux, S. Amar-Youcef, A. Besson et al., *Radiation tolerance of CMOS monolithic active pixel sensors with self-biased pixels*, Nucl. Instr. and Meth. A **624** (2010) p. 428-431.

[57] S. Gorbunov, U. Kebschull, I. Kisel et al., *Fast SIMDized Kalman filter based track fit*, Comp. Phys. Comm. **178** (2008) p. 374-383.

[58] J.M. Heuser (CBM collaboration), *The Compressed Baryonic Matter Experiment at FAIR: Progress with feasibility studies and detector developments*, Nucl. Phys. A **830** (2009) p. 563c-566c.

[59] CbmROOT simulation and analysis framework, http://cbmroot.gsi.de/

[60] V. Bartsch et al., *An algorithm for calculating the Lorentz angle in silicon detectors*, Nucl. Instr. and Meth. in Phys. Res. A **497** (2003) p. 389-396.

[61] W.C. Sailor et al., *A model for the performance of silicon microstrip detectors*, Nucl. Instr. and Meth. in Phys. Res. A **303** (1991) p. 285-287.

[62] GEANT toolkit for the simulation of the passage of particles through matter, http://wwwasd.web.cern.ch/wwwasd/geant/

[63] FLUKA particle physics Monte Carlo simulation package, http://www.fluka.org/

[64] M. Huhtinen, *Simulation of non-ionising energy loss and defect formation in silicon*, Nucl. Instr. and Meth. A **491** (2002) p. 194-215.

[65] G. Lindström et al., *Developments for radiation hard silicon detectors by defect engineering–results by the CERN RD48 (ROSE) Collaboration*, Nucl. Instr. and Meth. in Phys. Res. A **465** (2001) p. 60-69.

[66] G. Lindström et al., *Radiation hard silicon detectors–developments by the RD48 (ROSE) collaboration*, Nucl. Instr. and Meth. in Phys. Res. A **466**, (2001) p. 308-326.

[67] M. Moll [RD50 Collaboration], *Development of radiation hard sensors for very high luminosity colliders–CERN-RD50 project*, Nucl. Instr. and Meth. in Phys. Res. A **511** (2003) p. 97-105.

[68] RD50 Collaboration, *Radiation hard semiconductor devices for very high luminosity colliders*, RD50 Status Report 2002/2003, CERN-LHCC-2003-058 and LHCC-RD-002, Nov. 2003.

[69] G. Kramberger, V. Cindro, I. Mandic, M. Mikuz, M. Zavrtanik, *Effective trapping time of electrons and holes in different silicon materials irradiated with neutrons, protons and pions*, Nucl. Instr. and Meth. in Phys. Res. A **481** (2002) p. 297-305.

[70] P.P. Allport, T.J.V. Bowcock, G. Casse, A. Greenall, J.N. Jackson, S. Martí i García, P.R. Turner, *Charge collection efficiency studies with irradiated silicon detectors*, Nucl. Instr. and Meth. in Phys. Res. A **501** (2003) p. 146-152.

[71] M. Da Rold et al., *Radiation effects on breakdown characteristics of multi-guarded devices*, IEEE Trans. Nucl. Science **44** (1997) p. 721.

[72] J. Kaneko et al., *Improvement of Radiation Hardness of Double-Sided Silicon Strip Detector for Belle SVD Upgrade*, IEEE Trans. Nucl. Science **49** (2002) p. 1593.

[73] J. Stahl, E. Fretwurst, G. Lindström, I. Pintilie, *Radiation hardness of silicon–a challenge for defect engineering*, Physica B **340–342** (2003) p. 705–709.

[74] J. Härkönen et al., *Radiation hardness of Czochralski silicon, Float Zone silicon and oxygenated Float Zone silicon studied by low energy protons*, Nucl. Instr. and Meth. in Phys. Res. A **518** (2004) p. 346-348.

[75] Z. Li, E. Verbitskaya, V. Eremin, B. Dezillie, W. Chen, M. Bruzzi, *Radiation hard detectors from silicon enriched with both oxygen and thermal donors: improvements in donor removal and long-term stability with regard to neutron irradiation*, Nucl. Instr. and Meth. in Phys. Res. A **476** (2002) p. 628-638.

[76] L. Fonseca, M. Lozano, F. Campabadal, C. Martínez, M. Ullán, B. S. Avset, A.Ruzin, F. Lemeilleur, E. Nossarzewska-Orlowska, *Silicon wafer oxygenation from* SiO_2 *layers for radiation hard detectors*, Microel. Reliab. **40** (2000), p. 791-794.

[77] G. Casse, P.P. Allport, S. Martí i Garcia, M. Lozano, P.R. Turner [CERN/RD50 Collaboration], *First results on charge collection efficiency of heavily irradiated microstrip sensors fabricated on oxygenated p-type silicon*, Nucl. Instr. and Meth. in Phys. Res. A **518** (2004) p. 340-342.

[78] P.P. Allport, G. Casse, A. Greenall, *Radiation tolerance of oxygenated n-strip read-out detectors*, Nucl. Instr. and Meth. in Phys. Res. A **513** (2003) p. 84-88.

[79] G. Casse, P.P. Allport, S.F. Biagi, T.J.V. Bowcock, A. Greenall, P.R. Turner, *Charge collection and charge sharing in heavily irradiated n-side read-out silicon microstrip detectors*, Nucl. Instr. and Meth. in Phys. Res. A **511** (2003) p. 112-117.

[80] I. Pintilie, M. Petris, C. Tivarus, M. Moll, E. Fretwurst, G. Lindström, *Some annealing effects in proton irradiated silicon detectors*, Semicond. Conf., CAS 2000 Proc. Int., Vol. 1 , 10-14 Oct. 2000, p. 259-262.

[81] M. Da Rold et al., *Study of breakdown effects in silicon multiguard structures*, IEEE Trans. Nucl. Science **46** (1999) p. 1215-1223.

[82] S.N. Igolkin, Yu.A. Murin, G.A. Feofilov, J.M. Heuser, *Ultra light-weight carbon-fiber structures for the CBM Silicon Tracking System*, CBM Progress Report 2008, Darmstadt 2009, p. 19.

[83] The LHCb collaboration, *The LHCb Detector at the LHC*, J. Instr. V3 S08005 (2008) p. 42.

[84] C. Bauer et al., *Radiation hardness of the HERA-B double-sided silicon strip detectors*, Nucl. Instr. and Meth. in Phys. Res. A **485** (2002) p. 116-120.

[85] G. Lindström, M. Moll, E. Fretwurst, *Radiation hardness of silicon detectors – a challenge from high-energy physics*, Nucl. Instr. and Meth. in Phys. Res. A **426** (1999) p. 1-15.

[86] M. Agaria, O. Steinkamp, *Design of the LHCb silicon tracker*, Nucl. Instr. and Meth. A **535** (2004) p. 352-356.

[87] O. Torheim, V. Kleipa, *Investigation on next STS FEB*, 17th CBM Collaboration Meeting, Dresden, 4-8 April 2011.
https://indico.gsi.de/getFile.py/access?contribId=98&
sessionId=2&resId=1&materialId=slides&confId=1118

[88] P. Chochula et al., *The DELPHI Silicon Tracker at LEP2*, Nucl. Instr. and Meth. A **412** (1998) p. 304-328.

[89] C.S. Hill, *Operational experience and performance of the CDFII silicon detector*, Nucl. Instr. and Meth. A **530** (2004) p. 1-6.

[90] Y. Unno, *ATLAS silicon microstrip Semiconductor Tracker (SCT)*, Nucl. Instr. and Meth. A **453** (2000) p. 109-120.

[91] F. Hartmann [for the CMS Silicon Tracker Collaboration], *Construction of the CMS Tracker*, Nucl. Instr. and Meth. A **572** (2007) p. 73-76.

[92] F. Hartmann, *Silicon tracking detectors in high-energy physics*, Nucl. Instr. and Meth. A **666** (2012) p. 25-46.

[93] G. Lutz, *Semiconductor Radiation Detectors – Device Physics*, Springer-Verlag, Berlin Heielberg 2001.

[94] A.I. Abramov, Yu.A. Kazansky, Ye.S. Matusevich, *Fundamentals of experimental methods in nuclear physics* (in Russian), Atomizdat, Moscow (1985) BBK 33.38.

[95] A.A. Grillo et al., *A Prototype Front-End Readout Chip for Silicon Microstrip Detectors Using an Advanced SiGe Technology*, Proc. of the Top. Worksh. on Electr. for Part. Phys. (TWEPP-09), Paris, France, pp 379-383, Sep. 2009.

[96] D. Nouais, *The ALICE Silicon Drift Detector system*, Nucl. Instr. and Meth. A **501** (2003) p. 119-125.

[97] M. Needham, *The LHCb Silicon Tracker*, Nucl. Instr. and Meth. A **530** (2004) p. 23-27.

[98] J.M. Heuser, *Development of a Silicon Tracking and Vertex Detection System for the CBM Experiment at FAIR*, Nucl. Instr. and Meth. A **582** (2007) p. 910-915.

[99] J.M. Heuser, Chr.J. Schmidt, A. Lymanets, R. Röder, and L. Long, *First microstrip detector prototypes for the CBM Silicon Tracking System*, CBM Progress report 2007, Darmstadt 2008, p. 32.

[100] K. Hara et al., *Design of Punch-Through Protection of Silicon Microstrip Detector against Accelerator Beam Splash*, Physics Procedia **37** (2012) p. 838-843.

[101] J.M. Heuser, C.J. Schmidt, A. Lymanets, R. Röder, and L. Long, *Development of microstrip detectors for the CBM Silicon Tracking System*, CBM Progress report 2008, Darmstadt 2009, p. 10.

[102] J. Ellison et al., *Punch-through currents and floating strip potentials in silicon detectors*, IEEE Trans. Nucl. Science **36** (1989) p. 267-271.

[103] V. Chabaud et al., *The DELPHI silicon strip microvertex detector with double-sided readout*, Nucl. Instr. and Meth. A **368** (1996) p. 314-332.

[104] T.I. Westgaard et al., *Radiation hardness of punch-through and FET biased silicon microstrip detectors*, Nucl. Instr. and Meth. A **377** (1996) p. 429-434.

[105] G. Giacomini et al., *Noise Characterization of Double-Sided Silicon MicroStrip Detectors with Punch-Through Biasing*, IEEE NSS 2008 Conference Record, N30-386.

[106] L. Andricek et al., *Radiation hard strip detectors for large-scale silicon trackers*, Nucl. Instr. and Meth. A **436** (1999) p. 262-271.

[107] S.M. Sze, *Physics of Semiconductor Devices*, 2nd ed., John Wiley & Sons, New York, 1981.

[108] R.H. Richter et al., *Strip detector design for ATLAS and HERA-B using two-dimensional device simulation*, Nucl. Instr. and Meth. A **377** (1996) p. 412-421.

[109] H. Sadrozinski et al., *Total dose dependence of oxide charge, interstrip capacitance and breakdown behavior of sLHC prototype silicon strip detectors and test structures of the SMART collaboration*, Nucl. Instr. and Meth. A **579** (2007) p. 769–774.

[110] J.M. Heuser, L. Long, M. Luleich, H.G. Ortlepp, and R. Röder, *Progress with the development of double-sided microstrip detectors for the CBM Silicon Tracking System*, CBM Progress report 2009, Darmstadt 2010, p. 10.

[111] J.M. Heuser, L. Long, H.G. Ortlepp, S. Chatterji, A. Lymanets, I. Sorokin, M. Singla, C.J. Schmidt, V. Kleipa, C. Simons, W. Niebur, L. Xu, and A. Hastir, *Development of microstrip detectors for the CBM Silicon Tracking System*, CBM Progress report 2010, Darmstadt 2011, p. 10.

[112] A. Dierlamm, *Irradiations in Karlsruhe*, RD50 Workshop, 01.06.2010. http://indico.cern.ch/getFile.py/access?contribId=19&sessionId=3&resId=1&materialId=slides&confId=86625

[113] G. Casse et al., *A comparative study of oxygenated and non-oxygenated Si pad diodes, miniature and large area microstrip detectors*, Nucl. Instr. and Meth. A **466** (2001) p. 335–344.

[114] V. Eremin, *Comparative analysis of double and single sided silicon strip detectors for the STS*, 17th CBM Collaboration Meeting and Symposium on Charm, Dileptons and Deconfinement, April 4 - 8, 2011, Dresden, Germany.

[115] V. Eremin, E. Verbitskaya, Z. Li, *The origin of double peak electric field distribution in heavily irradiated silicon detectors*, Nucl. Instr. and Meth. A **476** (2002) p. 556.

[116] V. Pugatch et al., *Characterization of CBM01 sensors for the Silicon Tracking System*, CBM Progress report 2008, Darmstadt 2009, p. 15.

[117] V. Pugatch et al., *Laser stand for testing STS silicon microstrip detector modules*, CBM Progress report 2008, Darmstadt 2009, p. 16.

[118] V. Pugatch, M. Borysova, A. Chaus, J. M. Heuser, O. Kovalchuk, V. Kyva, A. Lymanets, A. Melnyk, V. Militsiya, O. Okhrimenko, Yu. Sorokin, D. Storozhik, V. Perevertailo, V. Zhora, *Characterization of CBM prototype microstrip detectors*, CBM Progress report 2009, Darmstadt 2010, p. 11.

[119] V. Pugatch, J. Heuser, V. Kyva, A. Lymanets, G. Melnyk, V. Militsiya, O. Okhrimenko, Y. Panasenko, *Development of a Quality Assurance System for the Silicon Tracking System*, CBM Progress report 2009, Darmstadt 2010, p. 12.

[120] J. Heuser, V. Kyva, A. Lymanets, H. Malygina, V. Militsiya, Y. Panasenko, V. Pugatch, I. Sorokin, *Development of a Quality Assurance System for the Silicon Tracking System*, CBM Progress report 2010, Darmstadt 2011, p. 18.

[121] J. Heuser, V. Kyva, H. Malygina, V. Militsiya, Y. Panasenko, V. Pugatch, I. Sorokin, *Performance of the n-XYTER chip with external triggering*, CBM Progress report 2011, Darmstadt 2012, p. 25.

[122] L. Bardelli et al., *A method for non-destructive resistivity mapping in silicon detectors*, Nucl. Instr. and Meth. A **602** (2009) p. 501-505.

[123] S. Beolè et al., *Study of the uniformity of high resistivity neutron doped silicon wafers for silicon drift detectors*, Nucl. Instr. and Meth. A **473** (2001) p. 319-325.

[124] H. Spieler, *Semiconductor detector systems*, Oxford University Press, New York (2005).

[125] LCR Measurement Primer (Part Number 030122 A6), 6th Edition, QuadTech, Inc. November 2009, p. 22.

[126] Ye.G Zveryev, D.E. Karmanov, M.A. Kurbantsev, A.K. Leflat, V.M. Manakov, M.M. Merkin, Ye.K. Shabalina, *Measurement of interstrip capacitance of single-sided microstrip detectors for D0 experiment (FNAL)* (in Russian) // Preprint 14/518. Lomonosov Moscow State University Skobeltsyn Institute of Nuclear Physics, Moscow, 1998, 23 p.

[127] I. Rachevskaia, L. Bosisio, S. Potin, O. Starodubtsev, *Test and quality control of double-sided silicon microstrip sensors for the ALICE experiment*, Nucl. Instr. and Meth. A **530** (2004) p. 59-64.

[128] N.L. Bruner, M.A. Frautschi, M.R. Hoeferkamp, S.C. Seidel, *Characterization procedures for double-sided silicon microstrip detectors*, Nucl. Instr. and Meth. A **362** (1995) p. 315-337.

[129] G.-F. Dalla Betta, M. Boscardin, L. Bosisio, *A comparative evaluation of integrated capacitors for AC-coupled microstrip detectors*, Nucl. Instr. and Meth. A **411** (1998) p. 369-375.

[130] D. Karmanov, *Development and construction of the forward tracker for the D0 experiment* (in Russian). Diss. Lomonosov Moscow State University Skobeltsyn Institute of Nuclear Physics, Moscow, 2008, 155 p.

[131] E. Catacchini, *Characterization of a Double Sided Microstrip Silicon wedge Detector*, Nucl. Phys. B (Proc. Suppl.) **61** (1998) p. 335-340.

[132] D. Passeri, G.M. Bilei, M.M. Angarano, F. Moscatelli, *Analysis and Test of Overhanging-Metal Microstrip Detectors*, IEEE NSS-MIC 2000 Conference Record, October 15-20, 2000, Lyon, France, p. 3/28 - 3/30.

[133] A.S. Brogna, S. Buzzetti, W. Dabrowski, T. Fiutowski, B. Gebauer, M. Klein, C.J. Schmidt, H.K. Soltveit, R. Szczygiel, U. Trunk, *N-XYTER, a CMOS read-out ASIC for high resolution time and amplitude measurements on high rate multi-channel counting mode neutron detectors*, Nucl. Instr. and Meth. A **568** (2006) p. 301-308.

[134] DETNI - Detectors for Neutron Instrumentation,
http://jra1.neutron-eu.net/jra1/

[135] C.J. Schmidt, M. Höhl, V. Kleipa, W. Müller, H.K. Soltveit, A. Lymanets, *Characterization of the n-XYTER chip and preparations for the engineering run*, CBM Progress report 2009, Darmstadt 2010, p. 50.

[136] T. Balog, A. Lymanets, *Calibration of the n-XYTER front-end chip*, CBM Progress report 2011, Darmstadt 2012, p. 24.

[137] A. Kotynia, J.M. Heuser, *Performance simulations with a realistic model of the CBM Silicon Tracking System*, Progress Report 2010, Darmstadt 2011, p. 8-9.

[138] V. Friese, J.M. Heuser, V. Kleipa, S. Linev, W. Müller, W. Niebur, C.J. Schmidt, A. Kotynia, A. Lymanets, A. Wilczek, B. Bozsogi, *Operation and performance of the CBM Silicon Tracking reference telescope*, CBM Progress Report 2009, Darmstadt 2010, p. 9.

[139] A. Andronic, P. Braun-Munzinger, K. Redlich, J. Stachel, *Charmonium and open charm production in nuclear collisions at SPS/FAIR energies and the possible influence of a hot hadronic medium*, Phys. Lett. B **659** (2008) p. 149-155.

[140] S. Manz, N. Abel J. Gebelein and U. Kebschul, *An Universal Read-out Controller*, Topical Workshop on Electronics in Particle Physics 2010, Aachen, 20-24 Sep. 2010.

[141] N. Abel, S. Manz, U. Kebschull, *Design and Implementation of an Universal Read Out Controller*, GSI Scientific Report 2009, Darmstadt 2010, p. 323.

[142] F. Lemke, D. Slogsnat, N. Burkhardt, U. Bruening, *A Unified Interconnection Network with Precise Time Synchronization for the CBM DAQ-System*, IEEE Trans. Nucl. Sci. **57** (2010) p. 412.

[143] W. Gao, A. Kugel, A. Wurz, G. Marcus, R. Männer, *Active buffer for DAQ in CBM experiment*, Proc. 16th IEEE-NPSS Real Time Conference 2009, Beijing, 10-15 May 2009, p. 527-531.

[144] F. Lemke, S. Schenk, U. Bruening, *Prototype Results of an Optical Communication Network for the CBM*, GSI Scientific Report 2009, Darmstadt 2010, p. 87.

[145] J. Adamczewski-Musch, H.-G. Essel, N. Kurz and S. Linev, *Data Acquisition Backbone Core DABC release v1.0*, J. Phys.: Conf. Ser. 219 (2010) 022007.

[146] J.M. Heuser, V. Borshchov, S. Chatterji, M. Singla, W.F.J. Müller, *Development of low-mass readout cables for the CBM Silicon Tracking System*, CBM Progress Report 2010, Darmstadt 2011, p. 14.

[147] Yu.A. Murin, V.A. Vasendina, V.A. Budilov, S.N. Igolkin, D.E. Karmanov, V. Lenok, M.M. Merkin, N.N. Egorov, S.A. Golubkov, V.M. Borshchov, M.A. Protsenko, I.T. Tymchuk, J. Heuser, *First experience in prototyping detector modules for the CBM STS*, CBM Progress Report 2011, Darmstadt 2012, p. 19.

[148] V. Pugatch et al., *Supporting frame and microcable properties for the STS microstrip detector module prototype*, CBM Progress Report 2008, Darmstadt 2009, p. 17.

[149] S.N. Igolkin, Yu.A. Murin, S.N. Vinogradov, *Pre-production of ultra-light carbon fiber support frames for the CBM-STS*, CBM Progress Report 2011, Darmstadt 2012, p. 20.

[150] ROClib, https://subversion.gsi.de/cbm/ROC

[151] K. Kasinski, R. Szczygiel, P. Gryboś, *TOT01, a time-over-threshold based readout chip in 180nm CMOS technology for silicon strip detectors*, JINST 6 (2011) C01026.

[152] K. Kasinski, R. Szczygiel, P. Gryboś, *Evolution of a prototype Silicon strip detector readout ASIC for the STS*, CBM Progress Report 2010, Darmstadt 2011, p. 22.

[153] R. Szczygiel, P. Gryboś, K. Kasinski, R. Kleczek, *Proposed architecture of prototype readout ASIC for CBM STS*, CBM FEE/DAQ/FLES Workshop, ZITI, University of Heidelberg, Germany, January 25-27, 2012.

[154] F. Lemke, S. Schenk, U. Brüning, *The adapted CBM network structure design and CBMnet V2.0 implementation*, CBM Progress Report 2011, Darmstadt 2012, p. 61.

[155] J. de Cuveland, V. Lindenstruth, *A First-level Event Selector for the CBM Experiment at FAIR*, J. Phys. Conf. Ser. **331** (2011) 022006.

[156] J.M. Heuser, W. Niebur, R. Karabowicz, W. Müller, V. Friese, C.J. Schmidt, R. Lalik, A. Lymanets, Y. Murin, P. Nomokonov, *First test of a prototype CBM silicon detector system in a proton beam at GSI*, CBM Progress Report 2008, Darmstadt 2009, p. 11.

[157] A. Kotynia, J.M. Heuser, W. Müller, *Simulation of realistic detector response in the CBM Silicon Tracking System*, CBM Progress Report 2009, Darmstadt 2010, p. 7.

[158] V.M. Borshchov, J.M. Heuser, Yu.A. Murin, M.V. Zamirets, O.M. Listratenko, M.A. Protsenko, I.T. Tymchuk, *Design and assembly of STS demonstrator module 0-B*, CBM Progress Report 2008, Darmstadt 2009, p. 12.

[159] J.M. Heuser, W. Niebur, W. Müller, S. Linev, J. Adamczewski-Musch, V. Friese, B.W. Kolb, S. Chatterji, T. Balog, A. Lymanets, I. Sorokin, M. Singla, *Test of prototype modules of the CBM Silicon Tracking System in a proton beam at COSY*, CBM Progress report 2010, Darmstadt 2011, p. 19.

[160] L. Snoj, G. Žerovnik, A. Trkov, *Computational analysis of irradiation facilities at the JSI TRIGA reactor*, Appl. Rad. and Isot. **70** (2012) p. 483–488.

[161] Experimental Physics and Industrial Control System, http://www.aps.anl.gov/epics/

[162] M. Singla, *Simulation and noise study for ultra-thin readout kapton cables*, 17th CBM Collaboration Meeting, Dresden, Germany, 2011.

[163] W. Dąbrowski, P. Gryboś, M. Idzik, *Study of spatial resolution and efficiency of silicon strip detectors with different readout schemes*, Nucl. Instr. and Meth. A **356** (1995) p. 241-254.

[164] Data Acquisition Backbone Core (DABC), http://dabc.gsi.de/

[165] GSI Object Oriented On-line Off-line system (Go4), http://www-win.gsi.de/go4/

[166] Multi Branch System (MBS), http://www-win.gsi.de/daq/

[167] Control System Studio (CSS), http://css.desy.de/content/index_eng.html