The CBM Silicon Tracking System front-end electronics

from bare ASIC to detector characterization, commissioning and performance

Dissertation
zur Erlangung des Doktorgrades
der Naturwissenschaften

vorgelegt beim Fachbereich Physik
der Johann Wolfgang Goethe-Universität
in Frankfurt am Main

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Frankfurt am Main (2019)
(D 30)

vom Fachbereich Physik der
Johann Wolfgang Goethe-Universität als Dissertation angenommen.

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Datum der Disputation:	15. Mai 2020

"An experiment is a question science poses to Nature and a measurement is the recording of Nature's answer"

Max Planck

To my family

Contents

Abstract

The last decades have brought tremendous progress in understanding the phase structure of the strongly interacting matter. This has been driven by studying heavy-ion collisions on the experimental side and Lattice QCD, functional approaches to QCD, perturbation theory and effective theories on the theoretical side. Of particular interest is the transition from hadrons to partonic degrees of freedom which is expected to occur at high temperatures or high baryon densities. These phases play an important role in the early universe and the core of neutron stars. Nowadays, the existence of a deconfined phase, i.e. Quark Gluon Plasma (QGP) and its phase transition at vanishing and small net-baryon densities, are well established. However, the situation at larger densities is less clear.

Complementary to the studies of matter at high temperatures and low net-baryon densities performed at RHIC and LHC, the proposed Compressed Baryonic Matter (CBM) experiment at the future FAIR facility, aims to explore the QCD phase diagram at very high baryon-net densities and moderate temperatures. The CBM research program includes the search for the deconfinement phase transition, the study of chiral symmetry restoration in super dense baryonic matter, the search for the critical endpoint, and the study of the nuclear equation of state at high densities. While other experiments (STAR-BES at BNL, BM@N at NICA) are suited to measure bulk observables, CBM is explicitly designed to access rare observables, such as multi-strange hadrons, dileptons, hypernuclei and charmonium. Therefore, a key feature of CBM is the very high interaction rate, exceeding those of contemporary and proposed nuclear collision experiments by several orders of magnitude. However, some of the rare probes have a complex signature, hidden in a background of several hundreds of charged tracks. This forbids a conventional, hardware-triggered readout; instead, the experiment combines self-triggered front-end electronics, fast and free-streaming data transport, online event reconstruction and online event selection.

The central detector for tracking and momentum determination of charged particles in the CBM experiment is the Silicon Tracking System (STS). It is designed to measure up to 700 charged particles in nucleus-nucleus collisions between 0.1 and 10 MHz interaction rate, to achieve a momentum resolution in 1 Tm dipole magnetic field better than 2%, and to be capable of identifying complex particle decays topologies, e.g., such with strangeness content. The STS comprises 8 tracking stations equipped with double-sided silicon microstrip sensors. Two million channels are read out with self-triggering electronics, matching the data streaming and on-line event analysis concept applied throughout the experiment. The detector's functional building block consists of a silicon sensor, aluminum-kapton microcables and two front-end electronics boards integrated in a module. The custom-designed ASIC (STS-XYTER) implements the analog front-end, the digitizer and the generation of individual hit data for each signal.

Design of the front-end chip requires finding an optimal solution for time and input charge measurements with tight constraints: small area (58 μm channel pitch), low noise levels (below 1500 ENC(e^-)), low power consumption ($\leqslant$10 mW/channel), radiation hard architecture and speed requirements. Being a part of the first processing stage in the full readout and data acquisition chain, the characterization of the chip and its integration with the detector components is a crucial

task. In this work, various methods and tools are established for testing and qualifying the ASIC analog front-end. A procedure for amplitude and timing calibration is developed using different functionalities of the chip. The procedure is optimized for our prototype system in order to achieve the best accuracy in the shortest amount of time. Results were verified using a gamma source and an external pulse generator, showing discrepancies below 5%.

Among the multiple operation requirements of the ASIC, the noise performance is of essential importance. The characterization of the chip noise is carried out as a function of a large number of parameters such as: low-voltage power regulators, input capacitance, shaping time, temperature and bond's protective glue (glob-top). These studies allowed to optimize the ASIC configuration settings, to identify possible malfunctions in the low voltage powering scheme and to select possible glob-top materials to be used in the module assembly. Moreover, important differences are found among odd and even channels, which main cause was related to the bias scheme of the amplifiers of the two groups of channels. This effect has been corrected in the new version (v2.1) of the ASIC.

Despite the STS front-end electronics being located outside of the physics acceptance, they will be exposed to high fluxes of charged particles. Considering the SIS100 possible running scenario, the lifetime dose at the location of the electronics is expected not to exceed 800 krad. Consequently, the STS-XYTERv2 ASIC implements a radiation hard design based on dual-interlocked cells (DICE), and triple modular redundancy (TMR).

Multiple dedicated beam campaigns were carried out to evaluate the ASIC's design in terms of immunity to single event upsets (SEU) errors and overall performance after a lifetime doses. The DICE cell SEU cross section was measured in a high-intensity proton beam. Result show a significant improvement of the SEU immunity in the STS-XYTERv2 compared to its predecessor, and allows to estimate the upset rate in the CBM running scenario, resulting in less than one SEU/ASIC/day.

The studies on the total ionizing dose (TID) show that the overall noise levels for the ASIC, at the end of the experiment lifetime, are expected to increase by approximately $40 - 60\%$. Moreover, they demonstrated that short periods of annealing at room temperature can favorably influence the noise performance of the chip.

The assembly and test of the STS modules, a complex process with multiple stages and a long learning curve, is illustrated in different parts of this work. The first prototype modules were built with the front-end board type B (FEBs-B), capable of reading out 128 channels for p and n side respectively. The studies were conducted with a relativistic proton beam of 1.7 GeV/c momentum at the COSY accelerator facility, Research Center Jülich, in March 2018. The campaign brought valuable insights to the development of an effective grounding and powering scheme for reading out the detectors. The signal-to-noise was measured for one of the prototype modules, resulting in values larger than 15 for both polarities. A deeper analysis into the collected data allowed the identification of a logic error in the ASIC that affected the readout rate and the quality of the data. This issue was corrected in the new version of the chip.

A precursor of the STS detector, named mini-STS (mSTS), has been built within the mCBM project carried out in FAIR Phase0. mSTS was built from 4 fully assembled detector modules. To ensure the proper operation of the ASICs that were used in the module assembly, it was required to develop a rigorous quality assurance procedure. A dedicated setup was built based on a custom designed pogo-pin station and a total of 339 chips were tested. More than 90% of good-quality and operational ASICs were obtained. In the mCBM beam campaign of March 2019, four detector modules were successfully operated in a close-to-final readout chain and valuable data were collected. The mSTS detector was exposed to the products of Ag+Au collisions at energies above 1.58 AGeV and overall interaction rates up to 10^6, which resembles the real conditions of the CBM experiment.

Along this work, significant progress for the development of the STS detector modules was achieved. Techniques for characterization of the front-end electronics and the complete detector system were developed and worked out. They will be applied for QA of the components during the series production.

Kurzfassung

Die vergangenen Jahrzehnte haben große Fortschritte im Verständnis der Phasenstruktur stark wechselwirkender Materie gebracht. Von experimenteller Seite wurde dies ermöglicht durch die Untersuchung von Schwerionenkollisionen, von theoretischer durch Lattice-QCD, funktionale QCD-Ansätze, Störungstheorie und effektive Theorien. Von besonderem Interesse ist der Übergang von hadronischen zu partonischen Freiheitsgraden, der bei hohen Temperaturen oder bei hohen Baryonendichten erwartet wird. Diese Phasen spielen eine wichtige Rolle im Verständnis des frühen Universums und der Kerne von Neutronensternen. Die Existenx einer "deconfined" Phase, des Quark-GLuon-Plasmas (QGP) und des zugehörigen Phasenübergangs bei verschwindenden oder kleinen Baryonendichten sind zwischenzeitlich wohl etabliert. Die Situation bei hohen Dichten ist jedoch weniger gesichert. Die Erforschung des Phasendiagramms stark wechselwirkender Materie ist ein bedeutendes Feld der modernen Schwerionen- und Hochenergiephysik.

Komplementär zu den Studien von Materie bei hoher Temperatur und kleinen Netto-Baryonendichten am RHIC und LHC zielt das geplante "Compressed Baryonic Matter" (CBM) Experiment an der zukünftigen FAIR Beschleunigeranlage darauf ab, das QCD-Phasendiagramm bei sehr hohen Baryonendichten und moderaten Temperaturen zu untersuchen. Das CBM-Forschungsprogramm beinhaltet die Suche nach dem "Deconfinement"-Phasenübergang, Untersuchungen zur Wiederherstellung der chiralen Symmetrie in superdichter baryonischer Materie, die Suche nach dem kritischen Endpunkt und die Untersuchung der nuklearen Zustandsgleichung bei hohen Dichten. Während andere Experimente (STAR-BES bei RHIC/BNL, BM@N bei NICA/JINR) vor allem häufig produzierte ("bulk") Observable messen, ist CBM explizit zur Messung seltener Observablen konzipiert, wie z.B. "mehrfach seltsame" Hadronen, Dileptonen, Hyperkerne und Charmonium. Eine Schlüsselfähigkeit von CBM ist daher die sehr hohe Wechselwirkungsrate, die um mehrere Größenordnungen über den Raten existierender und anderer vorgeschlagener Experimente der Kernphysik liegt. Die gesuchten seltenen Proben haben jedoch komplexe Ereignissignaturen innerhalb eines Untergrundes von mehreren Hundert Spuren geladener Teilchen. Dies verbietet eine konventionelle, hardware-getriggerte Auslese. CBM kombiniert daher selbsttriggernde Frontend-Elektronik, einen schnellen "free-streaming" Datentransport sowie eine in Echtzeit durchgeführte Ereignisrekonstruktion und -selektion.

Der zentrale Detektor für Spurerkennung und Impulsmessung geladener Teilchen im CBM-Experiment ist das sogenannte "Silicon Tracking System" (STS). Es ist in der Lage, bis zu 700 geladene Teilchen in Kern-Kern-Kollisionen bei Wechselwirkungsraten von 0.1 bis zu 10 MHz zu messen, eine Impulsauflösung besser als 2% in einem 1 Tm Dipol-Magnetfeld zu erzielen, und komplexe Zerfallstopologien, z.B. mit Strangeness-Content, zu identifizieren. Der STS besteht aus 8 Detektorlagen zur Spurkennung mittels doppelseitig segmentierter Silizium-Streifensensoren. Etwa zwei Millionen Kanäle werden mittels selbstgetriggerter Elektronik ausgelesen, in Einklang mit dem Data-Streaming und Echtzeit-Ereignisanalyse-Konzept, das im gesamten Experiment angewandt wird. Die funktionelle Einheit des STS-Detektors ist das sogenannte "Modul", bestehend aus einem Silizium-Sensor, geringmassigen Aluminium-Kapton-Auslesekabeln und zwei Frontend-Elektronik-Boards. Der dediziert für CBM-STS entwickelte ASIC (STS-XYTER) implementiert die analoge

Elektronik, die Digitalisierung sowie die Erzeugung individueller Datenworte für jedes Signal.

Die Entwicklung des Frontend-Chips erfordert das Finden einer optimalen Lösung für Zeit- und Ladungsmessung unter engen Randbedingungen: Geringe zur Verfügung stehende Fläche (58 μm Kanal-Abstand), niedriges Rausch-Niveau ($<$1500 ENC(e^-)), geringe Leistung ($\leqslant$10 mW/Kanal), strahlenharte Architektur und hohe Geschwindigkeit.

Die Charakterisierung des ASIC sowie seine Integration mit den Detektorkomponenten sind wichtige Aufgaben als Teil der ersten Verarbeitungsstufe in der kompletten Auslese- und Datenaufnahmekette. In dieser Arbeit werden diverse Methoden und Werkzeuge für das Testen und die Characterisierung des ASIC-Analogteils etabliert. Prozeduren für die Kalibration von Zeitstempel and Signalamplitude wurden entwickelt unter Verwendung unterschiedlicher Funktionalität des Chips. Die Prozeduren sind für das momentan benutzte Prototypsystem optimiert, um bestmögliche Präzision in kürzestmöglicher Zeit zu erreichen. Die Kalibrations-Ergebnisse wurden mit einer Gamma-Quelle sowie einem externen Signalgenerator überprüft, wobei eine Abweichung von unter 5% zwischen gemessenen und kalibrierten Werten festgestellt wurde. Unter den vielfältigen Anforderungen an den ASIC ist das Rauschverhalten von essentieller Bedeutung. Die Charakterisierung des ASIC-Rauschens wurde als Funktion einer großen Anzahl von Systemparametern durchgeführt: Spannungsregler der Niederspannungsversorgung, Eingangskapazität, ASIC shaping-time, Temperatur und Typ des Schutzklebers der ASIC-Drahtbonds (glob-top). Mit Hilfe dieser Studien wurde die ASIC-Konfiguration optimiert, potentielle Fehlfunktionen im System der Niederspannungsversorgung identifiziert sowie geeignete Glob-Top-Materialien für den Modulbau ausgewählt. Daneben wurden signifikante Unterschiede im Verhalten gerad- bzw. ungeradzahliger Kanalnummern gefunden, die auf Unterschiede im Bias-Schema der Verstärkerschaltungen dieser beiden Kanalgruppen zurückgeführt werden konnten. Dies wurde in der neuesten ASIC-Version v2.1 korrigiert und ein einheitliches Verhalten aller Kanäle erreicht.

Die STS-Frontend-Elektronik ist ausserhalb der geometrischen STS-Detektorakzeptanz platziert, jedoch auch dort hohen Flüssen geladener Teilchen ausgesetzt. Für ein Einsatzszenario am SIS100-Beschleuniger liegt die erwartete Dosis über die gesamte Lebensdauer des Experiments am Ort der Elektronik bei bis zu 800 krad. Der STS-XYTERv2 ASIC implementiert daher ein strahlenhartes Design unter Verwendung von Dual-Interlocked Cells (DICE) sowie Triple Modular Redundancy (TMR). Mehrere dedizierte Strahlzeiten wurden durchgeführt, um das ASIC-Design hinsichtlich Immunität gegenüber Single Event Upsets (SEU) sowie das Verhalten nach einer Lebenszeit-Dosis zu evaluieren. Der SEU-Wirkungsquerschnitt wurde mit einem Protonenstrahl hoher Intensität gemessen. Die Ergebnisse zeigen eine signifikante Verbesserung der SEU-Immunität des STS-XYTERv2 im Vergleich zu seinem Vorgänger und erlauben eine Abschätzung der erwarteten SEU-Rate im Regelbetrieb des kompletten STS mit weniger als einem SEU/ASIC/Tag. Die Untersuchungen zur Gesamtdosis (total ionizing dose, TID) zeigen einen Anstieg des ASIC-Gesamtrauschens am Ende der Lebensdauer um ca. 40 – 60%. Darüber hinaus konnte gezeigt werden, dass kurze Ausheilungsabschnitte (annealing) bei Zimmertemperatur einen positiven Einfluss auf das Rauschverhalten des Chips haben.

Der Zusammenbau und Test der STS-Module, ein komplexer Prozeß mit mehreren Bauabfolgestufen und einer langen Lernkurve, ist in mehreren Abschnitten dieser Arbeit dargestellt. Einer diskutiert die Tests der ersten Prototypmodule mit Frontend-Boards vom Typ B (FEBs-B), die in der Lagen sind, jeweils 128 Kanäle auf der p- bzw. n-Seite des Sensors auszulesen. Diese Untersuchungen wurden mit einem relativistischen Protonenstrahl von 1.7 GeV/c Impuls am COSY-Beschleuniger, Forschungszentrum Jülich, im März 2018 durchgeführt. Diese Strahlzeit brachte wertvolle Erkenntnisse für ein effektives Erdungs- und Spannungsversorgungsschema der Detektorauslese. Das Signal-zu-Rauschen-Verhältnis wurde für eines der Prototyp-Module gemessen, mit Werten grösser 15 für beide Signalpolaritäten.

Ein Vorläufer des STS-Detektors, genannt Mini-STS (mSTS), wurde innerhalb des mCBM-Projekts im Rahmes des "FAIR Phase 0"-Programms gebaut. Die erste Ausbaustufe des mSTS besteht aus 4 vollständigen Dektormodulen. Um die Funktionalität der beim Modulbau verwendeten ASICs sicherzustellen, war es nötig, eine rigorose Prozedur zur Qualitätskontrolle zu entwickeln. Ein dedizierter Aufbau unter Verwendung einer speziell entworfenen "Pogo-Pin"-Station wurde gebaut und insgesamt 339 ASICs getestet. Der Anteil funktionierender ASICs guter Qualität betrug mehr als 90%. In der mCBM-Strahlzeit im März 2019 wurden 4 STS-Module mit einer nahezu finalen Auslesekette erfolgreich betrieben und wertvolle Daten genommen. Der mSTS-Detektor war den Reaktionsprodukten von Ag+Au Kollisionen bei 1.58 AGeV und Wechselwirkungsraten in der Größen ordnung von 10^6 ausgesetzt, was den Bedingungen im realen CBM-Experiment entspricht.

Im Verlauf dieser Arbeit wurde entscheidender Fortschritt bei der Entwicklung der STS-Detektormodule erzielt. Techniken zur Charkterisierung der Front-end Elektronik und des ganzen Detektorsystems wurden entwickelt und erarbeitet. Sie werden bei der Qualitätskontrolle in der bevorstehenden Modul-Serienproduktion für das STS Detektorsystem angewendet werden.

Chapter 1

Introduction

The understanding of the evolution of the universe has always been a fundamental question in the center of all scientific research. With the progress in technology during the last century, sophisticated devices were developed capable of accelerating particles at higher and higher energies, others to look further in the stars. Nowadays, modern physics can quantitatively describe phenomena ranging from the scale of leptons and quarks (10^{-15} m) to the scale of astronomical objects (10^{26} m) based on our understanding of the four fundamental forces of nature: electromagnetism, gravity, strong and weak interactions. Probing the laws of nature at incessantly finer scales has revealed the existence of a surprisingly large number of elementary particles and provided the means to study their interactions and thus to understand their relationships.

The efforts and contributions from thousands of physicists since the 1930s have resulted in a remarkable insight into the fundamental structure of matter: everything in the universe is found to be made from a few basic building blocks called fundamental particles, governed by four fundamental forces. Whereas gravity is described by Einstein's general relativity theory, the other three forces can be described to an excellent degree by the quantum field theory of quarks and leptons based on a framework consistent with the Einstein's special theory of relativity and quantum mechanics, the Standard Model.

1.1 The Standard Model

The Standard Model, developed in the early 1970s, is currently the most successful theory of elementary particles and their interactions. It has explained almost all experimental results and precisely predicted a wide variety of phenomena. Over time and through many experiments it has become established as a well tested physics theory.

There are seventeen named particles in the Standard Model, organized into the chart shown in Fig. 1.1. Fundamental particles are either the building blocks of matter, called fermions, or the mediators of interactions, called bosons. Fermions follow Fermi-Dirac statistics, and obey the Pauli exclusion principle. These particles occur in two basic types called quarks and leptons. Each group consists of six particles, which are related in pairs, or "generations". The lightest and most stable particles make up the first generation, whereas the heavier and less-stable particles belong to the second and third generations. All stable matter in the universe is made from particles that belong to the first generation; any heavier particle quickly decays to more stable ones.

Three of the fundamental forces at work in the universe result from the exchange of force-carrier particles, which belong to a broader group called "bosons" and follow Bose-Einstein statistics. Particles of matter transfer discrete amounts of energy by exchanging bosons with each other. Each fundamental force has its own corresponding boson: the electromagnetic force is carried by the photon, and the W and Z bosons are responsible for the weak force and the strong force is

carried by the gluon. The physical quantity which is responsible for the strong interaction is color, which comes in three instances: red, blue and green, and the corresponding "negative" units ("anti-red","anti-blue" and "anti-green"). Quarks (antiquarks) carry only a single positive (negative) unit of color, while gluons are bi-colored, i.e. they carry one positive and one negative unit of color. The strong interaction between quarks is transmitted via gluons, which carry only a discrete number of colors (gluons do not have mass, charge or flavor which are another set of fundamental properties distinguishing elementary particles); therefore the strong interaction can only modify the color of the interacting quarks by a discrete amount. The underlying fundamental theory of strong nuclear interaction is called after these facts as Quantum Chromodynamics (QCD).

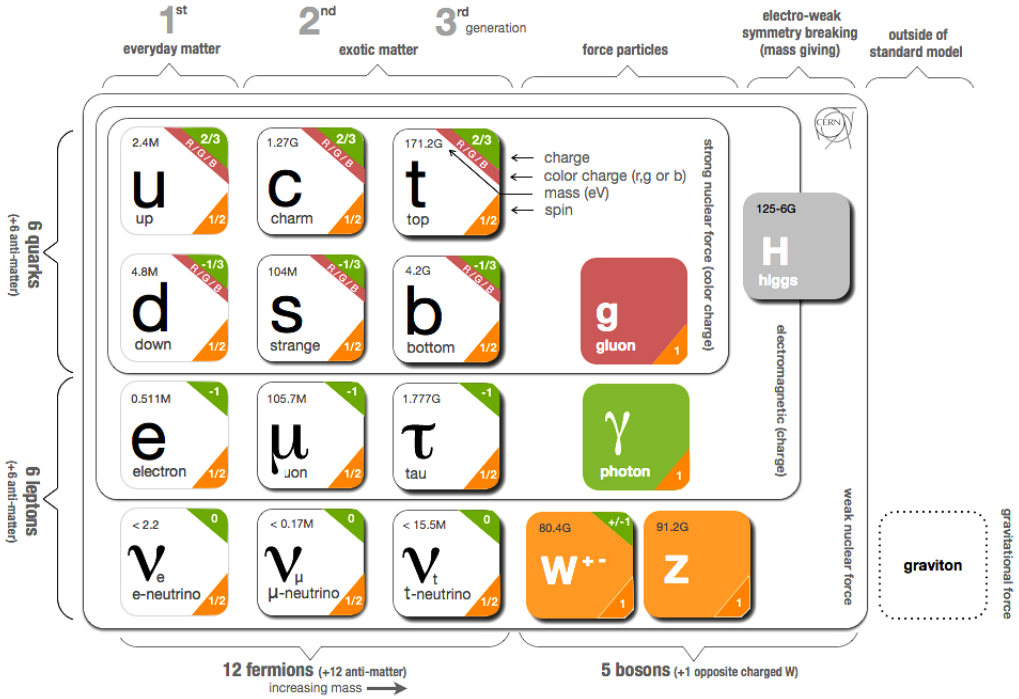


Figure 1.1: *Schematic depiction of elementary particles in the Standard Model [1].*

There are two fundamental phenomena associated with QCD. The first one is *confinement*, which refers to the experimental observation that quarks and antiquarks can not be found isolated in nature. Namely, quarks and antiquarks are found only confined in hadrons, the composite objects they form. This is a consequence of the constant force between the color charges, as they are separated, resulting from the self interaction of gluons, as they also carry charge. The second fundamental property of QCD is the *asymptotic freedom*, which states that quarks interact weakly at large energies (or equivalently at short distances). As the distance between quarks in hadrons increases, their interaction energy increases as well, which prevents the quarks from hadrons to be separated. Analytically, confinement is unproven, however, Lattice QCD calculations predicted that under certain conditions the confinement of quarks in hadrons vanishes, forming a new state of matter, the quark-gluon plasma (QGP). The quarks and gluons can move freely in the region where a QGP exists, on the scales larger than the size of hadrons (approximately 10^{-15} m). The nuclear matter under such extreme conditions may exist also nowadays in the interior of compact

stellar objects like neutron stars.

As every field theory of particle physics, QCD is based on certain symmetries of nature, deduced by observation. Chiral symmetry exists as an exact symmetry only in the limit of vanishing quark masses [2]. However, the actual quark masses and the strong interaction of quarks and gluons cause the explicit and spontaneous breaking of chiral symmetry, responsible for the generation of hadron masses. Chiral symmetry is approximately restored when quark masses are reduced from their large effective values in hadronic matter to their small bare ones at sufficiently high temperatures and energy densities.

1.2 Quark Gluon Plasma (QGP)

Based on the phenomenon of asymptotic freedom, it was expected that a new state of nuclear matter containing deconfined quarks and gluons, if ever managed to be produced in the laboratory at high temperatures and energy densities, should exhibit properties similar to a weakly interacting gas and its dynamics would have been described by kinetic theory. On the other hand, what was discovered at RHIC[1] and LHC[2] [8] exhibits totally opposite behavior: it turned out that hydrodynamic description of the QGP works reasonably well, which indicates discovery of a nearly perfect fluidity of the QGP and, in turn, strong coupling nature of quarks and gluons.

At near-zero net-baryon density, calculations on non-perturbative Lattice QCD predict the phase transition to occur at about an energy density of 1 GeV/fm^3 and a critical temperature of $T_{crit} \approx 170\ MeV$. This deconfined state of matter is believed to have existed approximately 10 μs after the Big Bang.

The QGP exists only for a short period of time ($\sim$ 10 fm/c $\approx 10^{-23}$ s) as an intermediate state in the heavy-ion collision and therefore can not be studied directly. Once the fireball expands and the density decreases, individual hadrons will form again. Nevertheless, the existence of the QGP has consequences for the dynamics of the medium and will influence the final particle spectra. Possible QGP signatures are anomalies in the flow [3, 4], J/ψ suppression [5], jet quenching [6] and variations in the strangeness production [7]. All these are indirect signals that get affected by the interactions in the hadronic medium. Further important signals are electromagnetic probes like photon and dilepton radiation, because they do not interact with the surrounding medium and leave the collision undisturbed [2, 8].

1.3 The study of the QCD phase diagram

The different phases of matter and their phase diagrams are among the most interesting and challenging fields of modern physics. Phase transitions are important for many different phenomena from ultra-cold atoms and solid-states to nuclear matter and cosmology. Especially the early universe features several phase transitions that are connected to the most fundamental aspects of physics like the separation of the four fundamental forces of nature or the decoupling of photons. The phases of nuclear matter, described in terms of thermodynamical parameters temperature (T) and baryochemical potential (μ_B), are illustrated in Fig. 1.2. At low temperatures and chemical potentials, or equivalent baryon-net densities[3], the degrees of freedom are hadronic, i.e., neutrons, protons, mesons, etc. At high temperatures, hadrons melt and their constituents, quarks and gluons, form a new phase (QGP), in which the fundamental degrees of freedom are quarks and gluons. This is a very good approximation for the matter produced at mid-rapidity in the highest

[1] Relativistic Heavy Ion Collider

[2] Large Hadron Collider

[3] Baryon-net density $\rho_B \propto e^{\frac{\mu_B - m}{T}} - e^{\frac{-\mu_B - m}{T}}$

energy heavy ion collisions at RHIC and LHC, and an exceedingly good approximation in the early universe [9]. In these cases, ordinary hadronic matter forms via a continuous crossover as the liquid QGP expands and cools. This process happened in the universe during the first few microseconds after the Big Bang. In this region of the phase diagram the transition is expected to be a smooth crossover from partonic to hadronic matter [10, 11].

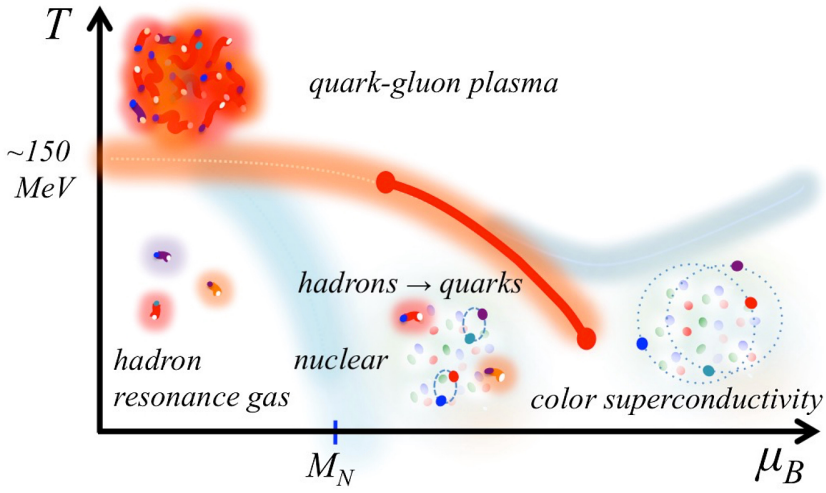


Figure 1.2: *Schematic phase diagram of dense nuclear matter, in the baryon chemical potential μ_B - temperature T plane [14].*

At moderate temperatures and relatively large baryon-net densities, a first order phase transition is predicted from hadronic to partonic matter, with a phase coexistence region in between. A new phase of so called quarkyonic matter [13] has been proposed to exist beyond the first order phase transition, which has properties of both high density baryonic matter and deconfined and chirally symmetric quark matter. Change of the transition nature between these two regimes of the phase transition is denoted by a critical point where strong fluctuations of the physical parameters occur. The nature of the transitions from hadronic to a QGP phase can be summarized as:

- crossover transition from the hadronic to quark-gluon plasma phase with increasing temperature, see Fig. 1.3;
- transition from nuclear to deconfined quark matter with increasing density, see Fig. 1.4.

Pushing to very high baryon-net densities while staying at low temperatures (squeezing nuclei without heating them) takes us into another interesting region of the QCD phase diagram. Matter that is sufficiently dense cannot be made of well-separated nucleons, even at low temperatures: the nucleons are crushed into one another. Because quarks attract each other, cold, dense matter in which quarks fill momentum space up to some high Fermi momentum is a color superconductor in which a condensate of correlated Cooper pairs of quarks creates a superfluid. This state of matter is called colour superconducting condensate, possibly existing in the interior of the neutron stars [15].

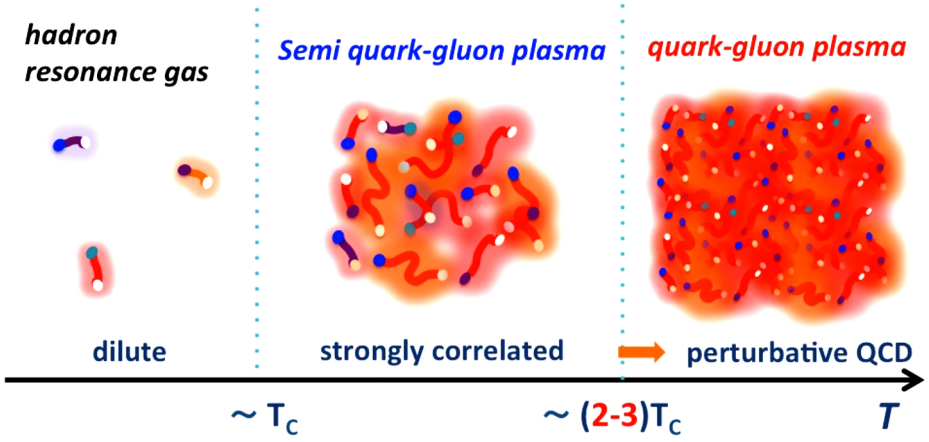


Figure 1.3: *1) For $T \lesssim T_{crit}$, the system is a dilute gas of hadrons; 2) For $T_{crit} \lesssim T \lesssim (2-3)T_{crit}$, thermally excited hadrons overlap and begin to form a semi quark-gluon plasma; and 3) for $T \gtrsim (2-3)T_{crit}$, the matter is percolated and a quasiparticle description of quarks and gluons, including effects of thermal media, becomes valid [14].*

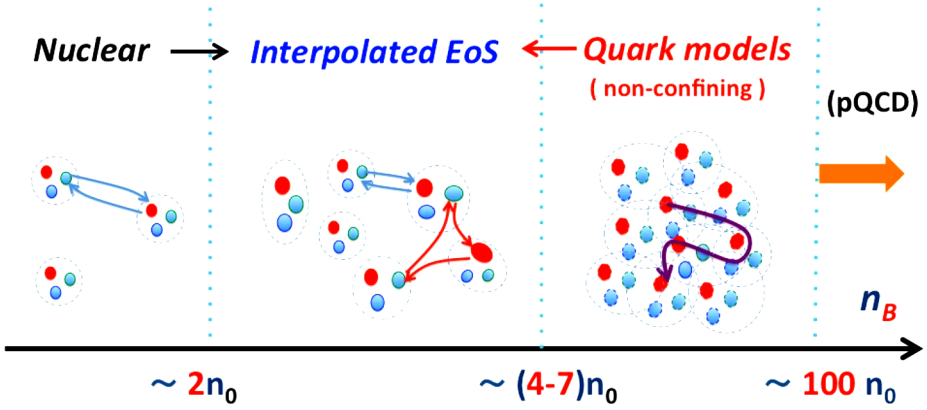


Figure 1.4: *1) For net-baryon densities $n_B \lesssim 2n_0$, the dominant interactions occur via a few (∼ 1-2) meson or quark exchanges, and description of the matter in terms of interacting nucleons is valid; 2) for $2n_0 \lesssim n_B \lesssim (4-7)n_0$, many quark exchanges dominate and the system gradually changes from hadronic to quark matter; 3) for $n_B \gtrsim (4-7)n_0$, the matter is percolated and quarks no longer belong to specific baryons. A perturbative QCD description is valid only for $n_B \gtrsim 10-100n_0$ [14].*

1.4 High baryon density at low temperatures in the cosmos

Neutron stars provide a cosmic laboratory in which the phases of cold dense strongly interacting nuclear matter are realized. The exception is at neutron star births in supernovae where temperatures can be tens of MeV, and in final gravitational mergers where hot and dense matter might be produced and temperatures could reach approximately 10^2 MeV [14]. While heavy ion collision experiments and Lattice QCD simulations provide insights into the properties of hot and dense QCD, neutron stars are the only known window into the rich structure of cold dense QCD [11, 15].

Compact stars are macroscopic objects ruled by the interplay of all fundamental forces in nature. Thereby the structure of the stars' interior is dominated by the strong force, which ultimately has

to counter balance the gravitational attraction. Typical compact-star masses are about 1.4 solar masses, while the radii are in the range of 10 to 14 km [16]. The central density can reach more than five times nuclear saturation density. Thus, the properties of such stars (e.g., mass, radius, moment of inertia, mass-shed frequency, tidal deformability, etc.) are largely determined by the equation of state (EoS) of highly compressed baryonic matter [14]. The temperatures in neutron stars are much smaller than 1 MeV (or 10^{10} K); matter in neutron stars lives essentially along the chemical potential axis in the QCD phase diagram, see Fig. 1.2. Therefore superfluid and/or superconductive states of matter are expected to appear inside such stars [11, 15].

In August 2017, the LIGO-Virgo Scientific Collaboration reported the milestone detection of gravitational waves (GWs) from a binary neutron star (BNS) coalescence, dubbed GW170817 [17]. This landmark discovery has opened a new era in astrophysics. Along with the GW detection, several telescopes also reported the observation of electromagnetic coincidence signals in various bands, inaugurating the birth of the GW multimessenger astronomy. The GW170807 event had a duration of approximately 100 seconds and was the result of two neutron stars colliding in a galaxy 130 million light-years from Earth. The localization of the sources of detected gravitational waves was significantly improved when LIGO information was supplied by VIRGO. The collision gave rise to two other major detectable phenomena: a short burst of X-rays and a transient optical near infrared source powered by the synthesis of large amounts of very heavy elements via rapid neutron capture (the r-process) [18]. One of the most relevant implications of this discovery is arguably the possibility of constraining the EoS of the neutron star core through the measurement of the tidal deformability of the binary components [19].

1.5 Probing QCD matter with heavy ion collisions

Heavy ion collision experiments at relativistic energies create extreme states of strongly interacting matter and enable their investigation in the laboratory. The main physics goals is to explore the QCD phase diagram, to discover the deconfined nuclear matter under equilibrium (QGP), and to understand its properties such as the EoS, temperature and order of the phase transition, transport coefficients, etc [20, 21]. The system produced in such collisions dynamically evolves within a time duration of the order of 10 - 100 fm/c.

Nowadays, several experimental programs are devoted to the exploration of the QCD phase diagram in different regions. Heavy ion programs at LHC in CERN and at RHIC in Brookhaven National Laboratory, have been running to explore the QGP at small baryon chemical potentials, where matter is produced with almost equal numbers of particles and antiparticles [22]. These studies, extensively developed at the LHC experiment, ALICE[4] [23] and STAR[5] at RHIC [24], have resulted in claiming that partonic degrees of freedom prevail in the early phase of the fireball evolution [11].

In order to search for features like the critical endpoint, the predicted first-order phase transition and the chiral phase transition, moderate temperatures and high baryochemical potentials must be achieved and experimentally accessed. High-energy heavy ion collision experiments worldwide are devoted to the investigation of strongly interacting matter under extreme conditions. The STAR Collaboration at RHIC has performed a beam energy scan (BES) from top energies down to $\sqrt{S_{NN}} = 7.7$ GeV [25]. In 2019, STAR has initiated the BES-II program, a dedicated low beam energy run for high precision measurements of observables that are expected to be sensitive to the phase structure of the QCD matter [26]. The collaboration will also extend the center-of-mass energy range ($\sqrt{S_{NN}} = 3 - 7.7\ GeV$) by means of a fixed-target program. At the CERN-SPS[6],

[4] A Large Ion Collider Experiment
[5] Solenoidal Tracker at RHIC
[6] Super Proton Synchrotron

the NA61/SHINE[7] experiment continues to search for the first-order phase transition by measuring hadrons using light and medium heavy ion beams [27]. At the Joint Institute for Nuclear Research (JINR) in Dubna, a heavy ion collider project (NICA) is planned with the goal to search for the coexistence phase of nuclear matter [28] at energies up to ($\sqrt{S_{NN}} = 11\ GeV$). Due to luminosity and detector limitations, these experiments are constrained to the investigation of bulk observables which are predominantly sensitive to the late and dilute phase of the collision when most of the particles freeze out. In contrast, the research program of the future Compressed Baryonic Matter (CBM) experiment [29] at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt [30] focuses on the measurement of diagnostic probes of the early and dense phase of the fireball evolution.

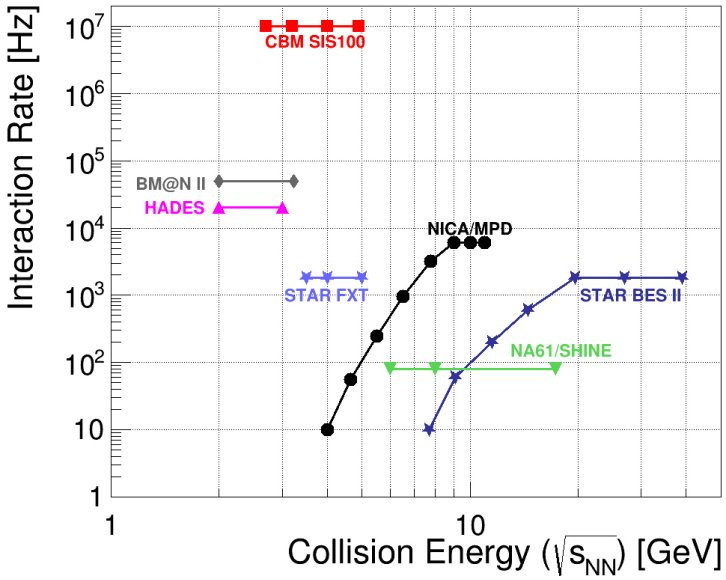


Figure 1.5: *Comparison of the interaction rates of existing and planned heavy-ion experiments as a function of the center-of-mass energy [31].*

The experimental discovery of landmarks like a first-order phase transition or a critical point in the QCD phase diagram would be a major breakthrough in our understanding of the strong interaction in the non-perturbative regime, with fundamental consequences for our knowledge on the structure of neutron star cores, chiral symmetry restoration, and the origin of hadron masses.

1.6 Motivation and scope of this work and thesis outline

The CBM experimental strategy is to perform systematic differential measurements of almost all particles produced in nuclear collisions, with unprecedented precision and statistics. The experiment will implement a novel readout scheme without hierarchical trigger. This novel concept requires fast, self-triggered and radiation hard readout electronics and a high-speed data preprocessing and acquisition system. The aim of this thesis work is the development and test of the front-end electronics of the main tracking and core detector of the experiment: the Silicon Tracking System (STS). The project focuses on the first component of the STS readout chain and its integration with the strip detector, with all required services and elements of the common CBM DAQ infrastructure used for data readout and detector control.

[7] North Area 61

The thesis is structured in six chapters, the current one has an introductory character, in which some fundamental concepts of the heavy ion collisions are briefly summarized. The second chapter introduces the physics program and main observables of the CBM experiment. In addition, it highlights the experimental challenges and the novel concept of a free-streaming readout chain. The final sections of the second chapter bring a detailed description of the STS detector, requirements, components design, physics performance and potentialities of the detector for particle identification based on the capabilities of its front-end electronics. The remaining chapters are organized as follow:

- Chapter 3 introduces the STS front-end electronics and its operation within a prototype readout chain. It summarizes the tests and results of the full chip characterization.
- Chapter 4 focuses on evaluating the radiation hard design of the STS front-end electronics in dedicated beam campaigns. The study allows to check the response of the chip after high irradiation doses and to evaluate how this could affect the operation of the final detector.
- Chapter 5 summarizes the results of a proton beam campaign dedicated to test the first STS prototype modules with the custom-designed front-end electronics. Several system aspects such as: overall noise, signal to noise ratio, powering scheme and system integration are presented and discussed.
- Chapter 6 covers the realization of a small-scale prototype of the STS detector for the activities of the FAIR phase 0. In the first sections of the chapter, the development and test of procedures for the quality assurance of the STS front-end electronics are illustrated. An important achievement was the built of the first fully assembled STS modules and their operation in realistic high-rate Ag+Au collisions at 1.58 AGeV.

The final chapter summarizes the fundamental results that have been presented and discussed across this work. The outlook section highlights the impact and contributions of this research in the next steps of the detector development and construction.

Chapter 2

The CBM experiment and the Silicon Tracking System

The CBM experiment is a next-generation experiment to be operated at FAIR, currently under construction in Darmstadt, Germany [30]. The CBM experiment proposes one of the richest and leading research programs in the field of heavy-ion physics. Its goal is to investigate the phase diagram of strongly interacting matter in the region of high baryon-net densities and moderate temperatures, employing high energy nucleus-nucleus collisions. A key feature of CBM is its very high interaction rate, exceeding those of contemporary nuclear collision experiments by several orders of magnitude [31]. The setup consists of a fixed-target forward spectrometer without a conventional, hardware-triggered readout; instead a novel free-streaming and online reconstruction concept will be implemented. The experiment is currently being developed by an international collaboration between institutes from Germany, Russia, India, Romania, Poland and other countries [29].

2.1 The future FAIR facility

The international FAIR facility in Darmstadt will provide unique research opportunities in the fields of nuclear, hadron, atomic and plasma physics [30, 32]. The heavy ion synchrotron SIS100[1] is the central part of the FAIR accelerator facilities. The accelerator tunnel has a circumference of 1084 meters and is being built with the possibility to accommodate, in the future, an additional synchrotron SIS300. The difference between the two synchrotrons relies in their magnetic rigidity of 100 Tm and 300 Tm, respectively.

FAIR will be one of the largest and most complex accelerator facilities in the world. It will have the unique ability to provide particle beams of all the chemical elements (or their ions), as well as antiprotons. These beams will support a broad field of research grouped mainly in four collaborations: APPA (Atomic, Plasma and Applications) , CBM, NuSTAR (Nuclear STructure, Astrophysics and Reactions) and PANDA (anti-Proton ANihilation at DArmstadt).

Figure 2.1 illustrates the existing (blue) and the future (red) installations of the FAIR facility. The existing GSI[2] accelerators will serve as the first acceleration stage for the SIS100/300 synchrotrons.

The research program devoted to the exploration of compressed baryonic matter will start with primary beams from the heavy ion synchrotron SIS100 [29]. The top energies of the SIS100 will be up to 29 GeV for protons and up to 11 AGeV for Au ions. Due to the slow extraction from the

[1] Schwerionensynchrotron (DE), Heavy ion synchrotron (EN)
[2] Gesellschaft für Schwerionenforschung GmbH

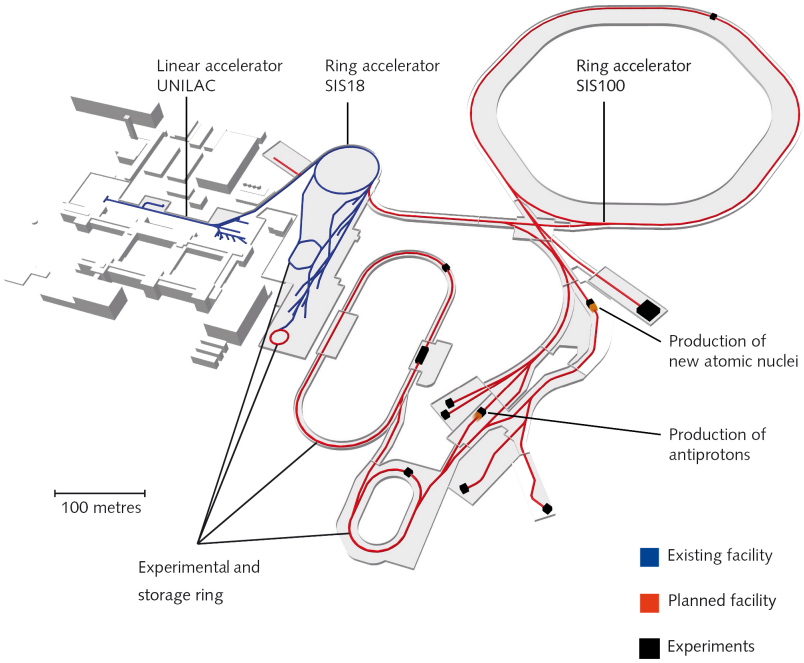


Figure 2.1: *Layout of the FAIR facility. Blue lines represent existing GSI facilities, the new accelerator complex is shown with red. The superconducting synchrotrons SIS100 or SIS300 will provide ion beams for the CBM experiment [30].*

synchrotrons, the beam at the CBM cave will have a continuous structure. This allows to increase the collision rate, since the beam particles will be uniformly distributed in time. The beam intensity is expected to be up to 10^9 ions per second resulting in 10^7 interactions per second using a 1% interaction probability in target.

2.2 The physics program of the CBM experiment

The rich physics program of the CBM experiment is devoted to explore the phase diagram of strongly interacting matter in the region of high-net baryon densities and moderate temperatures, employing high energy nucleus-nucleus collisions [11]. These studies, complementary to the experiments at SPS, BM@N[3] [28], HADES[4] [33], NICA/MPD[5] and STAR at RHIC [25], aim to investigate the EoS of QCD matter at densities similar to the densities in the core of neutron stars, and search for a possible phase transition from hadronic to quark-gluon matter, a critical point of the QCD phase diagram, existence of quarkyonic matter [13], and signatures of chiral symmetry restoration [9, 31]. However, due to luminosity or detector limitations these experiments can not measure rare observables with very low production cross sections and are constrained to the investigation of abundantly produced particles.

The high interaction rate of the CBM experiment opens the possibility to measure the rare probes and their properties with unprecedented statistics. The multiplicity of some probes is expected to be one in a million collisions or even less, as shown in Fig. 2.2. Figure 1.5 shows a

[3]Baryonic Matter at Nuclotron
[4]High Acceptance Di-electron Spectrometer
[5]Multi-Purpose Detector

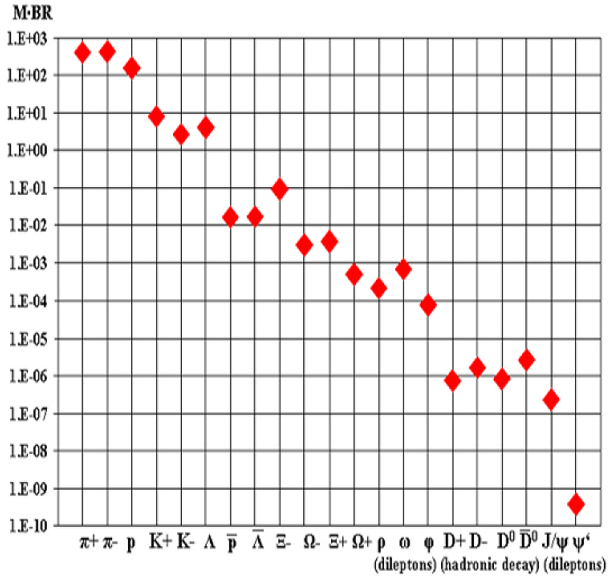
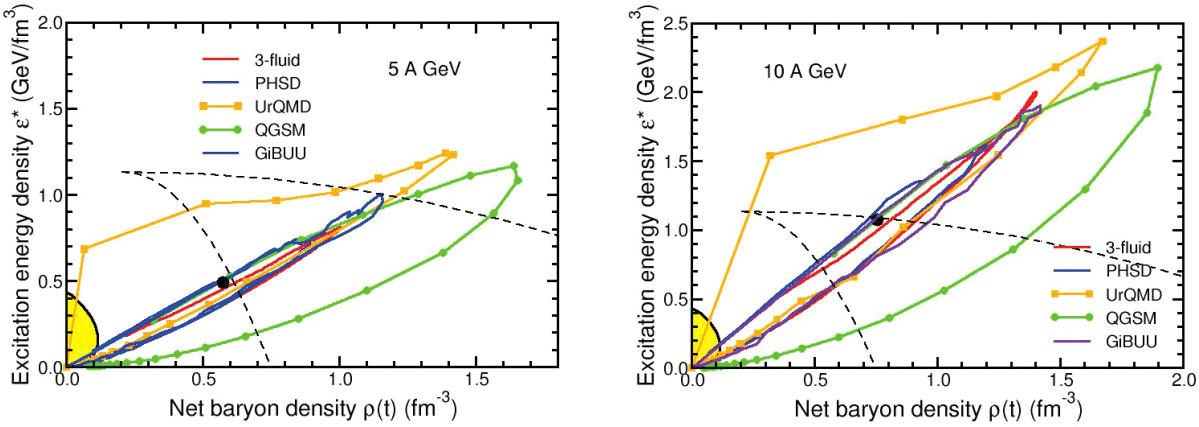


Figure 2.2: *Model predictions for yields (multiplicity × branching ratio) of probes intended to be measured by the CBM experiment.*

comparison of interaction rates and center-of-mass energies for different high energy experiments. Resting upon the fixed target approach and the large beam intensities, CBM aims to achieve unprecedented sensitivity in particle reconstruction [31].

To address these questions CBM will investigate collisions of heavy ion and proton beams, with fixed, heavy element targets, at beam energies from 2 to 11 AGeV (up to 14 AGeV for light nuclei and 29 AGeV for protons) [29]. Heavy ion collisions in this range of energies are ideally suited to explore the properties of dense baryonic matter. This is illustrated in Fig 2.3, where the excitation energy density in the center of the fireball, is shown as a function of the net-baryon density for central Au+Au collisions at beam energies of 5 A and 10 AGeV [11, 34]. This behavior is predicted by different transport models and a hydrodynamic calculation. According to the simulations, densities of up to 8 times saturation density can be produced already at beam energies of 10 AGeV. Under these conditions the nucleons overlap, and theory predicts a transition to a mixed phase of baryons and quarks. In addition, simulations show that the fireball spends a relatively long time in the phase coexistence (marked with dashed lines) at 5 AGeV and it emerges from it at higher energies. Time scale is extracted from UrQMD [35] and QGSM simulation, where every point in the evolution lines is equivalent to t = 1 fm/c [34].

Nowadays, the understanding of the properties of strongly interacting matter is mainly driven by new experimental results. Due to the complexity of the final state of heavy ion reactions, the extraction of significant information requires systematic measurements such as excitation functions, system size dependences, and multi-differential phase-space distributions of identified particles, including flow, event-by-event fluctuations, and other types of correlations. The most promising observables for a comprehensive study of the QCD phase diagram are here summarized.



(a) *Beam energy 5 AGeV* (b) *Beam energy 10 AGeV*

Figure 2.3: *Evolution of the excitation energy in the center of the fireball as a function of the baryon-net density calculated by different transport models and a 3-fluid hydrodynamics code. The Au+Au collision system is simulated for two different running scenarios, at 5 A and 10 AGeV.*

Collective phenomena

The collective motion of the final-state hadrons, resulting from heavy ion reactions, contains important information on the collision dynamics. The isotropic radial flow allows to characterize the collision system at kinetic freeze-out, i.e. when elastic collisions of the produced particles cease. Anisotropic flow results from the conversion of anisotropies in the density distribution into pressure gradients, and thus gives access to the equation of state of dense nuclear matter [36]. It can be described using a decomposition of the azimuthal distribution of the emitted particles in the plane transverse to the beam axis:

$$\frac{dN}{d\varphi} \propto 1 + 2\sum_{n=1}^{\infty} v_n cos[n(\varphi - \Psi_n)] \tag{2.1}$$

where N is the number of produced particles, φ is the azimuthal angle of each particle and Ψ_n is the n^{th} order symmetry plane. The coefficients v_n gives the magnitude of the flow-vector [3].

In order to conclusively address the degree of thermalization, the EoS and the in-medium properties of strange particles, multi-differential flow measurements for a large variety of hadron species, in particular strange hadrons and anti-baryons, are mandatory for a variety of collision systems and beam energies in the SIS100 energy range. The direct flow (v_1) is sensitive to the details of the phase transition, the softening of the QCD matter EoS, and it is also an important observable for clarifying the role of partonic degrees of freedom [4]. The strength of the elliptic flow (v_2) and its dependence on the particle transverse momentum can shed light on the degrees of freedom which prevail in the early stage of the collision. Moreover, the flow of strange particles and anti-baryons is determined by their in-medium potential and hence allows to address the restoration of chiral symmetry in the dense medium. The CBM experiment will significantly contribute to our understanding of the QCD matter EoS by measuring the flow of identified particles at FAIR energies, including multi-strange hyperons and di-leptons [31].

Event-by-event fluctuations

In the vicinity of the deconfinement phase transition, critical density fluctuations have been predicted to cause non-statistical event-by-event fluctuations of conserved quantities such as baryon number, strangeness and electrical charge. They are related to thermodynamical susceptibilities and therefore provide insights into the properties of matter created in high energy collisions [37]. Lattice QCD calculations suggest that higher moments of these distributions (skewness, kurtosis...) are expected to be particularly sensitive to the phase structure created in such collisions. The presence of a critical point is expected to lead to a non-monotonic behavior of these moments [37, 38].

Measurements of these fluctuations have been performed by other collaborations in order to search for the critical point. However, up to date no higher-order event-by-event fluctuations have been measured at SIS100 energies. The CBM experiment will carry out precise measurements of high-order fluctuations at various beam energies in the high net-baryon density range $\sqrt{S_{NN}} = 2.7$ - 4.9 GeV, corresponding to $\mu_B \simeq 800$ - 500 MeV [31].

Strangeness and hypernuclei production

High precision measurements of yields, momentum and angular distributions of multi-strange hyperons in nucleus-nucleus collisions at SIS100 energies, will allow to study the degree of equilibrium of the fireball. Strangeness production is an essential observable with possible connection to a phase transition. Systematic measurements of these observables as a function of collision energy appear a very promising strategy for the detailed investigation of the deconfinement phase transition [39, 40]. According to hadronic transport models, which do not feature a partonic phase, multi-strange hyperons are produced in sequential collisions involving kaons and lambdas; therefore they are sensitive to the density of the fireball. In addition, excited hyperon states can be identified.

Replacing an *up* or a *down* quark with a *strange* quark in a nucleon, which is bound in a nucleus, leads to the formation of a hypernucleus. A new quantum number, strangeness, is introduced into the nucleus, adding a third axis to the nuclear chart. The measurement of single and double hypernuclei opens the possibility to study the third dimension, and provides insights into the hyperon-nucleon and hyperon-hyperon interaction, which play an important role in the understanding of the structure of neutron stars [16]. Thermal model calculations show that the maximum of the hypernuclei excitation function is at FAIR energies. This is due to the superposition of two main effects: the increase of light nuclei production with decreasing beam energy, and the increase of hyperons production with increasing beam energy [41]. In contrast to the methods used before for the production of hypernuclei using K^- beams and light nuclei as target, CBM experiment intends to produce double-hypernuclei in heavy ion collisions via coalescence of Λ hyperons with nucleons or light nuclei in the final stages of the reaction [31].

Open and hidden charm

The yields of charmed hadrons are sensitive probes to the state in the fireball on the initial state of the collision. Due to its large mass, $c\bar{c}$ pairs can be produced only in hard processes, at the early stage of the nucleus-nucleus reaction. Depending on their interaction with the medium (hadronic or partonic), charm and anti-charm quarks hadronize into D mesons, charmed baryons, or charmonium [42].

At SIS100, hidden and open charm measurements can be performed in proton-induced reactions using proton beams with energies close to the production threshold (up to 29 GeV) and different targets. Open charm measurements address the understanding of charm production near threshold, the properties of charmed particles at saturation density and their propagation in cold nuclear matter. Moreover, they constitute an important baseline for measurements in nuclear collisions.

The formation of charmonium states is another observable sensitive to the conditions in the fireball. In a deconfined medium, charmonium states are expected to dissociate into c and $\bar{c}$ quarks due to color screening effects. This has been the first predicted signature for the QGP formation [42]. A particular and challenging experiment is to study the J/ψ production in collisions of symmetric nuclei up to 15 AGeV, and below threshold in Au+Au collisions at 10 AGeV. For this specific observable, the CBM experiment will use very high interaction rates and a dedicated experimental configuration, optimized for the identification of J/ψ [31].

Dileptons spectroscopy

The search for signatures of chiral symmetry restoration, which is expected to occur at very high baryon-net densities and/or temperatures, is one of the most important goals of heavy ion collision experiments. An observable consequence would be the modification of hadron properties inside nuclei, or in hot and dense matter. The degeneration of the spectral functions of chiral partners, such as the ρ-meson and the a_1-meson is a consequence of the restoration of the chiral symmetry. While the a_1-meson is very difficult to measure in the nuclear medium, the in-medium spectral function of the ρ-meson is accessible via the measurement of its decay into lepton pairs [2]. Moreover, the excess yield of lepton pairs in the energy range (M$\leqslant$1 GeV/c) is sensitive to the temperature of the created matter and its space-time extension. The slope of the dilepton invariant-mass spectrum between 1 and 2.5 GeV/c directly reflects the average temperature of the fireball [8]. The precise measurement of the energy dependence of the spectral slope opens the possibility to measure the caloric curve, which would be the first direct experimental signature for phase coexistence in high-density nuclear matter [31].

Short lived vector mesons can decay into di-lepton pairs ($\rho, \phi, \omega \rightarrow e^+e^-, \mu^+\mu^-$) which interact with particles in the collision region only via electromagnetic interaction. Dileptons are emitted from the fireball during all stages of the collision. Since they do not further interact with the surrounding medium, they offer the unique opportunity to look into the thermodynamical state of the medium at the moment of their production.

The CBM experiment will perform pioneering multi-differential measurements of lepton pairs over the whole range of invariant masses emitted from a hot and dense fireball. The experimental challenges are the very low signal cross sections, decay probabilities in the order of 10^{-4} and high combinatorial background [31].

2.3 The CBM experimental setup

The CBM experiment possesses a wide and challenging physics program that includes the study of multiplicity, distribution in phase space and flows of all interesting particles. Many of the important observables are rare diagnostic probes carrying the information of the dense stage of the fireball evolution [11]. To collect sufficient statistics, the experiment is planned to operate at reaction rates up to 10 MHz with a continuous (non-bunched) beam. Since most of the observables have complex trigger topologies, the experiment will implement a novel free-streaming readout mode [31]. Timestamped data from all detectors will be sent to a computing farm, where track reconstruction, event formation, and analysis will be performed online. The estimated data rate for the whole experiment in Au+Au collisions is approximately 2 TB/s in such experimental scenario. This represents a prohibitively data rate, therefore, fast algorithms for reconstruction and event selection will be performed in real time in order to reduce by two order of magnitude the stored data.

The CBM experiment has been designed as a multipurpose apparatus capable to register hadrons, electrons and muons in p+p, p+A and A+A collisions over the full FAIR beam en-

ergy range. The experiment has an angular acceptance between 2.5° and 25° to cover mid and forward rapidity hemisphere for symmetric collision systems over the energy range. It comprises the following subsystems:

- a dipole magnet for momentum measurements [43];
- a Micro Vertex Detector (MVD) to measure short-lived decay vertices and low-momentum particles;
- a Silicon Tracking System (STS) to provide tracking of charged particles and to measure their momentum;
- a Ring Imaging Cherenkov detector (RICH) to provide electron/pion identification;
- a Muon Chamber (MUCH) for muon identification and track reconstruction;
- a Transition Radiation Detector (TRD) to suppress pions and to support track reconstruction;
- a Time-of-Flight (TOF) wall for hadrons identification;
- an Electromagnetic Calorimeter (ECAL) for photon energy measurement;
- a Projectile Spectator Detector (PSD) for the collision centrality and event plane determination.

The CBM detector system can be used in two operation modes: the first one is optimized for electron identification (electron configuration) and the second is specialized for muon identification (muon configuration). In the first one, all the subsystems apart from MUCH will be involved. In the muon configuration, the RICH detector is replaced by MUCH and the electromagnetic calorimeter is removed. A schematic view of the detector-setup concept is shown in Fig. 2.4.

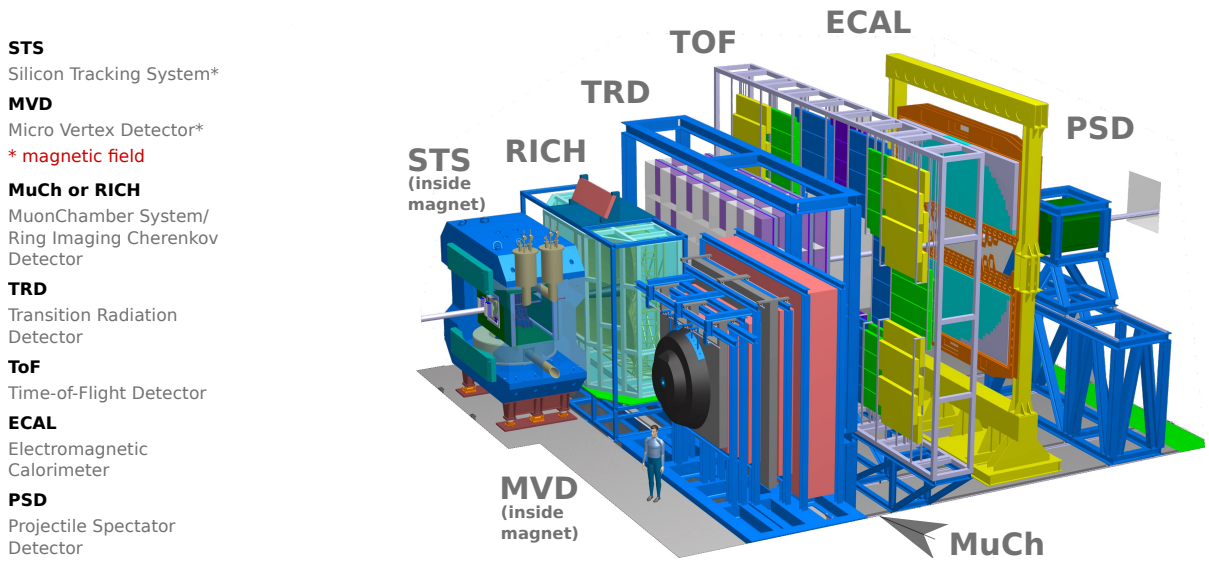


Figure 2.4: *The CBM experimental setup at FAIR.*

Table 2.1 summarizes the CBM subsystems used for registering the different particle types [44]. Below, each detector subsystem is briefly explained. The STS is described separately in the next section.

Table 2.1: *CBM detectors used for registering the different particle types are marked with ✓ symbol. Those subsystem that can also contribute to reduce the background are marked with (✓) [44].*

Particle	MVD	STS	RICH	MUCH	TRD	TOF	ECAL	PSD
π, K, p	✓	✓	(✓)		(✓)	✓		✓
Hyperons		✓			(✓)	(✓)		✓
Open charm	✓	✓	(✓)		(✓)	✓		✓
Electrons	✓	✓	✓		✓	✓		✓
Muons		✓		✓		(✓)		✓
Gamma							✓	✓
Gamma via $e^{\pm}$ conversion	✓	✓	✓		✓	✓		✓

Superconducting dipole magnet

The dipole magnet is one of the key devices used in the determination of the charged particle momenta in the CBM experiment. Its job is to bend the paths of particles emerging from the high-energy collisions. The more momentum a particle has the less its path is curved by the magnetic field, so tracing its path gives a measure of momentum. It magnet is designed to be superconducting in order to reduce the operation costs. It will provide a vertical magnetic field of 1 Tm from the interaction point to approximately 1 m downstream the target [43].

Micro Vertex Detector (MVD)

The main task of the MVD is to distinguish between primary and displaced vertices, for example, to reconstruct decays of charmed hadrons: D-mesons or Λ_c baryons. This task requires a high resolution along the position vector of approximately 70 μm, which turns to 5 μm spatial resolution and low material budget. The MVD is located directly behind the target (5 - 20 cm downstream) inside the dipole magnet. The MVD is placed in vacuum, thus it is able to reconstruct low-momentum tracks that helps to reject background for di-electrons [45]. The requirements of high spatial resolution, low material budget and high radiation tolerance are fulfilled with CMOS MAPS[6] with fine pixel size of several dozens of μm. Due to the limited readout speed, the MVD will participate only in data taking with interaction rates up to 10^5 Hz [45, 46].

Silicon Tracking System (STS)

The STS is a key detector of the CBM setup, responsible for tracking charged particle and provide momentum determination. The detailed description of STS design is presented in section 2.4.

Ring Imaging Cherenkov detector (RICH)

The RICH detector is designed to provide particle identification via Cherenkov radiation [47]. It allows separating electrons from pions up to 8 GeV/c with a pion suppression factor above 300 and electron identification efficiency above 85%. The RICH detector will be used in the electron-hadron configuration of the CBM setup. It will be located behind the dipole magnet, about 1.6 m downstream of the target. It will consist of a 1.7 m long CO_2 gas radiator and two arrays of mirrors and photo detector planes. The design of the photo detector planes is based on

[6]Monolithic Active Pixel Sensors

MAPMTs[7] (Hamamatsu H12700) in order to provide high granularity, high geometrical acceptance, high detection efficiency of photons also in the near UV region and a reliable operation. Mirrors are constructed with a reflective $Al + MgF_2$ coating to direct the light to the high granularity photon detectors [47, 48].

Muon Chambers System (MUCH)

The MUCH system allows to identify muon pairs produced in high energy heavy ion collisions [49]. It consists of 5 layers of hadron absorbers and tracking detector planes between the absorber layers. The absorber layers consist of a 60 cm thick carbon plate followed downstream by four iron plates of 20 cm, 20 cm, 30 cm and 100 cm thickness, respectively. The tracking planes are based on GEM[8] [50] and RPC[9] detectors. The MUCH will be operated in different setup configurations by varying the positions of the absorber-detector combinations. MUCH system in combination with STS are the main detectors in the CBM experimental setup to study di-muon decay channels of vector mesons like ρ, ω, ϕ and J/ψ. Reconstruction of such particles requires an accurate muon identification [49].

Transition Radiation Detector (TRD)

The main task of the TRD is to identify electrons above momenta of 1 GeV/c and thus to extend the electron identification capabilities of the RICH detector above momenta of p$\sim$5 GeV/c. This identification has to be achieved with a pion suppression factor in the range 10 – 20, in order to allow for a measurement of dielectrons in the mass range from below the ρ and ω masses to beyond the J/ψ mass with a good signal-to-background ratio. The particle identification is based on the effect that ultra-relativistic charged particles produce transition radiation when traversing a boundary between media with different dielectric constants. Currently, the TRD is envisaged to be a system composed of one station with four layers. The station will be located at a distance of approximately 5 m from the target. To detect the produced radiation MWPC[10] will be used, operated with a mixture of Xe/CO_2 gases [51].

Time of Flight (TOF)

The main task of the TOF detector is identification of hadrons: pions, kaons and protons. Different types of particles can have the same momentum, but due to their different masses, they will have different speed. The TOF wall will cover an area of 120 m^2 built with MRPC[11], which provides a very high efficiency and an excellent time resolution of approximately 60 ps. The TOF wall will be placed at 6 m downstream the target (for SIS100 energies) [52]. Detector granularity is adopted according to variation of hits rate (from 25 kHz in the central region to 2 kHz in the periphery). In order to achieve the required rate capability, MRPCs are built using low-resistivity glass [53].

[7] Multi-Anode Photo-Multipliers
[8] Gas Electron Multiplication
[9] Resistive Plate Chambers
[10] Multi-Wire Proportional Chambers
[11] Multi-gap Resistive Plate Chambers

Electromagnetic Calorimeter (ECAL)

The main purpose of the ECAL is to identify electrons and photons and to provide measurements of their energy and position. It is a "shashlik" type calorimeter consisting of 140 layers of 1 mm lead and 1 mm scintillator material, with the cell size of 6×6 cm^2, that results in more than 4000 readout channels [54].

Particle Spectator Detector (PSD)

The projectile spectator detector is a forward hadron calorimeter, which will be used to determine the centrality and the orientation of the reaction plane. These collision parameters are of crucial importance for studying the event-by-event fluctuations. In addition, the flow analysis requires to measure the reaction plane in a way that does not involve the collision participants. PSD will measure the number of spectator nucleons. The PSD is a full compensating lead-scintillator calorimeter. It will consist of 44 modules of area 20×20 cm^2 each. The modules will be made out of 60 lead/scintillator layers. The scintillation light will be read out with MAPD[12] via wavelength shifting fibers [55].

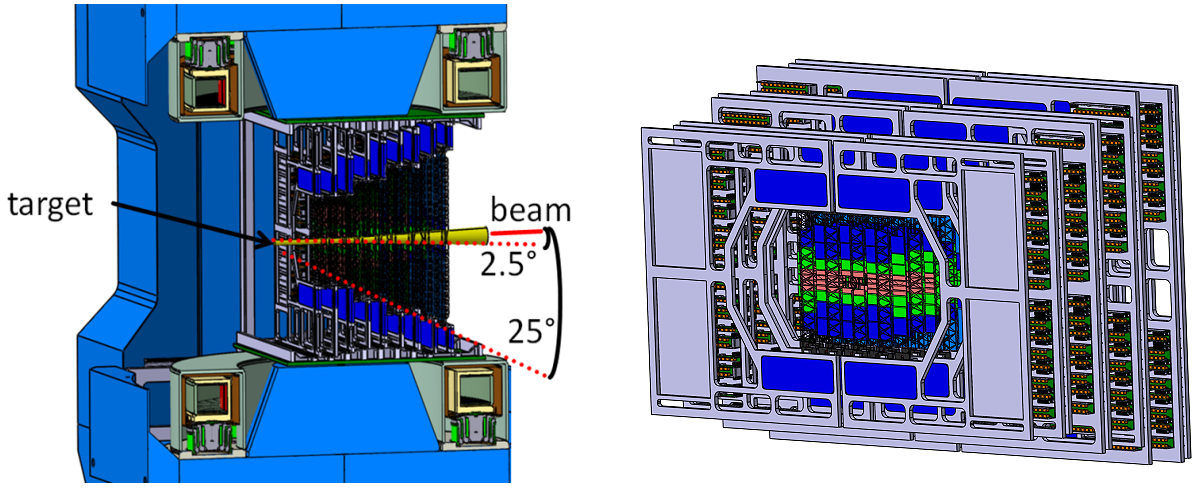
2.4 The Silicon Tracking System: challenges and design

STS is the main tracking detector of the CBM experiment. Its main task is to reconstruct tracks of charged particles with high efficiency (95% for p$\geqslant$1 GeV/c) and to measure their momenta with high resolution (1.5% for p$\geqslant$1 GeV/c). The STS consists of 896 double-sided silicon micro-strip sensors arranged in 8 tracking stations covering the physics aperture of $2.5^\circ \leqslant \Theta \leqslant 25^\circ$. The system, as shown in Fig. 2.5, is placed between 30 cm and 100 cm downstream the target, inside 1 Tm magnetic field [56]. It poses the most demanding requirements in terms of bandwidth and density of all CBM detectors and it also creates challenges that are unique compared to other silicon strip detectors commonly used in large high energy physics experiments. Some of the most important requirements to consider in the design of the system are listed below:

- the setup is contained in a volume of approximately $1.4 \times 2.3 \times 1.3$ m^3 inside the superconducting CBM dipole magnet;
- the detector must be capable of measuring up to 700 particles per central Au+Au collision at interaction rates up to 10 MHz without hardware trigger;
- since the momentum resolution is dominated by multiple scattering, the material budget of the STS has to be kept as small as possible;
- the system requires radiation hard silicon sensors, capable to withstand up to 10^{13} 1 MeV n_{eq} during the operation at SIS100;
- sensors will be readout using fast and self-triggered front-end electronics (FEE), which must keep a reliable performance in a radiation environment of up to 100 krad/yr [56];
- efficient cooling system, capable to remove up to 50 kW of dissipated heat from inside the detector box.

In order to minimize the multiple Coulomb scattering and to achieve a high momentum resolution, the STS tracker is required to have a low material budget. The front-end and readout electronics are placed in the periphery of the detector, out of the physics acceptance. Detector

[12] Multi-Avalanche Photo-Diodes



(a) *The STS inside the dipole magnet* (b) *Eight tracking stations for the STS detector.*

Figure 2.5: *Design concept of the STS. The detector is placed inside the superconductive dipole magnet between 30 cm and 100 cm downstream the target. The 8 tracking stations cover the physics aperture between 2.5° and 25°.*

modules are mounted on low mass carbon-fiber support structures [57]. Signals from sensors are transferred to the FEE via ultralight readout cables with up to 50 cm length. Such cable structure for a single detector module is equivalent to 213 μm of silicon [56].

The radiation tolerance is a vital quality specification for the silicon microstrip sensors due to the severe radiation conditions in the CBM environment. It is expected that the innermost sensors in the STS detector have to withstand a NIEL[13] damage up to 10^{13} 1 MeV $n_{eq}cm^{-2}$ and an ionizing dose around 1.1 Mrad during the SIS100 operation. The radiation hardness was confirmed up to twice the expected lifetime fluence [57, 58]. The sensor's charge collection efficiency decreases by 15 – 20% after irradiation to twice this level.

The STS detector is installed in a thermally isolated box that is inserted into aperture of the dipole magnet. This box serves as supporting structure for the STS and the MVD detectors, as well as the target and the beam pipe. During operation, a thermal power of about 50 kW will be continuously dissipated by the whole system. The front-end and readout electronics contribute with the largest amount (approximately 40 kW), while the rest is mostly generated by low voltage power cables, heat transfer via the walls of the STS box and a small amount from the sensors itself (approximately 6 mW/cm^2) [56].

The increase of the operating temperature leads to an increment in the detector leakage current. This has implication in the shot noise, which is proportional to $\sqrt{I_{leak}}$. In addition, the detector leakage current increases with the irradiation dose. Thereby, the excess of heat can cause the thermal runaway of the whole detector [59].

The task of the cooling system is to ensure that sensors are operated at a temperature not higher than -5°C. As the heat transfer inside the physics acceptance should be realized with a minimal amount of material, this induces usage of gas convection in the STS volume. At the same time, the humidity must be kept low to avoid condensation on the sensors. For the cooling of electronics, evaporative heat transfer based on CO_2 is chosen, because of its high volumetric heat transfer coefficient. The cooling blocks will be tightly connected to the boxes holding the FEE at the top and bottom sides of the STS [56].

[13]Non-Ionizing Energy Loss

2.5 The STS module as a functional unit

The functional building block of the STS is the detector module. It consists of a double-sided silicon sensor interconnected with two front-end boards (FEB) via ultra-thin microcables. Each sensor side has 1024 strips and is connected to a FEB carrying 8 custom-designed ASICs[14]. Groups of 128 strips are bonded to a pair of microcables carrying the analog signals to the FEE [56].

According to their position in the final detector, modules with different form factors (sensor sizes and microcables length) will be produced. A total of 896 modules, mounted onto 106 carbon-fiber ladders will populate the 8 tracking stations. Figure 2.6 shows a prototype of detector module. The main components are described in the next sections.

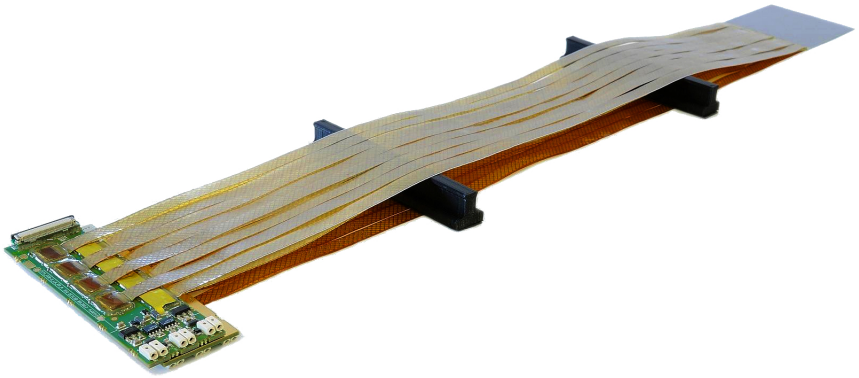


Figure 2.6: *The detector module is the functional building block of the STS. Every module consits of a double-sided silicon sensor, connected via a double stack of microcables to the FEBs.*

2.5.1 Silicon sensors and microcables

Silicon microstrip sensors have been successfully operated in many large experiments of high energy physics [60, 61]. The STS, like the inner tracker of the BELLE II experiment, will be populated with double-sided silicon microstrip sensors [62]. The sensor technology used in STS has been chosen to optimize the detector performance in terms of track reconstruction efficiency and low-mass requirement. These are important considerations for good momentum resolution and track matching with the upstream (MVD) and downstream (RICH, MUCH) detector systems. Double-sided microstrip sensors have the advantage of the (projective) space-point determination in the same amount of silicon material, while sensors segmented into strips on one side only require twice the sensitive material for this task [56].

The strips on the *n-side* of the sensor will be at the right angle with respect to the sensor edges, while on the *p-side* the strips will be inclined by 7.5°. This allows to keep the number of ghost hits at minimum, while still enables sufficient resolution in the direction along-the-strip. The stereoangle of 7.5° results in having shorter strips at the edges of the sensor. The short-length strips are interconnected with each other using a second metalization layer on the sensor [58].

Sensors are produced on 320 μm thickness *n-type* wafers, by Hamamatsu Photonics K.K. Each sensor side has 1024 strips (two interconnected short-length strips in the *p-side* are counted as one), positioned with a pitch of 58 μm. The sensors will feature integrated AC-coupling, in order to avoid the need of the leakage current compensation circuitry in the FEE. The sensors have been

[14] Application Specific Integrated Circuit

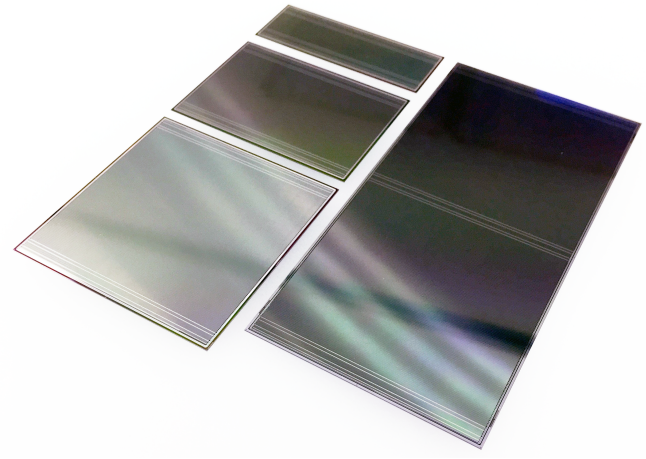


Figure 2.7: *The CBM06 silicon sensors family for the tracking system. Sensors will be produced with the same width of 6.2 cm and four different strip lengths (2.2 cm, 4.2 cm, 6.2 cm and 12.4 cm), matching the track densities in the STS detector.*

designed on a common base layout in four different strip lengths, matching the particle densities in the STS detector region of their deployment.

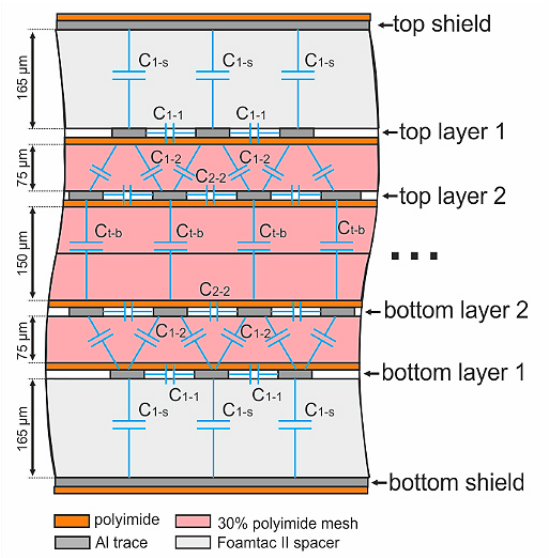


Figure 2.8: *Cross section of a stack of readout microcables. The diagram illustrates the effective capacitances between the different cable layers [56].*

Low-mass microcables are used to transfer signals from the sensors to the front-end electronics, which are mounted in the detector periphery due to material budget constraints. They are covered with a shielding layer in order to reduce the electromagnetic interference and noise level. For the signal transmission, two layers of microcable with aluminum strips and 116 μm pitch are used. They are separated with a meshed spacer in order to reduce the parasitic inter-layer capacitance, see Fig. 2.8. The supporting material for the aluminum strips is 20 μm polyimide.

2.6 The STS readout chain

The STS readout chain needs to assure all the control and readout functionality required by the system and sufficient data throughput to store all relevant information. In spite of the fact that technical details and solutions vary significantly between facilities and experiments, the common requirements of the communication between FEE and higher-level data aggregation systems remain similar:

- clocking the FEE;
- triggering (if applicable) or enabling data acquisition and synchronization of FEE;
- reliable commands transfer to the FEE;
- high-throughput output links for the experiment data.

The very high interaction rates, required to achieve the CBM physics program, impose strong constraints on the detector performance and the Data Acquisition (DAQ) system capabilities. CBM will implement a free-streaming DAQ, which means that no hardware trigger (level 0 or level 1 in typical systems) will be available. The full experiment is a combination of self-triggered FEE, fast free-streaming data transport, online event reconstruction and online event selection [63, 64].

In a free-streaming system, without a global trigger, each readout layer must decide by itself which data should keep. For the FEE, this represents a self-triggered mode in which any signal crossing a defined threshold is digitized, timestamped with a common clock and stored in a first buffer. For the readout components, each layer of the transport network has to read all the data and push them through the network depending on the status of its own buffer(s) or coarse information about the network status [65]. No decisions, in terms of higher level trigger, are taken during these phases. Figure 2.9 presents the general readout chain scheme for the STS detector. The major components are:

- front-end board (FEB) carrying 8 readout ASICs [66], which are connected to the strip sensors. The ASICs implement the analog front-end, the digitizer and the generation of individual hit data with ADC[15] and timestamp information. They provide an electrical interface (LVDS[16]) to the readout;
- readout board (ROB), based on the CERN GBT[17] ASIC [67], for data aggregation from multiple FEBs and the optical readout interface to ship data out of the detector volume [68];
- common readout interface (CRI) for data preprocessing, timing distribution and interface to slow and fast control. The CRI also serves as interface to the computing farm responsible for CBM data acquisition and event selection;
- first level event selector (FLES) responsible for time slice building, full event reconstruction and online event selection.

The STS readout chain will hold more than 14000 front-end ASICs, approximately 600 ROBs and 2400 optical links between the CRIs and the ROBs. With a signal rate of up to 150 kHz/channel the STS will produce about 300 - 500 GB/sec of data, which have to be read out by several thousand of high-speed optical links from the detector for further processing and data reduction.

[15] Analog-to-Digital Converter
[16] Low Voltage Differential Signal
[17] Giga Bit Transceiver

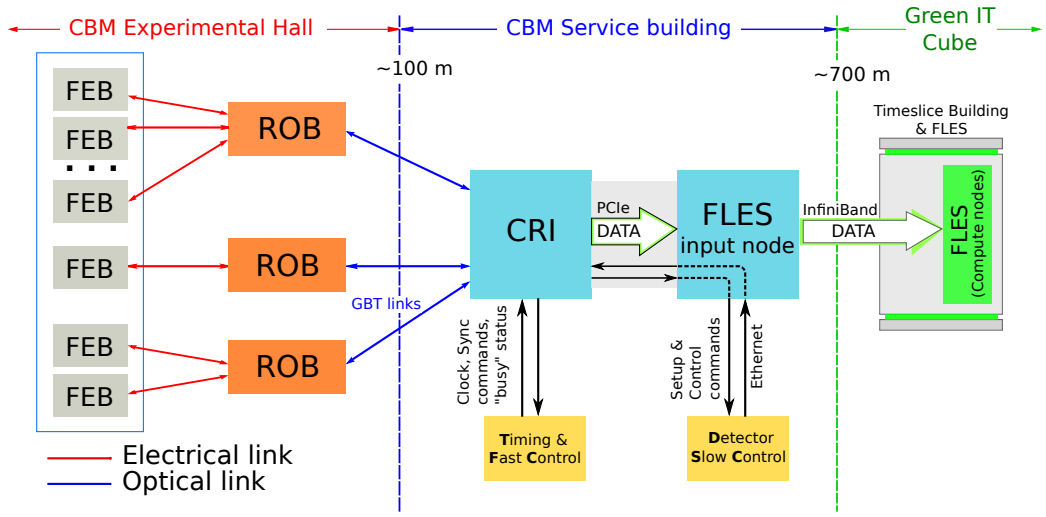


Figure 2.9: *Block diagram of the STS readout chain concept. Digitized data from the FEBs are aggregated in the ROB and shipped out from the detector box via high-speed optical links. The next stage in the data transmission line is the CRI, placed in the experiment service building, where data is preprocessed, clock and control commands are distributed. An efficient computer farm, located 700 m away from the experiment, will implement the online selection using high parallelizable algorithms. In numbers, the STS readout chain will consist of 1792 FEBs, approximately 600 ROBs and a total of 2400 optical links between the CRIs and the ROBs.*

2.6.1 Front-end electronics (FEE)

Signal read out of the silicon sensors will be performed by the custom-designed STS-XYTER (STS, X,Y coordinate, Time and Energy Read out) ASIC. The chips will be located at the end of the microcables which connect the detector readout strips to the first stage amplifiers. They will discriminate and digitize the signals on each sensor strip, further serialize the digitized data. The FEBs will be located at the perimeter of the detector stations and exposed to a radiation level up to 100 krad/year [56]; therefore the chip must also implement a radiation hard architecture. Further details regarding the STS-XYTER ASIC design, operation and performance are detailed in Chapter 3.

Different channel occupancies are expected for different areas of the detector. To enable sufficient bandwidth allocation, each ASIC can be configured to provide 1, 2 or 5 readout links at 320 Mb/s each depending on the expected local data load. This translates in realizing up to 5 LVDS pairs per ASIC, a high-density challenge for the FEB design and prototyping. All E-links will be AC-coupled in order to allow the connection of a single ROB to multiple FEBs, operated at the biasing potential of their respective sensor side. The boards will be stacked at the top and bottom layers of the detector ladders, mounted in a shelf structure that is in contact with a cooling plate to remove the power dissipated by the electronics. Due to the spatial constraints, the board dimensions are restricted to approximately 3 cm $\times$ 10 cm, as shown in Fig. 2.10. The FEB-8 also implements the last stage of power regulation, by using custom designed radiation hard linear regulators developed at at the Semiconductor Laboratory SCL Chandigarh, Department of Space in India [69].

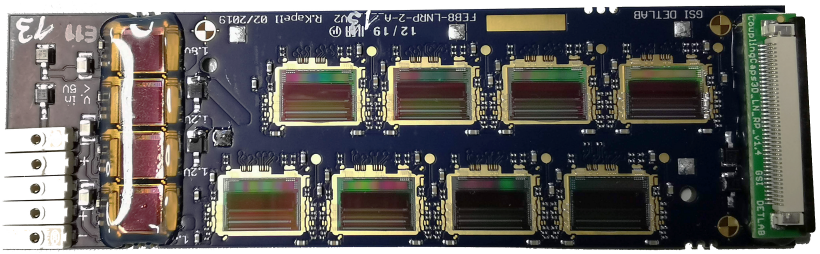


Figure 2.10: *Prototype design of the FEB-8 for reading out 1024 channels form the silicon sensors.*

2.6.2 Readout board (ROB)

The main purpose of the ROB is the data aggregation from many electrical readout links and multiple FEBs, together with the electrical-to-optical interface to connect the experimental area in the underground cavern to the CRIs on the surface. In addition clock as well as slow and fast control commands are distributed to the front-ends [70].

In the STS, ROBs will be placed out of the physics acceptance, but within the STS box, therefore, they will be exposed to very high radiation levels. The estimated irradiation levels over the full lifetime cycle of 10 years with 1 months of operation per year amounts to a Total Ionization Dose (TID) up to 1 Mrad and a NIEL up to 2×10^{13} n/cm^2. Consequently the ROBs are built using radiation hard components. In addition, they must also operate inside a 1 T magnetic field. These requirements are well within the specifications of the GBTX and Versatile Link devices.

A single ROB includes three GBTx chips. One chip operates in transceiver mode providing up- and down-links, while the remaining two operate in simple transmitter mode, providing only up-links. A GBT-SCA[18] will be used for slow control of the two GBTx configured in transmitter mode. The chips will be accompanied by the radiation tolerant optical transmitters (VTRx) and transceivers (VTTx) [67]. The GBTx ASIC provides bi-directional synchronous bit stream with constant latency between multiple front-end devices and the back-end system. The GBT widebus frame mode is used for the up-links in order to allow for maximum data throughput and number of available links. Operation without the forward error correction, provided in the GBT frame mode and the resulting error rate in the up-link data, is deemed acceptable especially in the case of the systems used for tracking in multiple layers which provide redundant information and can tolerate loss of individual hits or single misidentified hits [68].

The CBM Common Readout Board (C-ROB) is a common approach for all CBM GBTx based readout chains. It uses concepts, hardware, protocol and firmware solutions that can be shared among various readout chains to the largest possible extent. As an early prototype of the final ROB, it has a different form factor, and it includes other functionalities that are exploited during the testing phase. Figure 2.11 shows the existing C-ROB populated with the optical transceivers and the custom-designed ZIF-to-FMC card.

[18] Slow Control Adapter ASIC

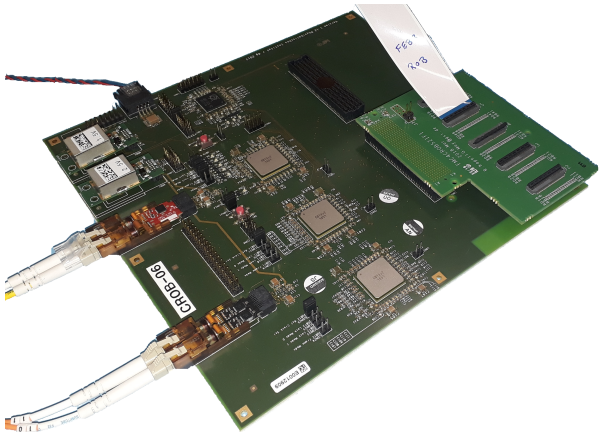


Figure 2.11: *The C-ROB is a common approach for all CBM GBTx based readout chains. The C-ROB is a predecessor of the final ROB. It includes three GBTx chips, a GBT-SCA ASIC and Versatile Links components.All components have a radiation hard design.*

2.6.3 Common readout interface (CRI)

The CRI is a common FPGA[19] hardware platform for CBM with system specific firmware [71, 72]. The CRI will implement the back-ends of the optical interfaces to multiple ROBs. This includes adaptations of the GBT-FPGA core and the back-end of the STS-XYTER communication protocol. Preprocessing of the hit data stream includes address expansion, time alignment of data from multiple sources and building of micro slices, which are data containers for all hit data created in a given time interval [68].

The CRI implements the interface to the Timing and Fast Control (TFC), which merges synchronization commands and fast control commands such as Start/Stop of the acquisition or throttling commands coming from the TFC master into the local down-link streams. In addition, it implements the interface to the detector control system (DCS) connected to the back-end of the communication protocol for the front-end ASICs.

As a preparatory step for the development of the CRI boards, a review of available hardware solutions for the PCIe[20]-based readout system is performed [72]. The results of this review allowed defining the viable configurations of the CRI boards and contributed to selection of the FLX-712 [73] board as the first prototype of the CRI board, see Fig. 2.12.

Even though the final solution for the CBM readout will be the CRI board, the Data Processing Boards (DPBs) are needed for developing and testing purposes [74]. They represent a multipurpose platform for prototyping the readout chain of different detectors. Every DPB flavor consists of a FPGA-based board, a custom-designed interface card to connect the FEE or the ROB, and a dedicated firmware. The hardware solution adopted by several CBM subsystems is based on the AMC FMC carrier Kintex 7 (AFCK) board [74, 75].

[19] Field Programmable Gate Array
[20] Peripheral Component Interconnect express

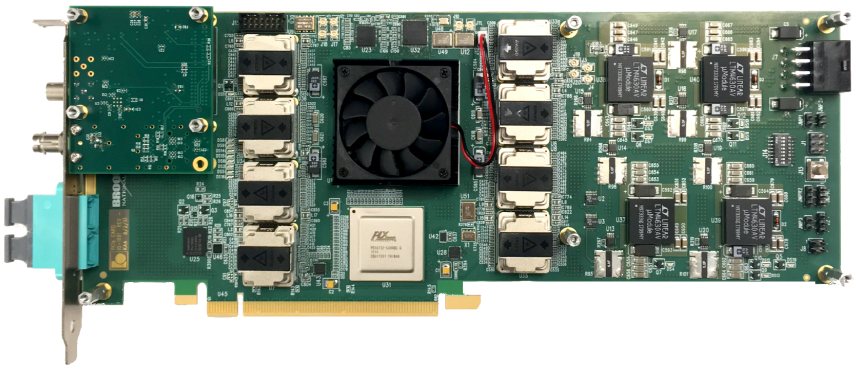


Figure 2.12: *FLX-712 board as the first prototype of the CRI board [73].*

2.6.4 First Level Event Selector (FLES)

For important signatures of the CBM physics case, such as Ω hyperons or D mesons, there are no simple criteria for collisions triggering and selection. The complicated decay topologies require the full reconstruction of the collisions, which imply a prohibitively long trigger latency [64].

The CBM data readout concept employs no hardware trigger, thus it will push all detector raw data to an online computing farm. For high interaction rates, the raw data volume has to be reduced by more than two orders of magnitude by online selection of physically interesting data. Based on the reconstructed signals, the collisions of interest will be selected and data stored on tape.

The basis for the online event selection will be fast and fully parallelize algorithms for reconstruction of hits, tracks and short-lived particles running on a high-performance, energy-efficient computer farm (GSI, GreenIT cube). The online CBM FLES will consist of nodes equipped with modern many-core central processing units (CPU) and graphic cards with the total power of about 60 000 CPU cores equivalent [76].

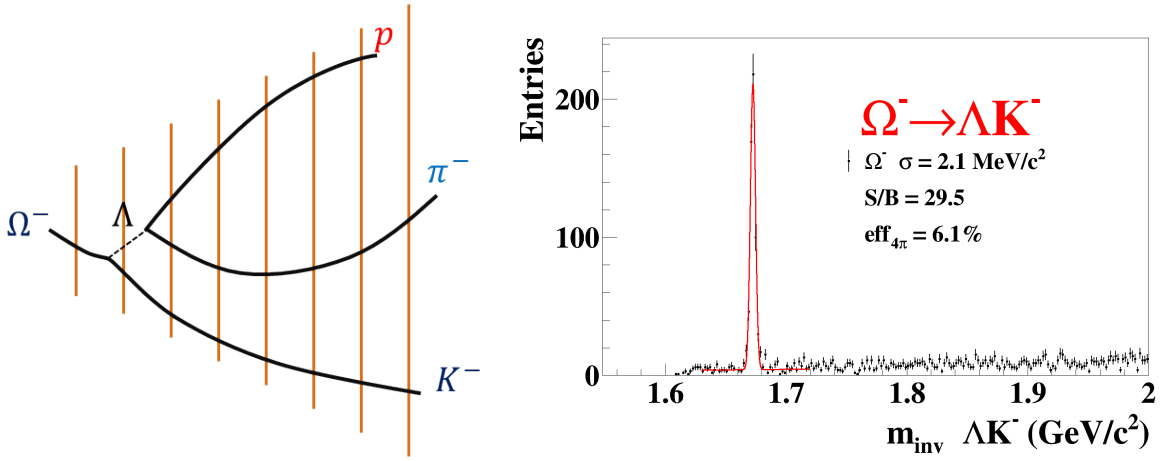
2.7 Challenging physics observables

As the core detector of the CBM experiment, the STS must reconstruct charged particle tracks with good momentum determination and high efficiency. Except for the case of neutral charged particles, STS intervenes in the registration of almost all CBM observables, as shown in Table 2.1. The track finding in STS, operated in an inhomogeneous magnetic field, is based on the Cellular Automaton method [77, 78]. A dedicated software package based on the Kalman filter [79] procedure is used for track fitting and reconstruction of primary and secondary vertices with the precision allowed by the granularity of the detector. Some of the most challenging physics cases for the STS detector are summarized below.

Particles with strange content

The precise reconstruction of weak decay topologies in order to measure strange and multi-strange hyperons is an important and challenging task for the STS. Since weak decays are characterized by long lifetimes of the mother particle, the decay vertex has a substantial distance to the primary vertex, therefore geometrical (distance of closest approach) and topological (back-pointing of the mother track to the collision vertex) cuts allow to substantially reduce the random combinatorial background from primary tracks. This procedure is repeated to reconstruct entire decay

chains such as Λ or Ω hyperons. Figure 2.13a illustrates the decay topology for the $\Omega^- \to \Lambda K^-$.



(a) Ω^- *hyperon decay topology.* (b) Ω^- *invariant mass spectrum.*

Figure 2.13: *Decay topology for* Ω^- *hyperon and their reconstruction in the STS. The invariant mass spectrum is generated after a simulated collision of 10 AGeV Au+Au nucleus using UrQMD. Secondary charged hadrons are identified by means of the TOF detector.*

The realistic detector response and track reconstruction have been goals of simulation studies for key physics observables of the CBM experiment. Performance of hyperon reconstruction has been studied in simulations. These studies use the UrQMD event generator as input for a realistic environment in terms of track multiplicities and phase space distributions. Rare signals like baryons or charmed mesons, which are either not produced with sufficient probability or not at all by the UrQMD model, are embedded on top of the UrQMD background events. Particles are transported through the detector material using the GEANT3 [80] transport engine. The reconstructed invariant mass spectra for the $\Omega^- \to \Lambda K^-$ decay is shown in Fig. 2.13b. Charged hadrons ($\pi^\pm, K^\pm, p^\pm$) produced directly on the fireball or as a result of a decay, will be reconstructed in the STS and identified by their time of flight in the TOF detector, placed approximately 6 m from the target.

Open charm case

For the measurement of open charm states like D mesons, STS will be operated together with the MVD. The same measurement technique, as described above, will be applied; however, the experimental conditions result more challenging in these specific cases, because of the extreme low multiplicity of D mesons (10^{-5} per collision), and short decay lengths ($c\tau$ = 312 μm for $D^\pm$ and 123 μm for D^0). Since tracks are first reconstructed in the STS and later on extrapolated towards the MVD, it is then crucial that the STS detector provides sufficient precision to find the correct hits.

Hyperons identification using the missing mass method

In the reconstruction of particles with strange content, a special challenge poses those hyperons where all decay modes have at least one neutral daughter, which can not be registered by the CBM detectors. Abundant particles, such as $\Sigma^\pm$, carry a large fraction of the strange quarks created in the collision. Their reconstruction, together with other strange-content observables, completes the picture of strangeness production and allows to compare yields of Σ and Σ^* for our specific experimental conditions.

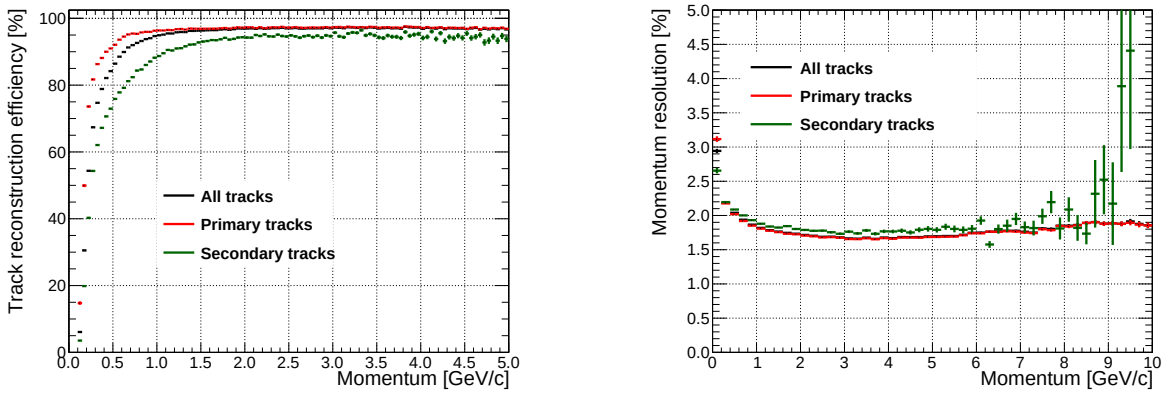
The STS in combination with the MVD detector provide adequate tracking capabilities for registering the Σ-hyperons. The "missing-mass" method, based on the conservation laws of energy and momentum, is proposed for their identification [81]. Even if the particle's lifetime is below 5 cm, the relativistic boost allows them to reach up to 15 - 20 cm. Since the first station of the MVD detector will be placed 5 cm downstream the target, the hyperons can cross 3 to 4 detector layers before decaying. In this case, the decay occurs inside the detector system, thus a charged particle produced in the decay can also be registered. A dedicated algorithm finds tracks of the Σ-hyperon and its charged daughter in the tracking system, and reconstruct the invariant mass of the neutral daughter. If the assumption that the Σ-hyperon mass is correct, a peak will result in the region of the mass of the neutral daughter; otherwise, it will form a continuous combinatorial background. Then the real mass spectrum of the hyperon can be generated from the charged and obtained neutral daughter [57, 82].

2.8 Performance simulations of the STS detector

2.8.1 Tracking reconstruction efficiency and momentum resolution

Among the examples described above, common requirements for the STS detector are high tracking efficiency and precise momentum resolution. Figure 2.14 shows the tracking performance of the STS evaluated by means of a realistic simulation. A sample of central Au+Au events at 10 AGeV, generated with the UrQMD event generator, is propagated through the multiple detector layers using GEANT3. The reliable model includes the detector geometry, the sensors response model and an accurate digitizer [83, 84].

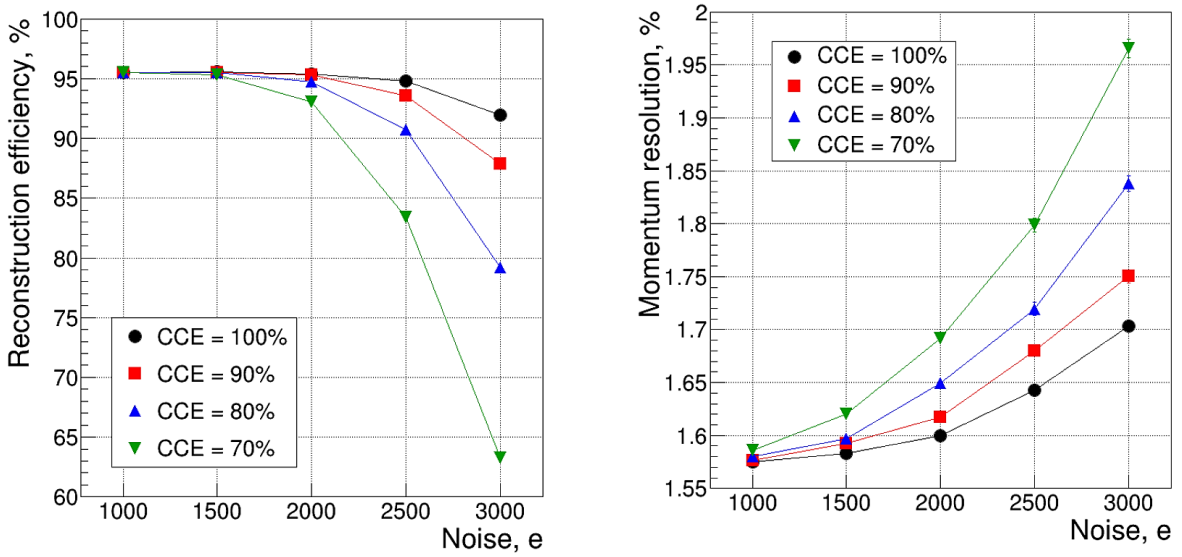
The tracking efficiency is determined as the ratio between the reconstructed tracks and those which are considered reconstructible. By definition, a track is considered reconstructible if it traverses the active area of at least four stations. The efficiency for primary tracks reaches a plateau of 97% above 1 GeV/c momentum, and for secondary, it is about 95% above 2 GeV/c. Momentum resolution is kept below 2% over a wide range of momentum. The drop of the efficiency at momentum below 1 GeV/c is caused by the low of number of charged particles that cross more than four stations.



(a) *Track recosntruction efficiency.* (b) *Momentum resolution.*

Figure 2.14: *Reconstruction efficiency and momentum resolution for different track sets as a function of their momentum.*

An important requirement for the STS detector is to achieve and maintain a signal-to-noise ratio (SNR) larger than 10 over the operation lifetime. This milestone is determined by the sensor charge collection efficiency (CCE) and the overall system noise. The SNR ratio has a strong influence on the tracking performance; therefore the simulated results shown in Fig. 2.14 could be assumed as an optimistic scenario for STS, since they were calculated assuming 1000 ENC(e^-) noise and a CCE of 100%. Figure 2.15, on the other hand, illustrates the detector performance for primary tracks of p$\geqslant$1 GeV/c as a function of the noise for different CCE values. The reconstruction efficiency is almost not affected by the CCE if the system noise is considerable low (below 1500 e^-). However, it significantly degrades if the noise level is in the order of 3000 ENC(e^-). This can be understood by the partial signal cutoff with the digitization threshold [84]. Higher threshold, worsens the hit reconstruction efficiency, which results in a decrease of the track reconstruction efficiency.



(a) *Track recosntruction efficiency.* (b) *Momentum resolution.*

Figure 2.15: *Reconstruction efficiency and momentum resolution for fast tracks (p $\geqslant$ 1 GeV/c) as a function of the overall system noise. Simulations are performed for different levels of (CCE) [84].*

2.8.2 Potentialities for particle identification using the STS detector

Particle identification based on the energy loss in a thin absorber can be implemented in a tracking system by studying the energy loss dE/dx as function of the measured ratio of particle momentum and charge p/q. In addition to the existing particle identification (PID) detectors in the CBM experiment, the contribution from STS can shed lights on some particular cases such as low momentum particles not registered by the downstream detectors, decays inside the STS, and particles with the same m/Z ratio, e.g. ^2H and ^4He, which can not be distinguished by means of a time of flight measurement alone.

The technique relies in the capabilities of the STS front-end electronics to discriminate in every channel, signals with amplitudes up to 14 fC using a 5-bit resolution flash ADC. The implementation of the dE/dx method has limitations in cases where the energy deposition in 300 μm sensor exceeds the chip dynamic range, e.g. for low momentum light ions. However, a simple discrimination threshold (signals above 70000 electrons) allows to identify light ions from single particles, see Fig. 2.16.

As a proof of concept, the dE/dx technique was tested using realistic simulations [72]. Figure 2.16 shows the separation power that can be achieved using the STS detector. Energy loss measurements allow to distinguish between single and double-charged particles over the whole momentum range. An example that illustrates the performance of the method is the reconstruction of ^{3}H. In this particular case, it is possible to improve the signal-to-background ratio by a factor of 50 compared to using only the TOF identification of the decay products. The method appears to be promising and is currently under development for its further implementation in the CBM software package as a PID tool.

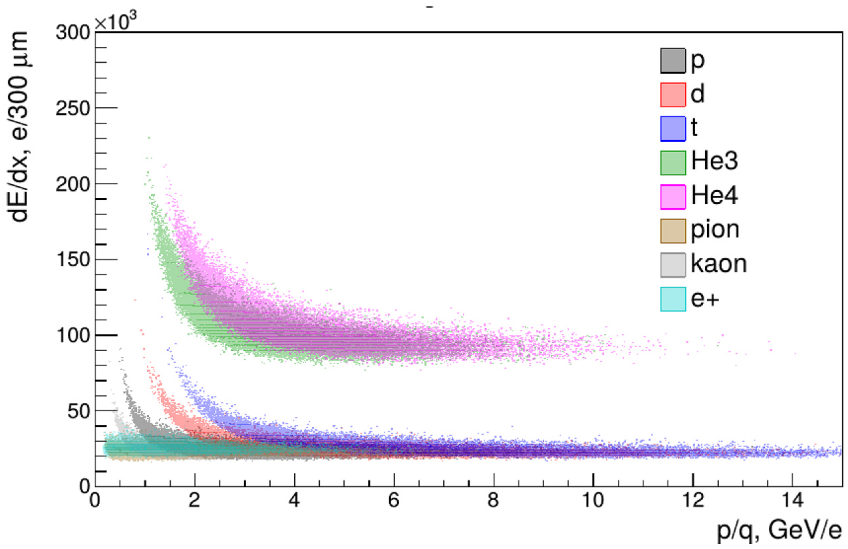


Figure 2.16: *Study of the particle identification potentialities using the STS detector [72]. The test of the dE/dx method yields promising results in the separation of single and double-charged particles.*

Chapter 3

Characterization of the front-end electronics for the STS

The STS-XYTER is a self-triggered, low-power integrated circuit (IC) optimized for the readout of the silicon sensors in the STS. The custom-designed ASIC comprises 128 channels with accurate time and energy measurement for both signal polarities. The chip must comply with many design requirements; it should perform reliably in a heavily irradiated environment, keep low power consumption, low noise levels and deliver unambiguous data at high transfer speed [85, 86]. Being a part of the first processing stage in the full readout and data acquisition chain, the characterization of the chip is a critical task. Moreover, for a coherent analysis of the readout data, amplitude and timing calibrations are required before operation.

This chapter aims to describe the methods established for testing and qualifying the readout chip. It is structured in multiple sections that describe the functionalities of the ASIC, the prototype readout chain and summarize the test results. Particular emphasis is put on to the development and test of the ADC calibration procedure and the quantitative estimation of the ASIC noise.

3.1 Requirements for the front-end electronics of the STS

The STS readout ASIC must comply with multiple requirements related to the sensor performance, the common readout chain of the CBM experiment and the different aspects of integration within the front-end board. The fundamental requirements for the ASIC are summarized in Table 3.1. Many design specifications are shared between the STS and MUCH systems. Therefore, it was decided to extend the functionalities of the STS-XYTER to satisfy the needs of the GEM detector readout as well.

Besides the elements described above, the chip must be radiation hard and have a self-contained architecture, requiring a small number of components (power supplies, LVDS terminations, bypass capacitors) [85]. It must be fast with a scalable digital interface and protocol compatible with GBTx-based data acquisition systems [65, 70, 87]. It should also provide testability features such as wafer-level probing, pogo-pin probing, built-in calibration systems, and other diagnostic options.

The STS-XYTERv2 is a compact multi-task IC, which combines several features optimized for the readout of silicon sensors. In addition to the challenging requirements of its design, it is also necessary to consider that higher integration levels, larger input capacitances and high rates do not only deteriorate the noise performance of the ASIC but also the accuracy of the signal measurement. Therefore, from the user point of view, a basic operational description of the chip is not sufficient, it is also necessary an extensive characterization of the analog front-end (AFE) and the full signal processing chain. Moreover, to exploit the full precision of the STS-XYTERv2 ASIC, the development of tools for accurate ASIC calibration and proper noise estimation are mandatory.

Table 3.1: *Key requirements for the STS and MUCH readout circuit [85].*

Detector system	**STS**	**MUCH**
Detector type	Double-sided silicon microstrip sensors, AC-coupled	GEM detector, triple stack
Sensor lengths	2.2 cm, 4.2 cm, 6.2 cm, 12.4 cm	
Microcable lengths	15 – 47 cm	-
Expected total capacitance	Up to 40 pF	Up to 50 pF
Number of channels/chip	128	64
Channel pitch	58 μm	116 μm
Power consumption	<10 mW/channel	
ADC dynamic range	0 – 15 fC	0 – 100 fC
Time measurement accuracy	<10 ns	
Signal polarity	Positive, negative	Negative
Operating temperature	-10 ℃	60 ℃

3.2 General description of the STS-XYTERv2 ASIC

The STS-XYTERv2 ASIC is fabricated in a UMC[1] 180 nm CMOS process. Due to the evolution of the experiment specifications and the requirements for reading out the GEM detectors of the MUCH system, it has undergone significant changes from its predecessor [85, 88]. It uses a redesigned set of input amplifiers, improved shapers, enhanced testing features, and a pad layout to meet specific conditions during the STS assembly procedure [85, 86]. Another major change came with the simplification of the back-end design to ensure its compatibility with a GBTx-based DAQ structure [70, 89]. A diagram of the ASIC and a view under the microscope are shown in Fig. 3.1

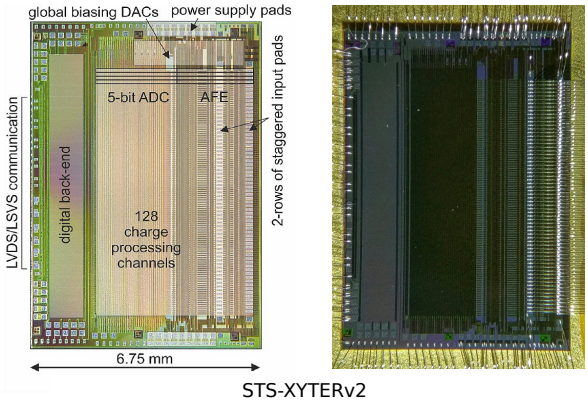


Figure 3.1: *STS-XYTERv2 ASIC simplified diagram (left) and a view under the microscope after wire bonding (right).*

[1] United Microelectronics Corporation

The chip includes 128 AFE channels with time and amplitude measurement circuits. Two additional test channels at the periphery of the ASIC, are provided with buffered outputs for the internal signals. It possesses full-custom configuration registers, common biasing blocks and calibration circuits. The digital back-end is clocked at 160 MHz, providing access to configuration registers, free-streaming digital readout, and multiple diagnostic features [90].

Figure 3.2 shows the block diagram of one channel of the STS-XYTERv2. The chip uses a low noise charge sensitive amplifier (CSA) to aggregate the charge generated in active volume of the detector and to convert it into a voltage step with amplitude proportional to the collected charge. The amplifier uses gain switching: 9.2 mV/fC (STS) and 1.6 mV/fC (MUCH) to address the different dynamic range requirements. The pulse passes then through the polarity selection circuit (PSC) to have a single pulse polarity in the processing stages and hence support the readout of a double-sided silicon sensor. Two parallel paths are used in the signal processing chain. A *fast* path, used for the determination of the signal arrival time, has been designed with a single stage CR-RC shaper of 30 ns peaking time, a comparator and a 14-bit timestamp counter operated at 320 MHz. The *slow* path has been optimized for low noise energy discrimination and measurement. It uses a two-stage amplifier with a CR-$(RC)^2$ characteristic followed by a 5-bit flash ADC. The *slow* shaper allows the selection of four different shaping times: 90, 150, 220 and 280 ns [85, 86].

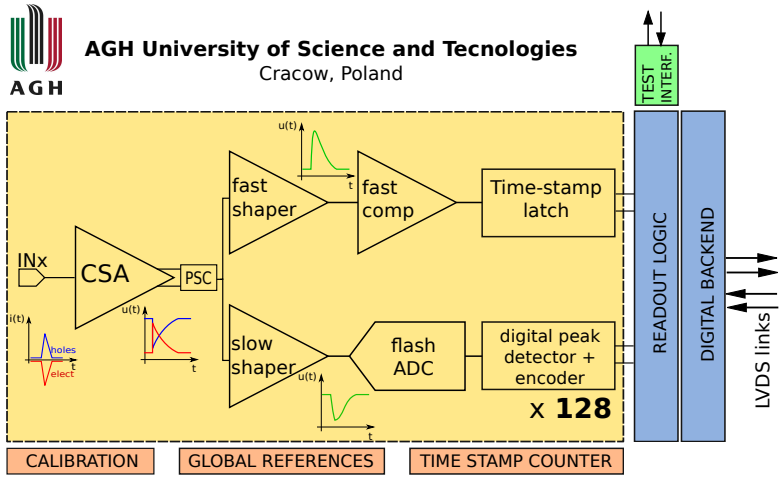


Figure 3.2: *A functional diagram of one channel of the STS-XYTERv2 ASIC. After the first pre-amplification stage, the signal splits into two branches optimized for time and energy measurements, respectively.*

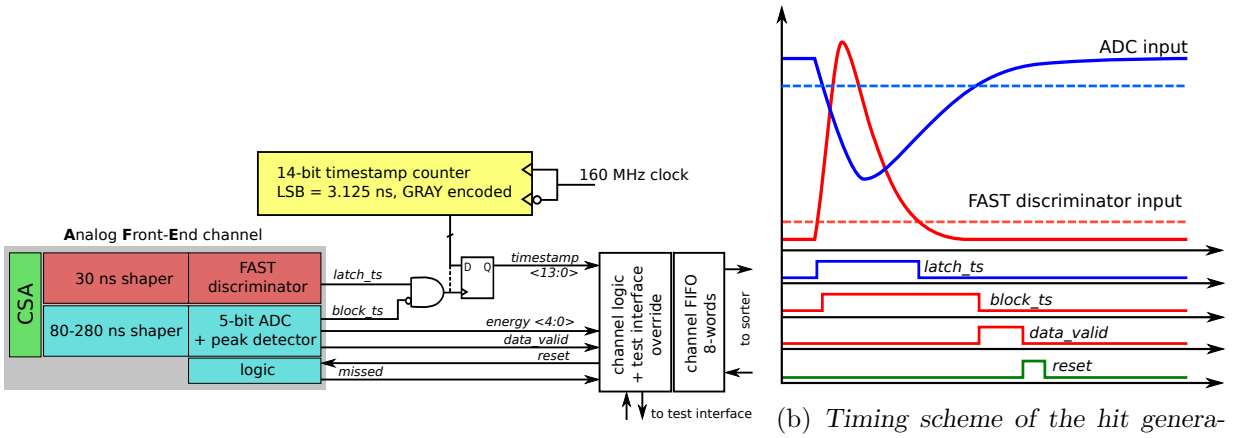
The back-end logic serves for register access and data readout. It additionally provides some diagnostic features like upset counter, a link error monitor and multiple modes of test hits generation. It incorporates five LVDS drivers that can be enabled depending on the expected channel occupancy [65, 90].

An efficient hit data transfer protocol, named STS-HCTSP[2], has been developed for use in the STS and MUCH detectors [65]. The synchronous protocol has been tested and ensures control request transfer in the ASIC direction with a speed of 2.6 Mframes/s. In the uplink direction, hit data transfer is achieved at 9.41 Mhit/s/link. Moreover, the protocol is compatible with the GBTx ASIC and the CBM DAQ structure [70, 89].

[2]STS Hit and Control Transfer Synchronous Protocol

3.3 Hit generation mechanism

When operating the STS-XYTERv2 in self-triggered mode, hit information is stored and latched by the arrival of every signal itself. The information contains 14-bit timestamp, 5-bit amplitude and 1-bit event missed flag. The data are generated by the two different signal paths: fast shaper and timing discriminator (time), slow shaper and ADC (amplitude). The hit generation mechanism, together with the time scheme are illustrated in Fig. 3.3a. It can be explained as follows: every time the fast comparator fires (including noise hits), new timestamp value is stored in the timestamp latch. Once a slow shaper signal crosses the lowest ADC threshold comparator, which typically occurs several tens of ns later, the timestamp latching is blocked by the *block_ts* signal. During next hundreds of ns, the signal driving the ADC reaches its peak amplitude and returns to the baseline. The peak detector keeps the maximum of the slow shaper output. As soon as the signal in the slow path falls below the lowest threshold discriminator, the *data_valid* flag is asserted and the hit data are ready to be written into the 8-word deep channel FIFO[3]. All signals are then synchronized with the back-end clock in the channels logic. If the channel FIFO is not full and the channel is not masked, the hit is written into the channel FIFO and the channel state is reset by the *reset* signal. The event-missed flag is asserted if in-between, a new hit occurs (excessive write time can be caused by a full FIFO). The successful acquisition of hit data requires correct AFE configuration, i.e., the timing discriminator threshold should be configured low enough to ensure latching of timestamp values whenever the first ADC discriminator is fired.



(a) *Hit generation mechanism.*

(b) *Timing scheme of the hit generation.*

Figure 3.3: *Schematic representation of the hit generation mechanism.*

[3]FIFO: First IN, First Out. Electronic circuits for buffering and flow control

3.4 Operation of the STS-XYTERv2 in a prototype readout chain

Towards the operation of the STS-XYTERv2 ASIC a test system was built at GSI laboratory. Initial chip characterization and testing of the STS-HCTSP readout protocol [91] was carried out. Figure 3.4 shows an image of the established set up and highlights the main components of the prototype readout chain. It includes:

- a prototype FEB carrying one STS-XYTERv2 ASIC;
- a data processing board (DPB), FPGA based board which implements the communication protocol back-end;
- a gDPB FMC mezzanine card, for interfacing the FEBs with the DPB.

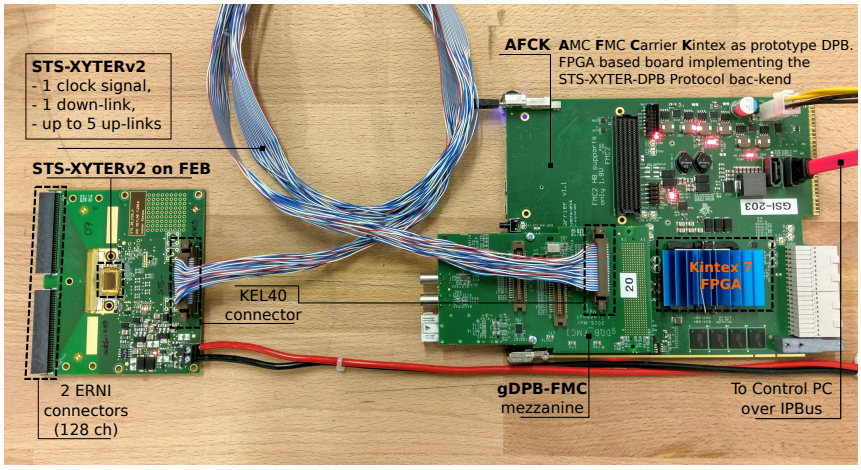


Figure 3.4: Prototype readout chain used for testing the STS-XYTERv2.

The prototype FEB-B is a custom-designed board for testing a single STS-XYTERv2 chip, see Appendix A. It contains two ERNI connectors (128 channels) for interfacing the detectors. A main low voltage line of 2.5 V powers the board, where low voltage linear regulators establish the potentials 1.2 V and 1.8 V required for the AFE operation and the 1.8 V for the digital part. In the FEB-B design, several analog spy points are routed to external connectors. The availability of such probes permits to monitor multiple analog signals as well as to check the reference biasing potentials.

The chosen hardware platform for implementing the readout back-end was based on the AFCK board [75], which is the development and prototyping platform for the CBM DPB boards. The firmware reuses the functionality of the STS protocol-tester [92], designed for standalone protocol test without ASIC. It has a modular design (Fig. 3.5) that implements in two separate blocks the STS-XYTERv2 model and the ASIC command controller. This design allows a fast transition from ASIC emulation to the real device tests. The communication with the controller back-end is provided by the IPBus protocol using a 1 Gbps Ethernet link [93]. The dedicated IPBus controller allows accessing the chip command processor and reading out the raw data FIFO. The STS-tester software is written in Python v2.7 to enable fast prototyping and the possibility of interactive work.

The test firmware has undergone significant upgrades according to the requirements for the data readout. However, a large number of tests were carried out using the full control path and the limited readout bandwidth. In addition, the simplicity of the firmware allowed to rapidly multiply the number of testing stations. For different applications, the functionalities of the tester firmware were considered sufficient; this is described in the next chapters.

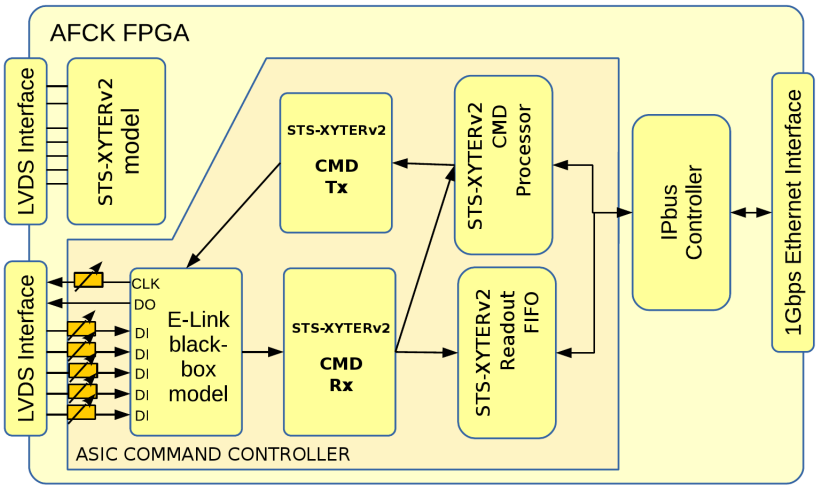


Figure 3.5: *Block diagram of the STS protocol-tester firmware. The modular design implements both the STS-XYTERv2 model and the ASIC command controller.*

3.5 ASIC operation and power consumption

The first step for bringing the STS-XYTERv2 into operation is to launch the procedure for synchronizing the communication link, hereafter mentioned as *synchronization*. This enables the communication with the ASIC, assuming that no correct time-phase between data and clock and incoming data is known. During the initialization phase, specific data frames are exchanged in the down-link and up-link directions. Depending on the chip response, the DPB adjusts the down-link clock phase and data delay to receive the message correctly [65]. After this step, the basic access is established and writing/reading actions in the control registers become possible.

Figure 3.6 shows the main settings in the ASIC operation. After the *synchronization* procedure, the chip requires a full register configuration. During this process, the 35496 bits for controlling the AFE are set, while in the digital part the number of enabled up-links, the channel masking, and the start value of the timestamp counter are established.

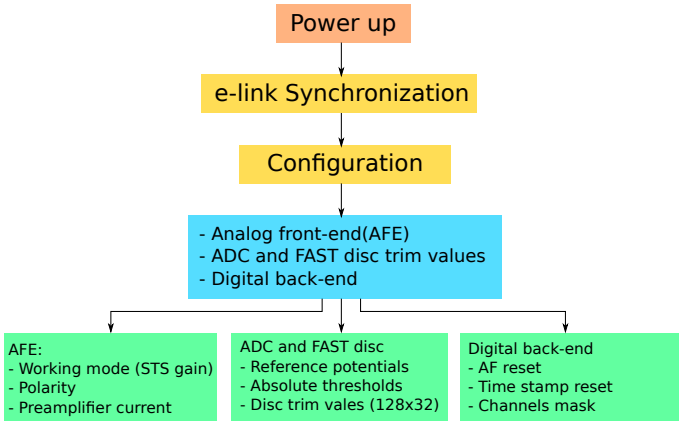


Figure 3.6: *Block diagram showing the main settings to operate the STS-XYTERv2 ASIC.*

Since the ASIC does not have a well-defined start-up configuration, its power consumption, and hence its temperature, will depend on the initial register values. Multiple readings of the chip

registers after repeated power-on show that these can assume any possible value. However, the power consumption is dictated mainly by the AFE biasing, more specifically by the current in the CSA. Figure 3.7 illustrates the current drawn by 339 ASICs in their initial state and after being fully configured. The distribution of the current after power-on is widely spread between 0.1 A and 0.8 A. The mean value of 0.5 A, has been measured in approximately 27% of the chips. After the *configuration*, the distribution has a small spread and an average value of 0.6 A, which can be considered as the typical current drawn by the ASIC [94]. This represents the first check in the ASIC tests, and might indicate if the chip performs well. Large current values might reveal problems in the readout, while lower ones could be an indication of no response of the AFE.

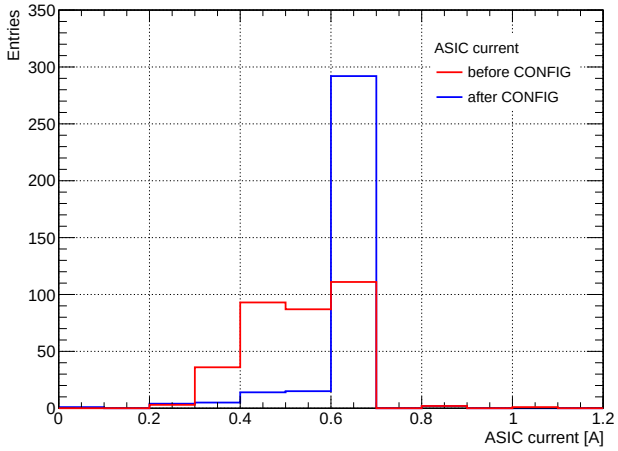


Figure 3.7: *Distribution of the drawn current in 339 ASICs before and after the configuration [94].*

3.5.1 Thermal behavior and monitoring tools

The dissipated power and the existing monitoring tools implemented in the STS-XYTERv2 ASIC are important features to test. Since the chip will not only be operated in a standalone FEB, but also as part of the highly integrated and compact FEB-8, the cooling aspect is one of the main concerns of the design. This is a valuable information for the next integration stage. Figure 3.8 shows thermal images taken from the FEB-B with the STS-XYTERv2 mounted. Every picture represents a different step in the operation chain of the ASIC:

a. after power on;

b. configured with typical register values;

c. maximum power consumption (largest current values of the CSA).

The images were taken with an infrared camera five minutes after setting the test configuration in order to assure a stable operation temperature. The upper panels represent views of the entire FEB. Two main hot spots can be distinguish in each one of them: on the left side the 1.2 V LDO[4], and in the center the STS-XYTERv2 ASIC. Temperature is measured in the cross point, and the automatic right scale indicates the different temperature range observed in the images. In the bottom of every picture it is indicated the absolute current consumption of the chip. The lower panel shows a close-up to the ASIC.

[4]Low Dropout Regulators

Due to thermal emissivity of the ASIC surface and the circuit board, the absolute temperature can not be properly measured. However, the images do illustrate a realistic heat map where not only the chip can be distinguished, but also other warmer spots such as the power LDOs.

It is expected that the chip should perform stable in the so-called typical working configuration (Fig. 3.8b), and hence limit the power consumption to moderate values. In this stage, the heat dissipated by the ASIC can be estimated by considering the operation current $I = 0.60\ A$ and the biasing potential $U = 2.50\ V$ of the FEB-B, $P \approx 0.60A \cdot 2.50V = 1.50\ W$. For a small laboratory system this might represent a reasonable value, however, it imposes significant challenges in the final STS system. Based on the obtained values, we could estimate in more than 20 kW, the dissipated heat by the front-end ASICs of 896 detector modules.

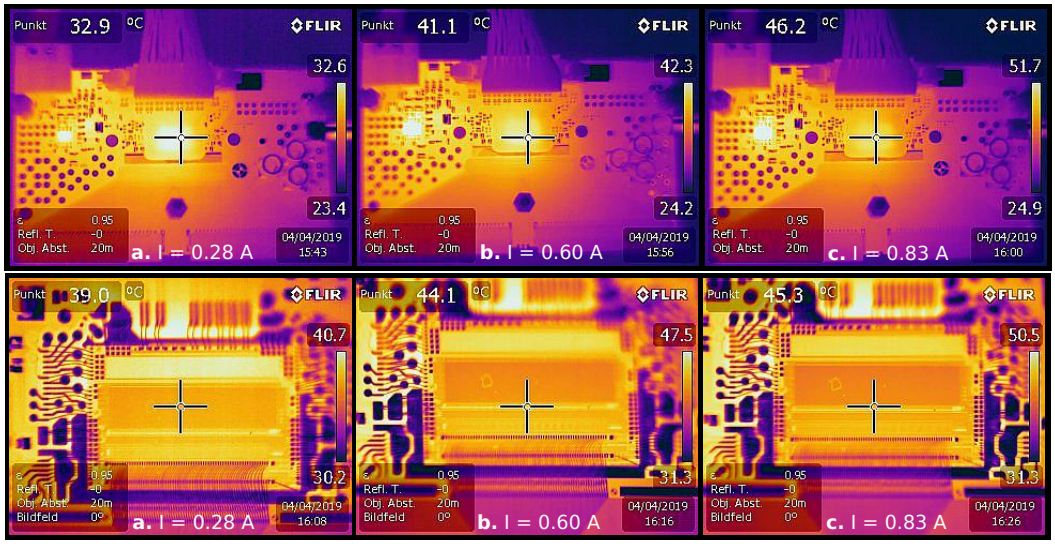


Figure 3.8: *Thermal images of the STS-XYTERv2 ASIC taken during different operation stages: a) After power start-up; b) Typical configuration loaded; c) Maximum current configuration.* ***Top****: ASIC in the prototype FEB-B.* ***Bottom****: Close-up to the STS-XYTERv2 ASIC.*

A thermal probe (*VTemp*) is one of the tools instrumented into the chip to survey its temperature during operation. It is foreseen that this feature will be part of a larger integrated diagnostic circuit to be implemented in revision 2.1 of the ASIC [95]. The STS-XYTERv2 possesses a simplified version with no readout access via the back-end. However, it is possible to monitor the temperature via an external pad in the ASIC. To check the performance and linearity of the *VTemp* probe, the chip was operated inside a thermal enclosure box. The temperature in the box was monitored using an external controller placed at the bottom of the FEB-B and in direct contact with the ASIC cooling block; this allowed an error margin of ±1 ℃.

By fitting the collected data with a linear function, the *VTemp* calibration parameters are extracted, see Fig. 3.9. The slope describes the voltage step created in the analog probe for a change of 1 ℃. According to the calibration it corresponds to -1.67 mV/℃, which is in agreement with the designed value of -2 mV/℃. At room temperature (27 ℃), the expected analog voltage is 660 mV, while the measured one corresponds to 685.9 ± 0.6 mV, resulting in a relative deviation smaller than 5%.

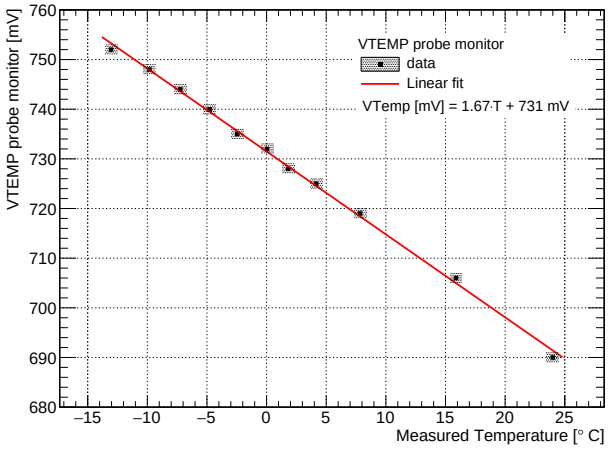


Figure 3.9: *Linearity check of the temperature probe VTemp placed as part of the STS-XYTERv2 monitoring tools.*

3.6 Characterization of the analog front-end (AFE)

The characterization of the STS-XYTERv2 ASIC is an extensive procedure carried out simultaneously across different institutes [91, 96, 97]. Functional tests such as proper amplitude and time calibrations are necessary to interpret the data correctly. This represents an essential step before using the chip in the readout of the silicon sensors. The characterization procedures are intended to check a large number of parameters that influence the chip performance. Some relevant parameters from the user point of view are discussed in the following sections.

In a first step, the analog waveforms are acquired using 1.5 GHz active probes connected to the test channels of the STS-XYTERv2. They are read out using a Tektronik 4054 oscilloscope. An arbitrary waveform generator with rising time $\tau_r = 1$ ns is used to provide the test pulses. Buffered signals from the test channels are routed to external connectors on the prototype FEB-B board, see Appendix A. Exemplary waveforms are acquired while the chip temperature is stabilized at 5 ℃. Figure 3.10 shows the response to a 85 mV negative pulse measured in 4 different stages during the signal's processing path:

- CSA (Signals directly after the channel CSA);
- PSC (CSA signals after the polarity circuity (always negative polarity));
- FAST shaper (Fast shaper signal (always positive polarity));
- SLOW shaper (Slow shaper signal (always negative polarity)).

The input signal polarity is only distinctive after the CSA stage. After the PSC, the polarity of the output signal is fixed. It always remains positive in the fast branch and negative in the slow branch. Both shapers employ amplifiers with input pMOS transistors and feature a gain bandwidth product of 1.3 GHz [85]. The signal on the slow path is shaped with a peaking time of 90 ns.

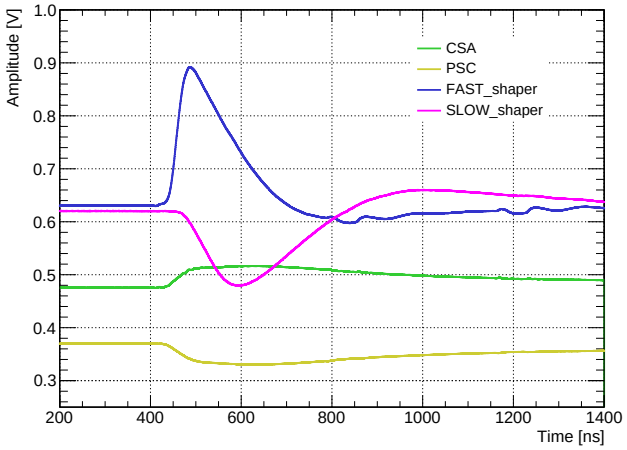


Figure 3.10: *STS-XYTERv2 ASIC waveforms from one test channel. Peaking time in the slow shaper is set to 90 ns.*

3.6.1 Slow and fast shapers gain estimation

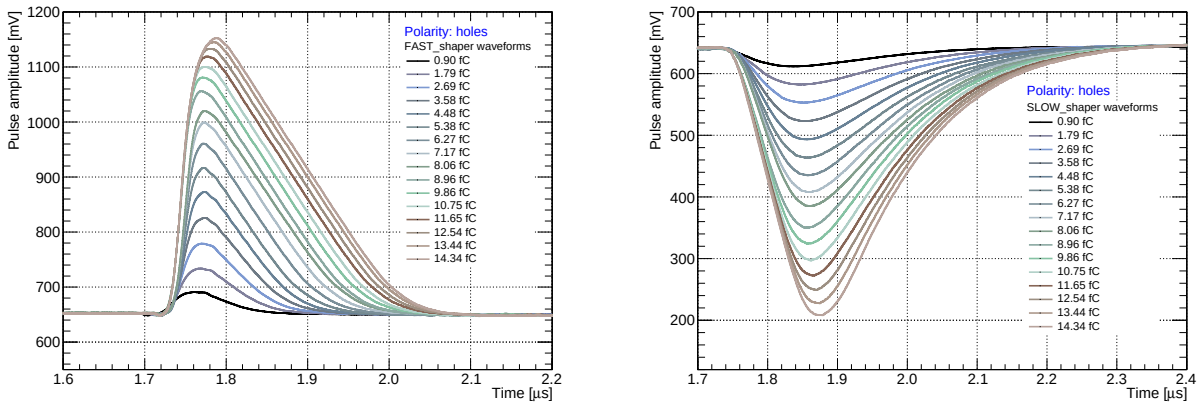
Waveforms from shapers in a test channel are shown in Fig. 3.11 for holes polarity, see Appendix B for electrons polarity. They represent the response to externally injected pulses of different amplitudes. By measuring the output signal amplitude, the shapers gain characteristics can be evaluated for the STS mode. The resulting gain curves for electron and hole polarities are shown in Fig. 3.12. A first order polynomial is used to fit the data and extract the gain parameters. The measured values result in approximately 50 mV/fC and 30 mV/fC for the FAST and SLOW shaper, respectively. The linearity of the fast path is kept up to approximately 5 fC, which can be considered good enough for adjustable threshold settings for time-stamping purposes. As the slow path is optimized for charge measurement, linearity is kept up to 13 fC. This range can be considered sufficient if we consider that for most of the particles created in the experiment, the passage through the active volume of non-irradiated silicon sensors of 320 μm creates charge pulses of approximately 4 fC.

3.6.2 Linearity check for the internal pulse generator

A very useful tool implemented in the STS-XYTERv2 ASIC is the internal calibration circuit that allows the injection of charge pulses into the front-end channels. The built-in circuit enables the automated calibration of all channels and hence to check the pulse processing chain in the chip. To reduce saturation effects, only 25% of the channels (subdivided in four groups) can be excited simultaneously by selecting the desired group. On chip, a bi-stable generator can inject charge pulses into the front-end channels via a set of capacitors (nominal value 100 fF), in a range up to 140 mV, translating to approximately 14 fC. The injected charge can be controlled with an 8-bit register and externally monitored via a dedicated pad on the board (*amp_cal*). Alternatively, an external generator can be sourced into the same pad to generate different pulse patterns (input impedance is 10 kΩ) [90, 96].

A first step to characterize the internal generator is to monitor the linearity of the 8-bit DAC[5] [90]. The generator performance is evaluated by connecting the signal from the *amp_cal* pad to a Tektronik 4054 oscilloscope. The pulses amplitudes are measured for different values

[5]Digital-to-analog converter



(a) *Fast shaper waveforms.*

(b) *Slow shaper waveforms.*

Figure 3.11: *Signal waveforms measured at the shapers output in test channel for injected charges in the range 0.9 fC – 14.4 fC.*

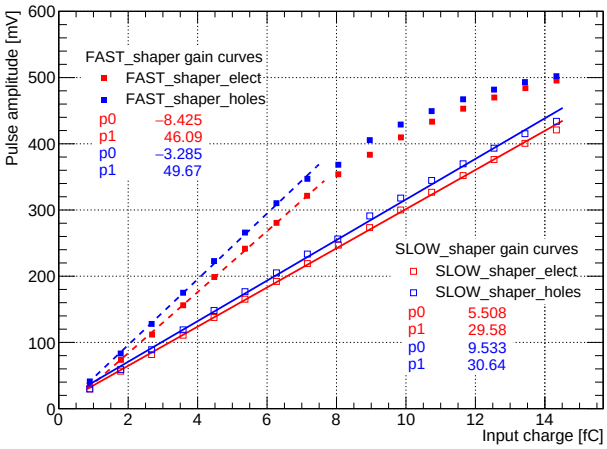
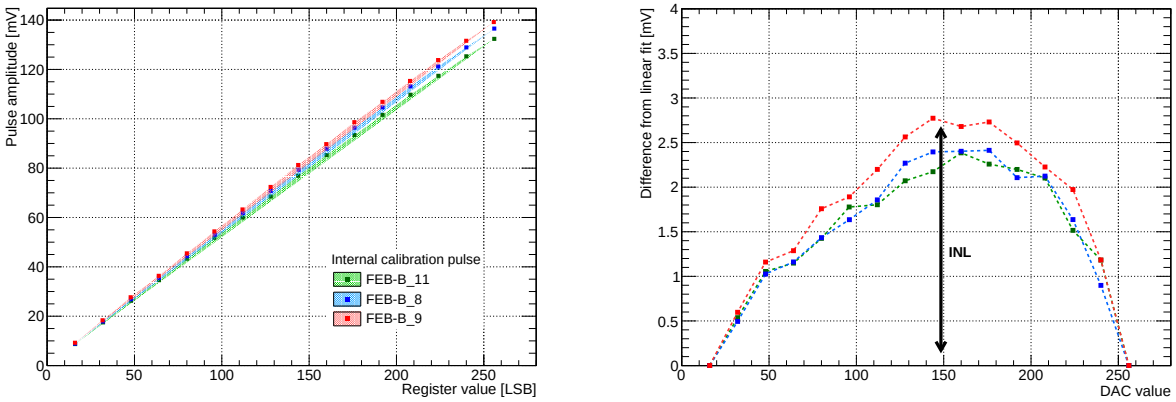


Figure 3.12: *Gain characteristics of the fast and slow shapers for a nominal STS gain.*

of the register in steps of 16 LSB[6]. The same procedure was carried out in two other prototype FEBs-B to cross-check the obtained values. Figure 3.13a shows the measured linear dependences, resulting in an average *amp_cal* unit equivalent to 0.53 mV/LSB. Small discrepancies among the three ASICs (below 5%) can be observed for larger values of the register. These are associated with variations in the baseline measurements. Each data set is fitted with a first order polynomial using the end-point method, in which a line is established using the coordinates of the first and last data point. The difference with respect to the fitting line is shown in Fig. 3.13b. The integral non linearities (INL), defined as the maximum deviation, were found to be below 3.0 mV. This result can be considered acceptable for using the internal pulser in the calibration process and other further analysis of the chip. In average, the full dynamic range of the internal pulse was determined to be 136.2 ± 1.4 mV [98].

[6]Least Significant Bit



(a) *Response function of the internal pulse generator.* (b) *INL of the internal pulse generator.*

Figure 3.13: *Internal pulse generator linearity checked in 3 prototype FEBs-B.*

3.7 Development of a procedure for amplitude and time calibration

The calibration of the STS-XYTERv2 ASIC is a complex process in which multiple registers and diverse ASIC functionalities take part. The process aims to determine the individual correction settings for the ADC and the FAST discriminator in every channel. Since the chip uses different paths for energy and time measurements, the calibration should consider not only the ADC linearity aspects but also a homogeneous time response among all channels. This is an important task to accomplish before using the ASIC in the readout of the silicon sensors.

This section intends to explain the development and test of the calibration procedure for the ADC and fast discriminator in the STS-XYTERv2 ASIC. It shows a detailed description of the process and its main points:

- the operation principle of the flash ADC and FAST discriminator in the chip;
- the development and optimization of the calibration process;
- results of calibrating multiple FEBs using the developed method;
- the verification of the calibration process using an external pulse and a gamma source;
- the stability of the calibration parameters tested in a long run.

3.7.1 The flash ADC and FAST discriminator in the STS-XYTERv2 ASIC

The STS-XYTERv2 implements in each channel a 5-bit continuous type, flash ADC with digital peak detector, see Fig. 3.2 [90]. Other ASICs addressing similar requirements (ultra-high sample speed, small size, low noise and relatively low power consumption) use either a SAR[7] ADC with peak detection based on several samples or a pipeline ADC. In these cases a significant amount of digital, clocked circuits are required, which are active while the signals are processed. For a self triggered ASIC, this can compromise the noise performance since the generated switching noise can easily be transferred into the AFE [85].

[7]SAR: Succesive Approximation Register

The channel-ADCs in STS-XYTERv2 can digitize signals in a dynamic range of approximately 14 fC. This is determined by two reference potentials *VRef_P* and *VRef_N*, controlled by 6-bit resolution registers. The common global threshold of the comparators, also called discriminators, are generated by a resistor ladder stretched between these potentials as shown in Fig. 3.14 [96]. The minimized area of every ADC results in a significant offset mismatch. As a consequence, trimming corrections are used to equalize the ADC transfer characteristics from comparator to comparator and within all channels. The converter uses $2^n - 1$ comparators, one per non-zero ADC value. Each of them has 8-bit trimming threshold voltages that can cover a correction range of ±150 mV. They can additionally be employed to compensate for a potential non-linearity in the amplitude measurement as well as to change the conversion characteristics of the ADC, i.e. to emphasize the amplitude range of interest for a particular experiment. The effective threshold of every discriminator can be mathematically represented as:

$$V_i(mV) = \underbrace{\left(\frac{VRef\_P - VRef\_N}{31}\right)}_{\text{resolution}} \cdot d_i \; + \; \underbrace{\Delta v_i}_{\text{trim correction}} \tag{3.1}$$

where V_i, expressed in mV or units of charge, corresponds to the $d_i th$ comparator, and Δv_i is the trim correction applied to the comparator voltage. The output of the comparators are connected to the peak detector logic, which provides thermometric encoding for all the 31 cells. To prevent ambiguity in conversion to the binary, the code is converted with priority to the first "1" starting from the MSB[8].

An additional reference potential *VRef_T* controls the position of the signal baseline relative to the ADC, thereby, it functions as the effective system threshold. This simplifies the ADC calibration and operation of the system [85, 90]. The calibration values are independent of the position of the baseline, i.e. in case of large amplitude noise, only this potential requires adjustment.

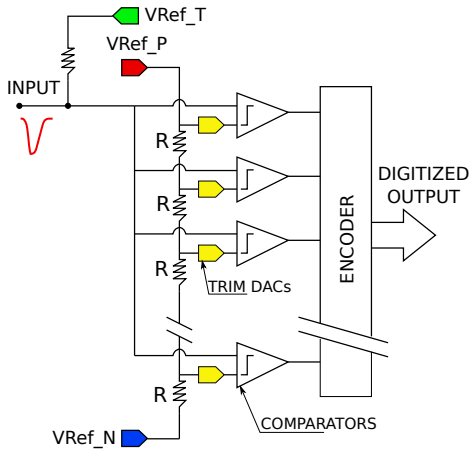


Figure 3.14: *Block diagram of the STS-XYTERv2 flash ADC.*

The fast shaper drives the leading edge discriminator of each channel, used for time-stamping the data. The discriminator uses a global adjustable level *Thr2_glb* and a 6-bit in channel offset trimming DAC.

In the ASIC, every discriminator is equipped with a diagnostic counter. This feature consists of 12-bit registers connected at the output of every comparator and readable via the control path. They are designed to facilitate the tests of the AFE and the chip calibration.

[8]MSB: Most Significant Bit

3.7.2 Description of the calibration procedure

The main steps of the calibration procedure are presented in the block diagram shown in Fig. 3.15); they can be described as follow: In an initial stage, the user must define the signal polarity, the reference potentials (*VRef_P* and *VRef_N*) and the calibration range of the ADC, i.e., the threshold of the first and last discriminator. Since the procedure uses the ASIC internal pulse generator, the calibration range is expressed in units of the internal pulse (see Section 3.6.2). This range is equally distributed in 31 steps, resulting in the corresponding threshold for each comparator. The threshold of the timing discriminator is adjusted to be the same as in the first ADC level.

The effective threshold is adjusted by scanning the trim DAC of every discriminator. The response function is read out using the diagnostic counters. The trim scan is done in two steps. The first one is referred to a coarse scan, in which the discriminator response (*s-curve*) is evaluated in a wide range of trim values with step of 5 LSB. A fast checking algorithm finds the value of the trim at which the hit occupancy represents 50% of the number of injected pulses. This value, called $primer\_v_{50}$, is used as an input for the second step of the procedure. The fine scan is performed in a range of ± 20 LSB values around the $primer\_v_{50}$ with a step of 1 LSB. The fine step allows to reduce the uncertainties in the procedure due to the local non-monotonic behavior of the trim DACs. Subsequently, a more elaborated algorithm analyzes the data to find again the 50% (vt_{50}) or switching point of the *s-curve*. The outcome is a 128 × 32 elements matrix that contains the trim values for every channel. The trimming procedure yields unique results for each channel and chip. The calibration matrix can not be parametrized and is not applicable to other ASICs.

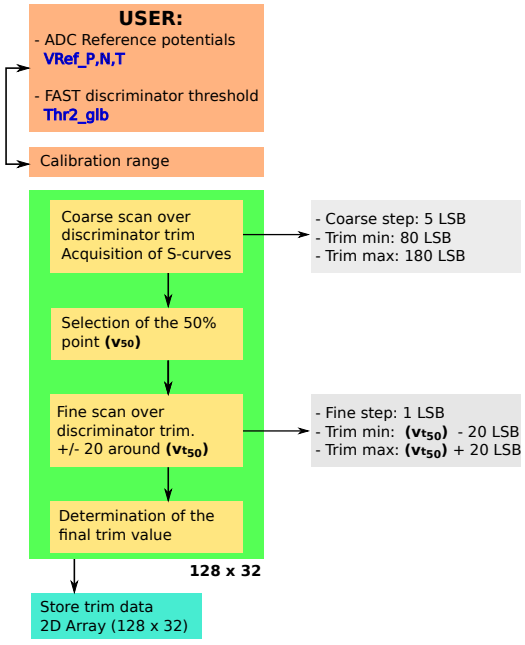


Figure 3.15: *Flow diagram of the calibration procedure.*

3.7.3 Optimization of the calibration procedure

For simplicity, the calibration process uses the internal generator, however, it can alternatively use an external pulse generator connected via the *amp_cal* pad. These two different ways has implications in the running time, since the number of pulses are injected four times in order to

excite all the channels of the chip (see subsection 3.6.2). The chip also implements a calibration pad, which accesses directly the ADC and grants to inject pulses in all channels simultaneously. However, this does not allow to test the AFE path. Therefore, the procedures described here are limited to the internal pulse generator. To optimize the performance of the calibration procedure in terms of time consumption while keeping the accuracy, it is mandatory to evaluate the contribution of the main parameters:

- the discriminator trimming range;
- the speed of the data transmission over the data control path;
- the number of injected pulses.

Every discriminator trimming DAC has 8-bit resolution, which represent 256 possible values that follow a non-monotonic behaviour. As a consequence, the procedure should scan every trim value to find the best set. A fitting algorithm, although accurate, may not result in the optimal value due to the local non-monotonic behavior of the trim. By knowing the calibration range and establishing the proper reference potentials ($VRef\_P$ and $VRef\_N$) for the desired range, it is possible to reduce the trimming range to approximately 50 values around the typical point (DAC configuration value = 128 LSB).

The control path in the readout chain relies on the IPBus protocol using a 1 Gbps Ethernet link. The effective data transmission speed is slower and is affected by the configuration of the computer local network. The number of write/read operations during the full procedure determines more than 98% of the performing time. This contribution is represented in Fig. 3.16a with dotted lines.

The reliability of the calibration values depends on the statistical errors in the acquisition of the *s-curves*. This has implications in the number of pulses that are injected in each channel and hence, the number of write/read actions. To estimate the accuracy of the calibration, we measure the difference between the effective discriminator threshold and the value set on the calibration. The width of the residual distribution for all channels represents a measure of the accuracy of the algorithm. In the case of the ADC, another reference measurement is to consider the linearity parameters. These estimators allow to establish a decision criteria for the number of required pulses and the running time.

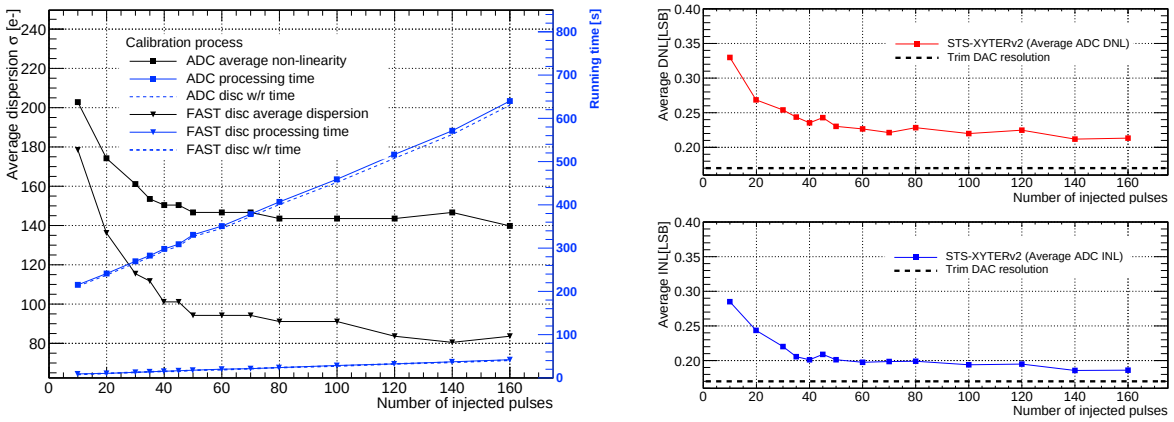
Figure 3.16a shows the performance of the algorithm and the running time as a function of the number of pulses. Every data point represents the spread of all discriminators threshold relative to their ideal calibration value. The estimator follows a decreasing trend with the number of injected pulses until it reaches a stable value around 80 and 140 electrons for the FAST discriminator and the ADC, respectively.

The ADC differential non-linearity (DNL) and INL are also considered to evaluate the calibration algorithm. They represent important characteristics of the data converter. Figure 3.16b top illustrates the trend followed by the DNL estimator as a function of the injected pulses. Every value represents the mean value of the channels distribution. In each channel, the DNL is calculated as follow:

$$DNL = max\Big(\frac{V(i+1) - V(i)}{\Delta V_{ideal}} - 1\ LSB\Big) \tag{3.2}$$

where $V(i)$ represents the physical value corresponding to the digital output code i, and ΔV_{ideal} is the ideal spacing for two adjacent digital codes.

The INL error is described as the maximum deviation, in LSB or percent of full-scale range, of an actual ADC transfer function from a straight line. The magnitude strongly depends on the



(a) *ADC and FAST discriminator average dispersion.* (b) *ADC linearity characteristics.*

Figure 3.16: *Performance of the calibration algorithm for the ADC and FAST discriminator as a function of the number of injected pulses in the chip. a) The convergence of the procedure is measured in terms of the dispersion between channels. The algorithm running time is shown in the right axis. b) Linearity characteristics of the channels ADCs (every point represents the average among all channels).*

chosen method to fit the data. This study implemented the end-point method, which fits a straight line between the first and last point of the transfer function. The results were averaged among all channels on the chip and plotted as a function of the number of injected pulses.

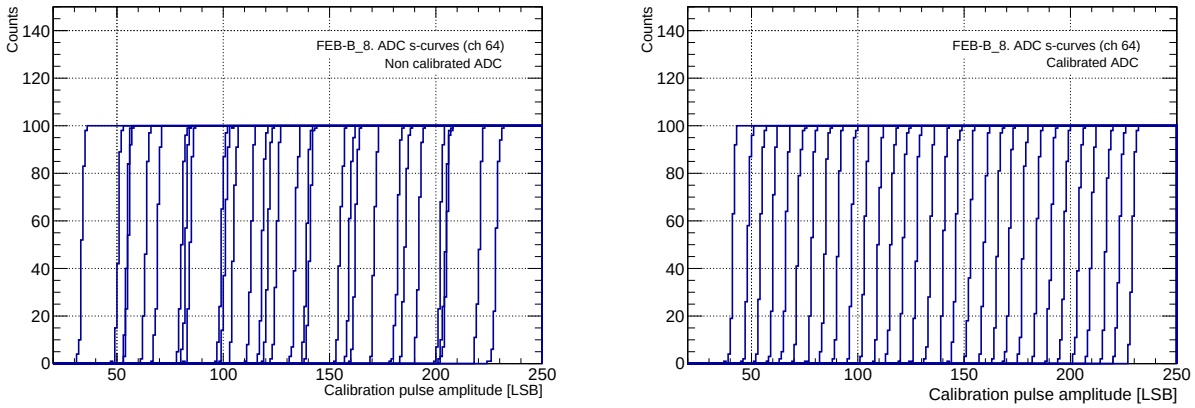
Results indicate that the calibration procedure reaches saturation values in the precision of the threshold when injecting more than 50 pulses in the ADC path and more at least 100 pulses in the FAST discriminator. These values establish the minimum running time per ASIC, approximately 360 s per chip. The ASIC test is one of the shortest procedure in the full module assembly work flow. However, for a big detector system as STS, where more than 14000 chips will be used, this result still requires improvements. In this direction, we think in different alternatives such as:

- reducing the coarse scan window;
- using an external pulse generator to increase the number of injected pulses and therefore, reduce the writing time;
- using the dedicated ADC calibration pad that allows to excite 128 channels simultaneously;
- multiplying the number of testing stations to address the amount of ASICs.

3.7.4 Results of the analog front-end calibration

To qualitatively illustrate outcome of the calibration procedure, Fig. 3.17 displays the ADC discriminator response for a randomly selected channel. The comparison shows the results of a *s-curve* scan before and after calibration. Figure 3.17 allows to visualize how the linearity of the ADC is achieved after applying the algorithm. A system that is configured with default trim values drives a poor performance due to many discriminator can overlap each other. Their effective thresholds might not only substantially differ from the ideal values, but also determine incorrect limits and even cause missing ADC codes. The calibration procedure corrects these effects by finding proper settings for every discriminator and it also reduces channel to channel variations.

From the discriminator's *s-curves* it is also possible to extract information concerning the linearity of the ADC. The effective threshold, in units of the calibration pulse amplitude, is the value

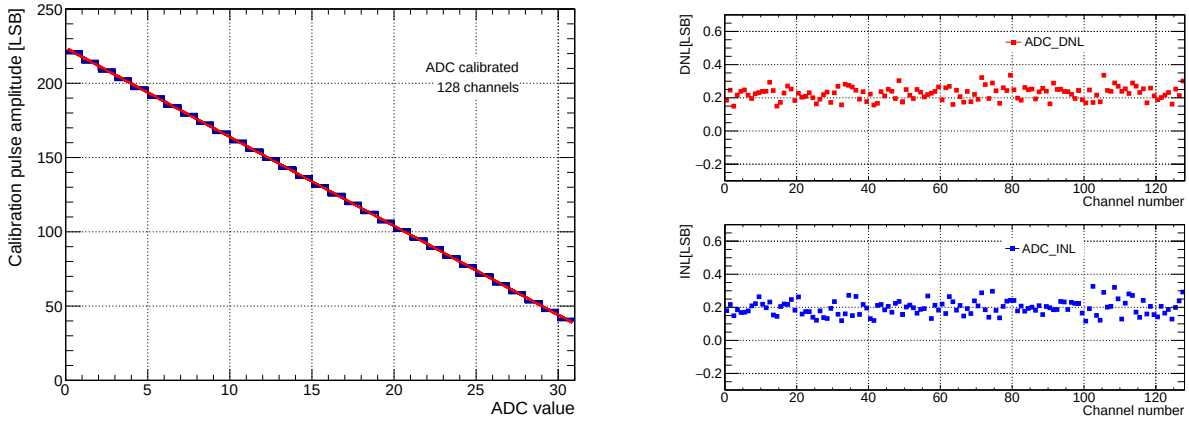


(a) *Before calibration.* (b) *After calibration.*

Figure 3.17: *Typical s-curves for the 31 ADC discriminators before and after applying the calibration procedure. In (a) it can be observed the overlapping of several discriminators, which may cause faulty values in the ADC response. This effect is corrected with the calibration as shown in (b).*

at which the discriminator response is half of the number of injected pulses. This parameter can be extracted by fitting the *s-curve* with an error function ($erfc$).

The transfer functions for 128 channels of a chip are displayed on Fig. 3.18a after calibration. The ADC has a dynamic range of 10.08 fC, with an offset corresponding to 2.24 fC. The linearity characteristics are shown in Fig. 3.18b, where it can be recognized that DNL and INL are below 1 LSB. For an ADC, the DNL error specification of less than or equal to 1 LSB guarantees a monotonic transfer function with no missing codes. The low INL values, below 0.4 LSB, ensures that the linearity of the system is correctly achieved.

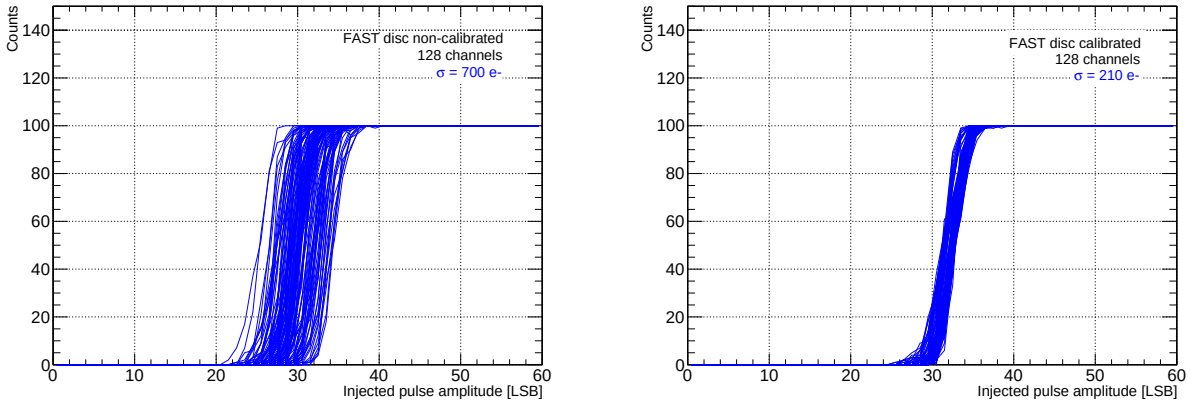


(a) *Calibrated ADCs in 128 channels* (b) *ADC linearity parameters.*

Figure 3.18: *ADC transfer function after calibration and linearity characteristics in 128 channels of a single STS-XYTERv2 ASIC.*

In order to achieve a homogeneous timing response among all channels, every fast discriminator also undergoes a trimming process. In case the fast threshold is not properly set, the hit data will contain a wrong timing information that might correspond to the previous recorded hit, and hence

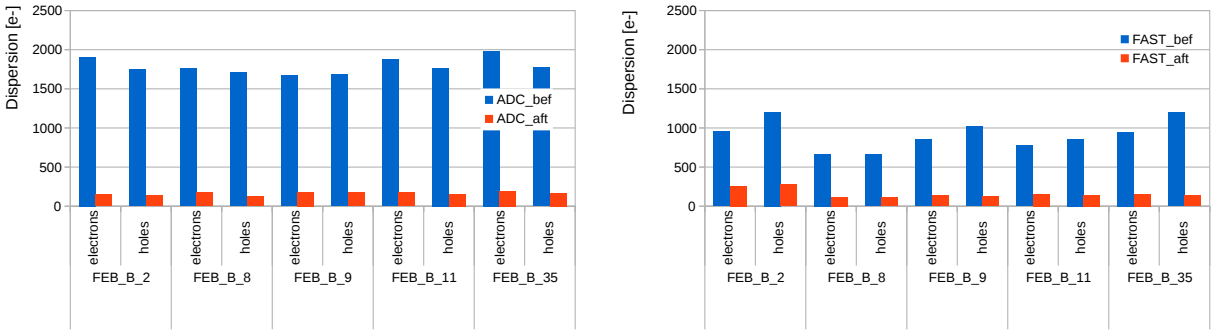
associated to a different physics event. Figure 3.19 shows the *s-curves* in 128 channels before and after calibration for a fixed absolute threshold. Similar values can be obtained independently from the signal polarity. In many cases, the spread can be reduced up to five times, which can result in more than 5 ns difference for smaller signals.



(a) *FAST discriminator before calibration.* (b) *FAST discriminator after calibration.*

Figure 3.19: *Comparison of the threshold spread in the FAST discriminator of all channels before and after calibration.*

During the series production of the prototype FEB-B, five different samples were randomly selected and the calibration procedure was verified. The threshold spread among all channel before and after calibration is shown in Fig. 3.20. The dispersion was found to be as large as 2000 electrons without calibration of the ADC, and significantly improved by a factor 13 after the process. The procedure yields similar results independently of the signal's polarity.



(a) *ADC threshold dispersion.* (b) *FAST discriminator threshold dispersion.*

Figure 3.20: *Uniformity of the channel's threshold measured before and after calibration in five different FEBs.*

3.7.5 Validation of the ADC calibration using an external pulse generator and a gamma source

To cross-check the results of the calibration procedure, the ADC response function to different signal sources is studied using two methods. The first one consists of injecting external charge pulses into the chip through the channels input using an attenuator board, see Fig.3.21. This method differs from using the *amp_cal* pad, since all channels can be accessed simultaneously. Reference voltage pulses are generated using an Agilent 33250A arbitrary waveform generator and injected at 10 kHz in four different channels. The input voltage is attenuated 20 times before passing into a 1 pF capacitor. The signal charge can then be calculated as $Q = C \cdot \Delta V$. To correct for parasitic capacitances and discrepancies in the resistance values, the capacitors, as well as the voltage divider resistors are measured using a Peak Tech 2155 LCR meter.

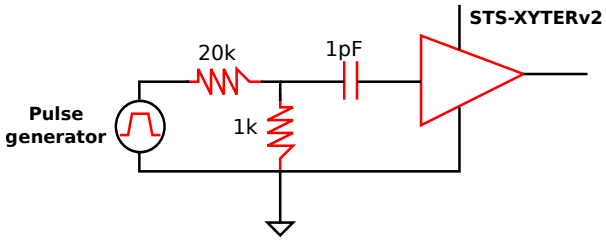


Figure 3.21: *Schematics of the charge pulse injection circuit.*

For such purpose a prototype FEB-B carrying one STS-XYTERv2 was used. Channels' ADCs are calibrated in advance for both polarities using two different ranges:

- **Extended range:** ADC gain of 0.39 fC/ADC LSB in a dynamic range of 12.2 fC (20 - 240 *amp_cal* LSB). The offset was kept at 1.17 fC to reject noise hits [98].
- **High resolution range:** ADC gain of 0.11 fC/ADC LSB, average offset of 1.52 fC and a reduced dynamic range of approximately 3.42 fC.

The ADC response functions for electron polarity are presented in Fig. 3.22. The same study was performed for hole polarity showing a good agreement with the previous results. From the linear regressions, it is also possible to determine that 1 *amp_cal* LSB, from the internal pulse generator, is equivalent to 0.056 fC or approximately 350 electrons. This result is consistent for both polarities and independent of the ADC range. The range of the internal calibration pulse can also be confirmed as approximately 14.16 ± 0.16 fC [98].

The second method to evaluate the ADC performance is reading out the signal of a gamma source emitter using a silicon microstrip detector. A sensor with a size of 4.2 × 6.2 cm^2 and a thickness of 285 μm is glued onto a testing board and 128 channels interfaced by means of two ERNI connectors. The sensor is operated at 150 V while full depletion is expected to be above 80 V. The signal is read out from 128 channels on the *n-side*, resulting in an active area of approximately 0.78 × 6.2 cm^2. A non-collimated ^{241}Am gamma source, with an activity of 37 MBq is used.

In order to have a better energy resolution, the measurements are performed using the ADC high resolution range described above. The resulting spectrum is shown in Fig. 3.23, where only 1 strip-cluster signals are considered. The low energy peaks in the gamma spectrum such as 13.6 keV and 26.3 keV are not observed due to the threshold level of 1.52 fC. The peak position of the 59.5 keV line from the ^{241}Am was determined by a Gaussian fit, yielding an ADC value of 10.27 LSB. According to the ADC transfer function for the high resolution calibration, see Fig. 3.22, the deposited energy can be calculated as 2.65 ± 0.22 fC, which is in agreement with the expected value of 2.64 fC.

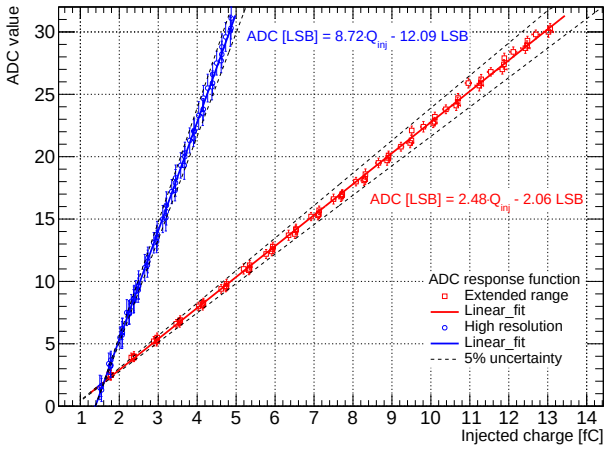


Figure 3.22: *ADC transfer function for two different ranges using external pulses injected via an attenuator board.*

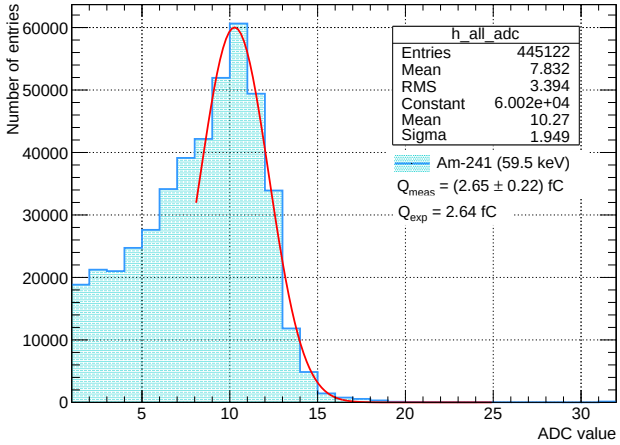


Figure 3.23: *Gamma spectrum of an ^{241}Am source measured with a silicon sensor read out with the STS-XYTERv2.*

3.7.6 ADC and FAST discriminator threshold linearity

The *VRef_T* and *Thr2_glb* are two important DACs that allow to control the absolute threshold of the ADC and the FAST discriminator, respectively. They do not modify the transfer characteristics of the system or affect the trim values, however, a proper understanding of the registers value is mandatory for a correct operation of the ASIC in the detector readout. With such purpose, the registers response was measured and their linearity evaluated.

The ***VRef_T*** is a global DAC, that allow to adjust the position of the signal baseline relative to the ADC, i.e. setting the effective threshold of the chip without the need to modify the ADC transfer function. This represents a comfortable degree of freedom that can be exploited during calibration or in case of noise saturation. To carry out this study, the signal threshold is scanned in a small domain of the *VRef_T* register. This range (∼3.2 fC) is sufficiently large for the STS mode, since the current design of the threshold is built to cover a large signal range, with a coarse

resolution of approximately 2000 electrons/LSB [90, 96]. Two methods are used to check the linearity of the register. The first one is based on *s-curve* scan for the ADC discriminators at different values of the *VRef_T* register. Results are shown in Fig. 3.24 for three discriminators of the ADC. Each data point represents the average response among all channels of the ASIC. To estimate the gain, the data are fitted in every discriminator, with a first degree polynomial in the selected range. To reject noise hits, the data in the lowest discriminator is taken from register values larger than 180. The accuracy of the method depends on the precise calibration of the ADC. No significant discrepancies (below 1%) between hole and electron polarities were observed. The *VRef_T* resolution can be established as 0.37 ± 0.02 fC/LSB in a large register's range.

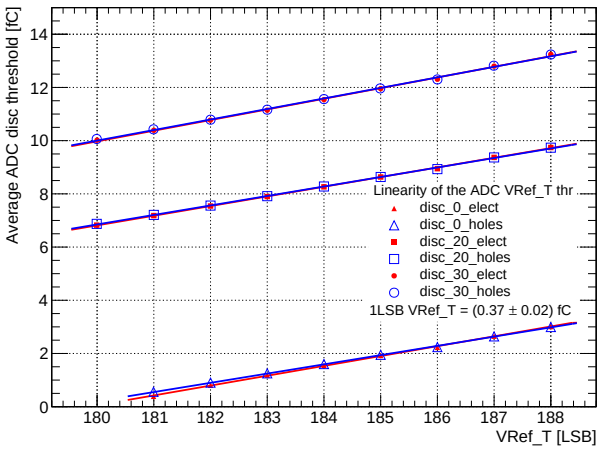
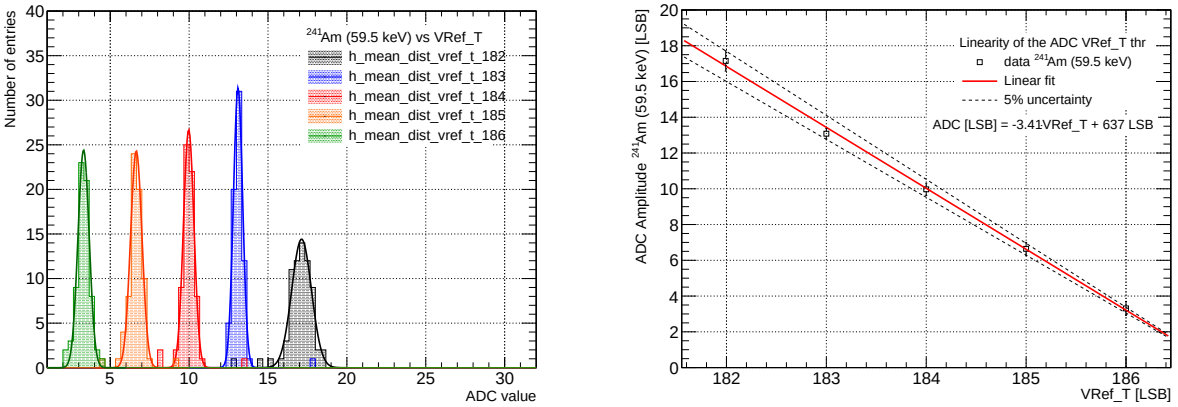


Figure 3.24: *VRef_T linearity check in three ADC discriminators.*

In the second method, the photopeak of an ^{241}Am 59.5 keV gamma source is measured at different *VRef_T* values. The ADC is calibrated as described in subsection 3.7.5, and signals are read out from 64 channels of a 4.2 × 6.2 cm^2 silicon sensor. The distributions of the peak position are shown in Fig. 3.25a. For a lower threshold (*VRef_T* = 182), the spread of the measured values is larger among the channels due to the noise contribution. The linearity of the *VRef_T* DAC is shown in Fig. 3.25b. The error bars describe the spread of the distributions represented in Fig. 3.25a. The transfer characteristics can be estimated from the results of the linear regression and the ADC gain, resulting in 1 *VRef_T* = 0.37 fC/LSB [98]. This result is in agreement with the one estimated above and shows a discrepancy of 15% with the designed value [85]. Precision of the method depends on the accuracy of the ADC calibration.



(a) ^{241}Am *(59.5 keV) peak position measured in 64 channels.*

(b) *Linearity check of VRef_T threshold using the 59.5 keV gamma line of an* ^{241}Am *source.*

Figure 3.25: *Cross-check of the VRef_T linearity using an* ^{241}Am *gamma source.*

The ***Thr2_glb*** is also an 8-bit global DAC, which determines the absolute threshold of the FAST discriminator and hence the latch of the hit timestamp [90, 96]. The transfer characteristics of the register are checked in a threshold scan. In every channel, a fixed charge is injected and the discriminator response is evaluated as a function of the register threshold. The procedure is repeated for different injected charges and both signal's polarities.

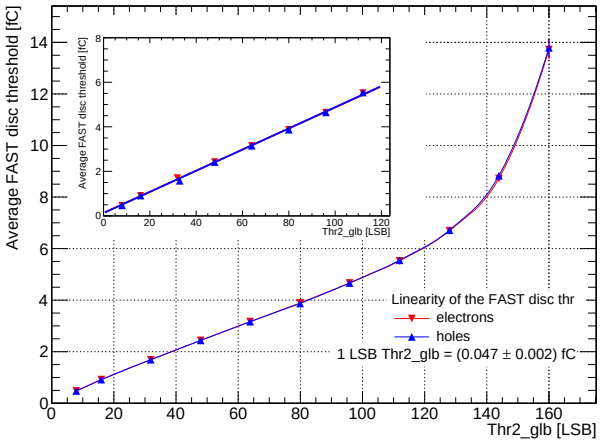


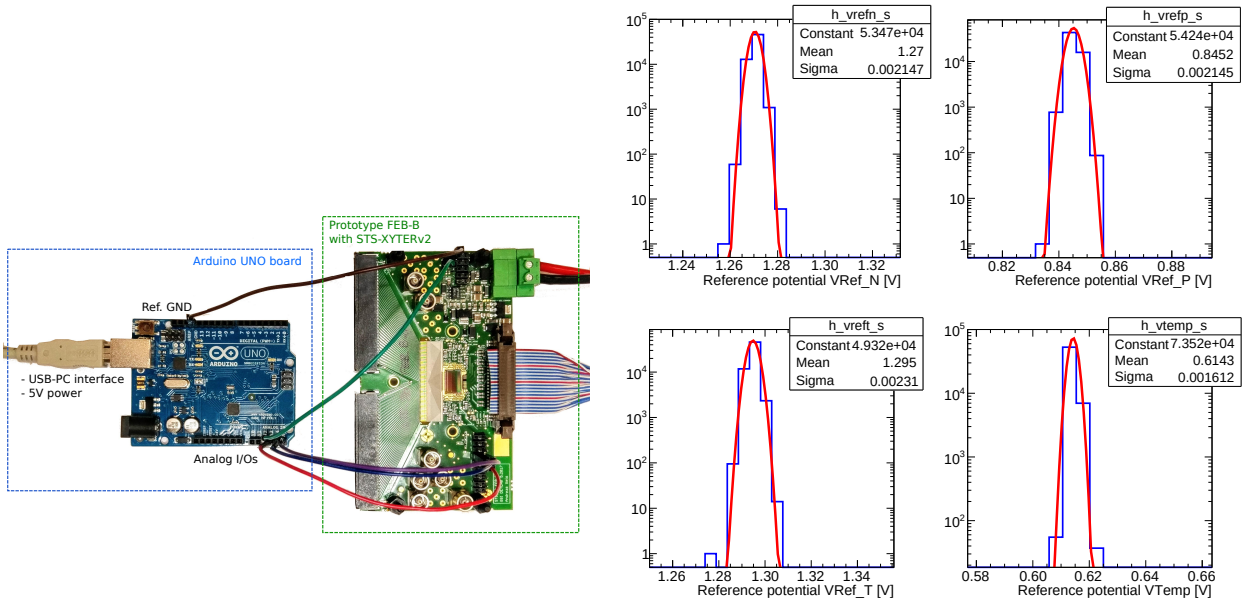
Figure 3.26: *Linearity is kept up to 6 fC for the Thr2_glb register.*

The linearity of the *Thr2_glb* is well maintained in a range larger than 5 fC (up to 120 LSB) as shown in Fig. 3.26. In these limits, a first order polynomial fit is used to estimate the charge equivalence of one register unit, resulting in 0.047 ± 0.002 fC/LSB, see zoomed range in Fig. 3.26. A clear overlap in the data is observed for electron and hole polarities, with discrepancies that increase towards larger register values but remain smaller than 1% in the whole range.

3.7.7 Stability of the calibration parameters

Stability of the operation parameters in time is an important performance metric of the system. We carried out a long run monitoring of the reference potentials of the ADC: *VRef_P*, *VRef_N* and the slow path baseline *VRef_T*. During the run, the chip temperature was also controlled via the built-in thermal probe. In the prototype FEB-B, these potentials are externally routed into output pins for easy access. For these tests we use the commercially available Arduino UNO microcontroller board [99]. This board is equipped with sets of digital and analog input/output pins that may be easily interfaced with the FEB-B. The extensive online support and flexibility of the programming platform allows to build up a simple design for the tests. The built-in 10-bit ADC, implemented on the board, enables the monitoring of analog voltages with a resolution of 4.88 mV/LSB in a range up to 5 V.

Figure 3.27a shows the simple test setup consisting of an Arduino UNO board and the prototype FEB-B connected via multiple wires. A common ground was shared among the boards providing a reference for the measurement. The acquisition software was built in the Arduino Iddle and ported to the board via the USB interface. The necessary power for biasing the board was provided via this interface. Potentials were monitored every second during more than 16 hours. Similar tests were carried out for multiple ASICs but no significant discrepancies were found among them.



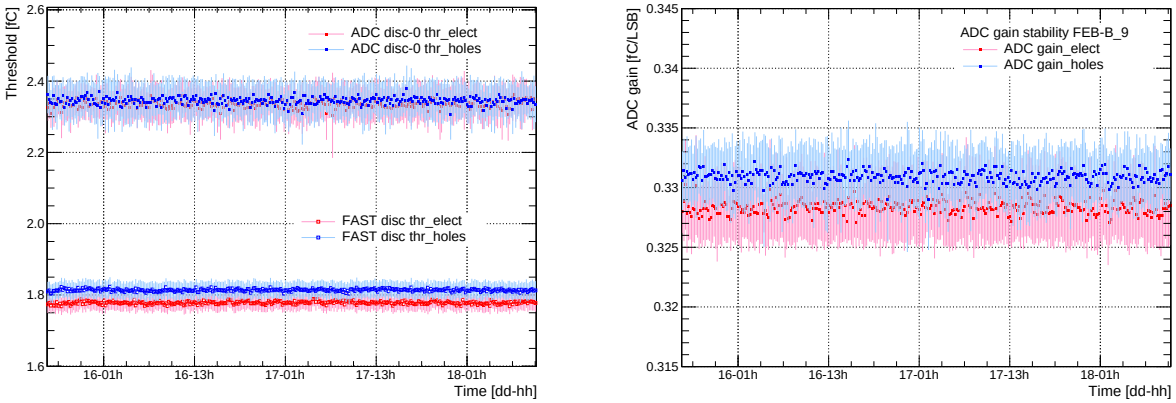
(a) *Test setup based on Arduino UNO board for monitoring ASIC potentials.*

(b) *ADC reference potential stability as a function of time.*

Figure 3.27: *Long-term stability test of the ADC reference potentials using an Arduino UNO board.*

The results of the long monitoring run are shown in Fig. 3.27b. Along the full test there is no observation of a significant change in the reference potentials; fluctuations around the typical values are no larger than 1%. Even if the resolution of the Arduino board is larger than the thermal probe, we can not observe a significant change of the temperature during the tests. Peak-to-peak variations in the chip temperature could be estimated up to 6°C.

The stability of operational parameters such as the effective discriminator thresholds and the ADC gain can be affected by fluctuations on the biasing potentials of the ASIC and in a smaller scale, by temperature changes. A stability test can shed light on the ASIC performance during and



(a) *ADC and FAST discriminator threshold.* (b) *ADC gain.*

Figure 3.28: *Long-term stability test of the calibration parameters. The chip response is measured every 12 min during more than 48 hours.*

after long operational periods. With this goal, a typical *s-curve* scan is performed every 12 min for more than 48 hours. The survey checks the chip operational parameters for both polarities. Figure 3.28a displays the results for the timing discriminator and the lowest threshold in the ADC. The latter is a sensitive value since it initiates the generation of the data or noise hit. A corrupted value during operation can result in a large noise occupancy of the chip. Every measured point corresponds to the average among all channels in the ASIC, while the error bars represent the dispersion.

The ADC gain, see Fig. 3.28b, was estimated as the slope of the transfer function in every channel and averaged among them. No significant change is observed for any of the monitored parameters. All fluctuations are contained within the error bars and the observed discrepancy in the average gain for holes and electrons is smaller than 1%.

3.8 Timing measurements. Evaluation of the jitter and time-walk

Timing measurements seek to optimize the determination of time of occurrence of a signal in the detector. In the STS-XYTER ASIC the fast discriminator is used to generate an accurately timed logic-level from an analog input pulse that triggers the latching of the timestamp value. In spite of the fact that the discriminator is optimized for time measurements, there are major contributors to the overall accuracy of time information [59, 85]. Those can be related as the following:

- clock frequency: LSB of the timestamp counter is $\mathrm{TS}_{bin} = 3.125$ ns;
- jitter: dependent on the voltage noise level at the fast shaper and slope around the threshold;
- time-walk: dependent on the input pulse amplitude.

The overall time resolution (σ_T) can be mathematically expressed as the sum of uncorrelated sources and hence added quadratically:

$$\sigma_T^2 = \underbrace{\left(\frac{TS_{bin}}{\sqrt{12}}\right)^2}_{\text{timestamp}} + \underbrace{\left(\frac{\sigma_n}{\frac{dV}{dt}\,|_{V_{thr}}}\right)^2}_{\text{jitter}} + \underbrace{\left(\frac{V_{thr}}{\frac{dV}{dt}}\right)^2}_{\text{time walk}} \tag{3.3}$$

where σ_n is the noise level, V_{thr} the threshold level of the discriminator and dV/dt the slope of the leading edge.

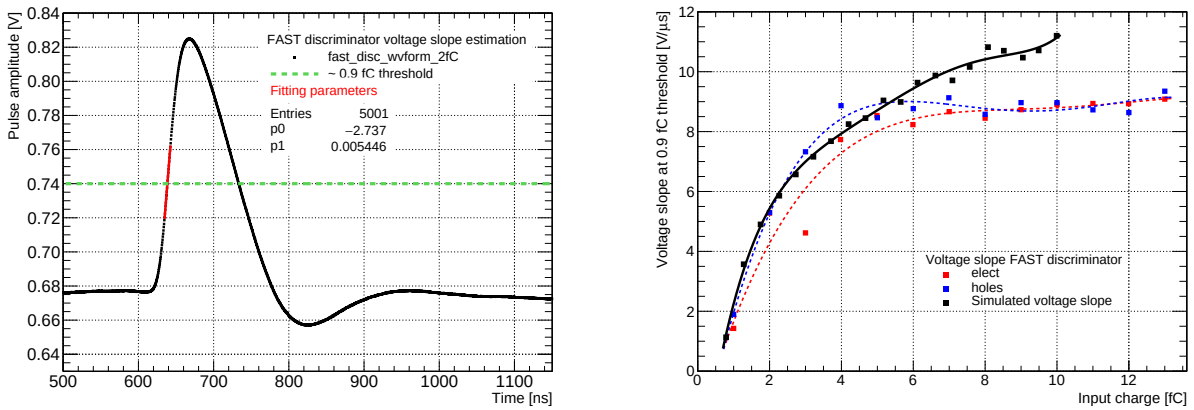
The clock frequency can be considered as an intrinsic property of the system and its contribution as a constant value. A reduction of the bin size, i.e. faster clock, has many implications in the design of the readout chain. In addition, faster, low jitter and stable clock are difficult and expensive requirements to implement.

The instantaneous signal level is modulated by noise. Because of these fluctuations, the time of threshold crossing changes. This is commonly known as jitter, and it can be expressed as:

$$\sigma_t = \frac{\sigma_n}{\frac{dV}{dt}\,|_{V_T}} \approx \frac{t_r}{S/N};\ t_r \textit{ discriminator peaking time.} \tag{3.4}$$

Since the leading edge is not linear, the optimum trigger level is the point of maximum slope dV/dt. A steep slope around the exemplary threshold level (e.g. at 0.9 fC) is required to minimize the jitter of the rising edge.

Figure 3.29a shows a waveform recorded in the fast shaper of a test channel. The leading edge has been fitted around the typical threshold ($\sim$ 0.9 fC) with a first order polynomial. A similar procedure is carried out for different amplitudes and polarities. The values of the voltage slope as a function of the input charge are depicted in Fig. 3.29b. The values obtained from a post-layout simulation are shown in black [85]. They show a good agreement with the measured values up to 6 fC. For the considered range, the transition rate changes from 2 V/μs up to 9 V/μs, where it remains constant. These properties together with the estimated average noise level of 1500 ENC(e^-) correspond to jitter values between 3.2 and 1.5 ns rms for the corner cases and 1.6 ns rms for a typical 4 fC charge [85].



(a) *FAST shaper waveform fitted around 0.9 fC threshold.*

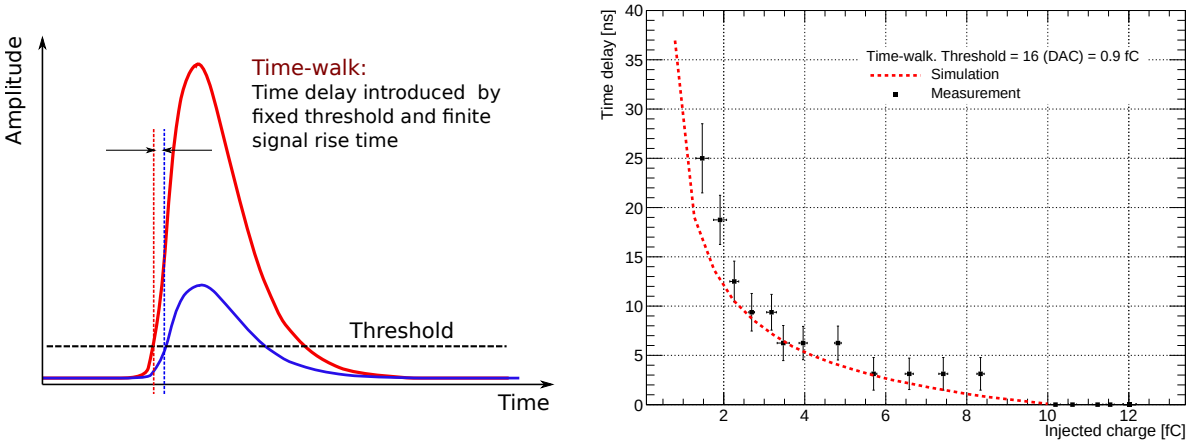
(b) *Voltage slope at approximately 0.9 fC threshold. Lines are just to guide the eye.*

Figure 3.29: *Estimation of the FAST discriminator voltage slope for different charge pulse amplitudes.*

The time at which a signal crosses a discriminating threshold depends on the rise-time and the amplitude of the signal. The variation on the pulse amplitude will inevitably create a time-walk effect in the measurements. This time-shift is known and illustrated in Fig. 3.30a.

There are two possible solutions to deal with this effect: the first one is to measure the amplitude and apply an offline correction; the second one to reduce the walk is by setting the threshold to the lowest practical level or by using amplitude compensation circuitry, e.g. constant fraction discriminator (CFD). In a CFD the time correction is made instantly by hardware. This solution

will require larger area and power resources. The STS-XYTERv2 implements a simple leading edge threshold discriminator and hence correction for optimal time resolution must be done offline.



(a) *Time shift present in pulses with different amplitudes.*

(b) *Comparison between time-walk measurements and simulated values.*

Figure 3.30: *Time-walk correction in the STS-XYTERv2.*

To estimate the time-walk in the STS-XYTERv2 ASIC, a simple setup using an AGILENT 33250A arbitrary waveform generator with $\tau_R = 1$ ns is used. Two consecutive pulses, separated by 12 μs, are injected into a channel of the chip. The first pulse is taken as time reference; it has a high amplitude (10.5 fC) to ensure the fast rising edge. The amplitude of the second pulse is modified between 1.2 and 12 fC. For every measured point a total of 20000 pulses are generated. Data are processed using the energy information collected in the ADC with a resolution of 0.34 fC/LSB. The corresponding time-walk response is shown in Fig. 3.30b. Simulation results, obtained during the designed phase, are also included. A good agreement is observed with the simulated data for signal amplitudes larger than 2 fC. The measured time-walk reaches up to 25 ns for pulses with small amplitudes after subtracting the propagation time. The horizontal error bars represent the width of the energy distribution measured in the channel's ADC. Vertical error bars are determined by the jitter of the system; their magnitude also decrease with larger signal amplitude. According to Eq. 3.3, the expected intrinsic resolution of the STS-XYTERv2 ASIC, is approximately 5.3 ns before correction. This estimation is based on signals from minimum ionizing particles (MIP), which generates approximately 4 fC charge when traversing 320 μm thickness of silicon. The largest contribution is precisely the time-walk, however, if this offset can be adjusted, the resolution can be improved to values below 2 ns.

3.9 Systematic study of the STS-XYTERv2 noise

The noise performance of the silicon detector modules is one of the most important design parameters for the STS [56, 100]. Excessive noise can not only worsen the quality of the data by introducing a large background, but also completely obstruct the data-taking by overwhelming the data acquisition system. This is especially threatening to self-triggering systems, which are intrinsically more vulnerable to the noise, compared to conventionally triggered systems. In the latter, a noise hit is produced whenever the hit amplitude is larger than the threshold and is timely located in the trigger window; whereas in a self-triggered system, noise hits are instantaneously

digitized as soon as their amplitude exceeds the threshold.

The signal in the STS-XYTERv2 is processed independently for time and energy measurements. This architecture enables a more elaborated scheme for the hit generation. Due to the higher bandwidth of the fast path, the noise level is comparatively high. On the contrary, the slow path has been optimized for lower noise, enabling to trigger the hit once a slow shaper signal crosses the ADC first comparator threshold. This mechanism prevents hit generation in case that only the FAST discriminator is triggered, i.e. the ADC imposes a veto to the data transmission in case it has generated a zero [85].

This section presents an extensive and systematic characterization of the noise in the STS-XYTERv2 ASIC. In a first part an analytical study of the noise sources in the STS is discussed. The second part is dedicated to the measurement of the overall noise levels in the chip as a function of multiple factors, as described in Figure 3.31. The influence of factors such as temperature or voltage regulators used in the powering scheme, can deteriorate or improve the performance of the chip. A more detailed study of them will allow a better understanding of the noise in the ASIC and can assist in the decisions of future materials and components to be used for the final STS system.

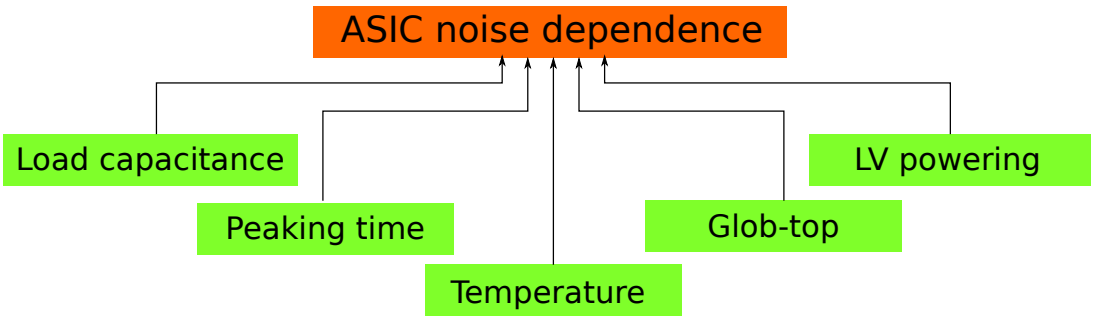


Figure 3.31: *Overall noise levels in the STS-XYTERv2 can be studied as a function of different factors.*

3.9.1 Analytical study of the noise in the STS-XYTERv2

Three are the major contributions to the noise in the STS detector module: the thermal noise of the resistive structures (biasing resistors, aluminium strips, cable traces), the shot noise due to the detector leakage current and the intrinsic noise of the charge sensitive amplifier. An external component to the shot noise is the current flowing through the transistors of the electrostatic discharge (ESD) protection circuit. This contribution has been analyzed in detail for the STS-XTERv2 [101].

Amplifiers tend to exhibit a "white" noise spectrum at high frequencies, which can be estimated as $e_{na}^2 \approx 4k_BT\alpha\gamma/g_m$, where α and γ are parameters of the CSA and g_m is its transconductance [100]. However, at low frequencies, the excess noise component has a spectral density proportional to K_f/f, also called flicker noise. The coefficient K_f is characteristic of the CSA. In field effect transistors based amplifiers, the current noise (i_{na}^2) contribution can be considered very small [59].

An equivalent circuit of the STS detector module showing the main elements contributing to the system noise is shown in Fig. 3.32 [100]. To analytically estimate the noise performance, the system can be described in terms of three equivalent noise sources:

- parallel current noise (i_n^2)

$$i_n^2 = \frac{4k_BT}{R_{bias}} + \frac{4k_BT}{R_{fb}} + 2eI_{det} + 2eI_{ESD_n} + 2eI_{ESD_p} \tag{3.5}$$

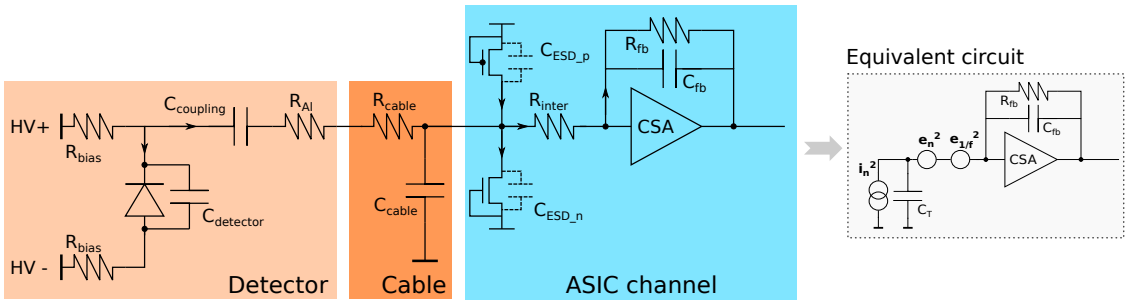


Figure 3.32: *Noise sources in the detector readout system. Simplified model.*

- series voltage noise (e_n^2)

$$e_n^2 = 4k_BTR_{Al} + 4k_BTR_{cable} + 4k_BTR_{inter} + e_{na}^2 \tag{3.6}$$

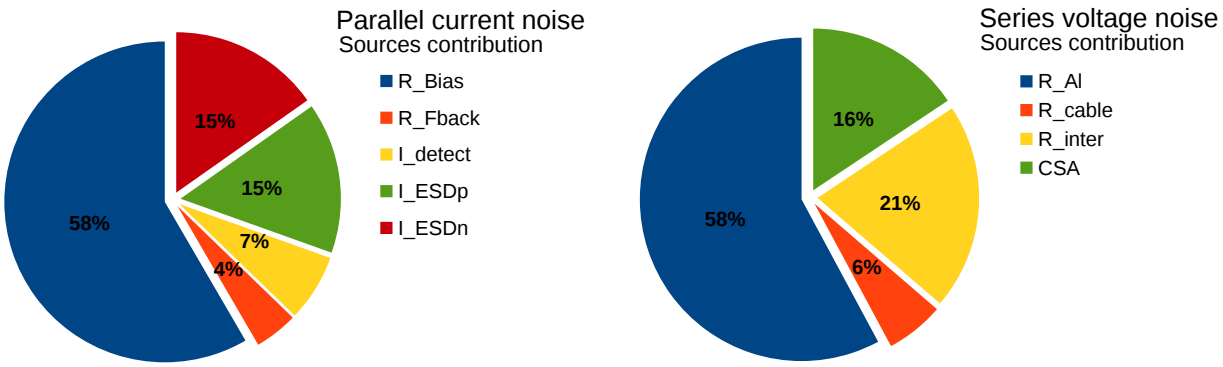
- series $1/f$ noise (e_{nf}^2)

$$e_{nf}^2 = \frac{K_f}{f} \tag{3.7}$$

Table 3.2: *Contributors to the current and voltage noise.*

Parameter	**Typical value**
R_{bias}	1.5 MΩ
R_{fb}	20.0 MΩ
I_{det}	4.0 nA
$I_{ESD_{n/p}}$	9.0 nA
R_{Al}	10.5 Ω/cm
R_{cable}	0.6 Ω/cm
R_{inter}	12.7 Ω
CSA	$\alpha = 0.5, \gamma = 1$
	$g_m = 0.044\ A/V$

Figure 3.33 relates the weight of each factor in the groups. This comparative analysis helps to identify the dominant contribution and devise alternatives to reduce their consequences. The parameters used in this calculation are presented in Table 3.2. For the parallel current noise, the predominant sources are the biasing resistors of the sensors. An alternative way to address this effect can be a small modification in the bias resistor; an increase from 1.5 to 4.5 MΩ can reduce up to 26% its contribution. The voltage noise is principally determined by the resistance of the aluminium traces in the sensor.



(a) *Contributions to the parallel current noise.* (b) *Contributions to the series voltage noise.*

Figure 3.33: *Analytical estimation of the main noise sources in the module readout with the STS-XYTERv2 ASIC.*

The total noise can be obtained by integrating over the relevant range of the amplifier with frequency dependent gain $A(f)$:

$$ENC^2 = \int_0^\infty (i_n^2 + e_n^2 + e_{nf}^2) A(f) df \tag{3.8}$$

Since radiation detectors are typically designed to measure the deposited charge, the system noise level is conventionally expressed as equivalent noise charge (ENC); this is equal to the detector signal that yields a SNR of one. After performing the integration over the whole frequency domain, and considering the total detector and stray capacitance $C_T = C_{det} + C_{cable} + C_{ESDn/p} + C_{PCB}$, this leads to a general formulation of the ENC:

$$ENC^2 = \underbrace{i_n^2 F_i T_s}_{\text{current noise}} + \underbrace{e_n^2 F_v \frac{C_T^2}{T_s}}_{\text{voltage noise}} + \underbrace{F_{vf} A_f C_T^2}_{\text{1/f noise}} \tag{3.9}$$

$$ENC^2 = ENC_i^2 + ENC_e^2 + ENC_{1/f}^2 \tag{3.10}$$

where F_i, F_v and F_{vf} depend on the pulse determined by the shaper and T_s is a characteristic time. For a CR-(RC)^2 shaper, like the one implemented in the slow path of the STS-XYTERv2, these values have been estimated to be 0.64, 0.85 and 3.41, respectively [102]. Since the different noise sources are not correlated, they add quadratically.

Figure 3.34 shows the ENC calculation for two STS detector modules as a function of the peaking time. The dimensions of the module components considered for this estimation are:

- Module 1: Sensor size 6.2 × 6.2 cm^2 and microcable length: 14 cm;
- Module 2: Sensor size 12.4 × 6.2 cm^2 and microcable length: 41 cm.

At small peaking times, the voltage noise dominates, whereas for larger peaking times, the current noise becomes the most significant contribution. The minimum ENC is achievable when both contributions are the same. This corresponds to a peaking time of 170 ns for module 1 and 350 ns for module 2. The overall noise is flattened by the presence of the series $1/f$ noise, which is independent of the characteristic time of the shaper. The contribution of the $1/f$ noise is initially estimated for a bare ASIC, and scaled to the module using the total capacitance. An increase in the detector capacitance enlarges the voltage noise and shifts the noise minimum towards longer

peaking times. For one of the extreme cases of the STS detector (module 2), the expected noise level is in the order of 1600 electrons at the typical shaping time of 90 ns.

The different filter's weighting coefficients (F_i, F_v and F_{vf}) and peaking times can be used for multidimensional ENC minimization based on given conditions of the detector. They also provide a tool for designing pulse shapers that can reduce the effect of current noise in irradiated sensors, where there is an increase of the leakage current [59, 101].

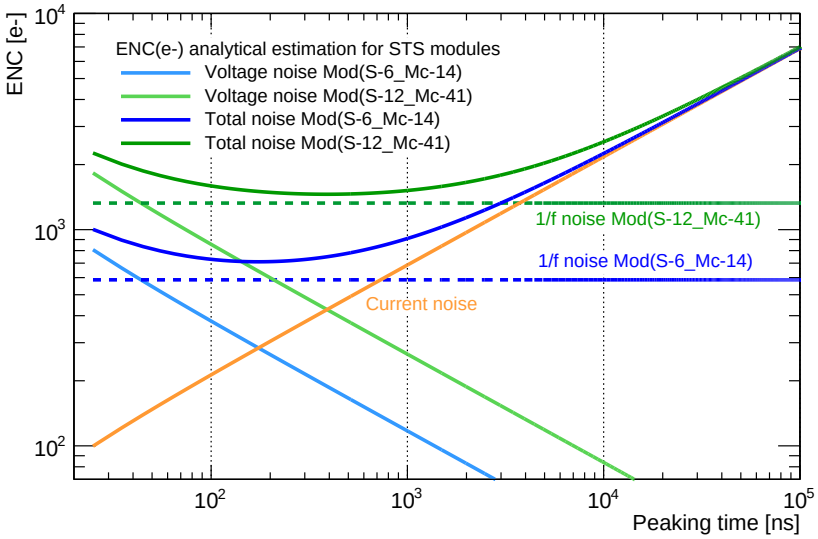


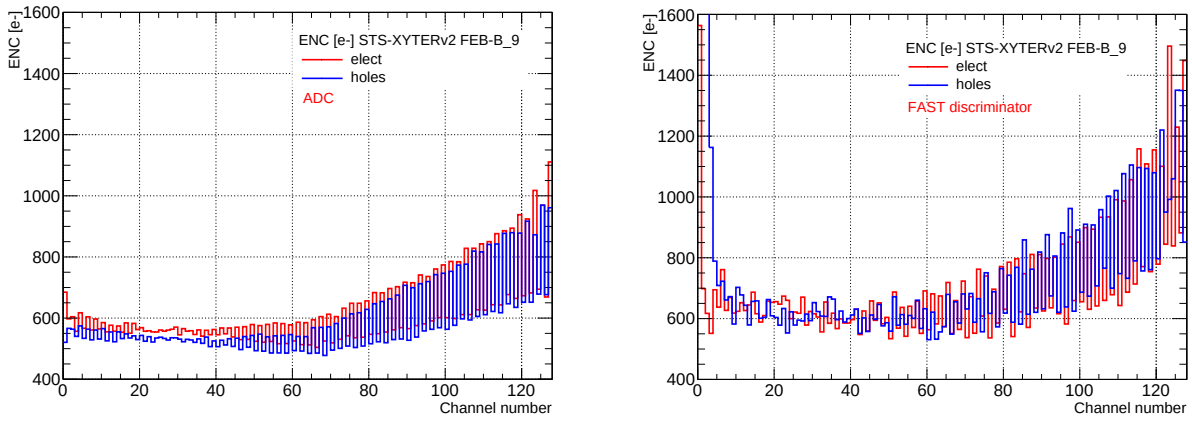
Figure 3.34: *Analytical estimation of the total noise for STS modules as a function of the peaking time. The different noise contributions are calculated for two STS modules (module 1: Sensor size 6.2 × 6.2 cm^2 and microcable length 14 cm; module 2: Sensor size 12.4 × 6.2 cm^2 and microcable length 41 cm.*

3.9.2 Measurement of the noise levels in the STS-XYTERv2

The tests to determine the ENC(e^-) levels for the STS-XYTERv2 ASIC are carried out with multiple ASICs bonded onto the prototype FEBs-B. The noise performance of a single chip in a simple system as the prototype FEB-B, allows to optimize its operation, and to identify critical issues at the chip level that could also affect the sensor readout. Moreover, these tests investigate the dependence of the noise with respect to different factors (see Fig. 3.31), which can be very difficult to check in a more integrated system as a detector module.

The noise measurements rely on the acquisition of the response function from all channel discriminators. The noise is extracted from a *s-curve* scan, where pulses with different amplitudes are injected at the input of the channel's CSA. Although ideally the discriminator response would follow a step function, in reality the distribution is smeared by the electronic noise. The discriminator response is fitted with the complementary error function $erfc(\frac{x-\mu}{\sqrt{2}\sigma})$, where the width is a measurement of the noise amplitude and the mean value indicates the effective discriminator threshold. In every channel, the ADC noise levels are calculated as the average among all discriminators while for the fast path it represents the contribution of its only discriminator. Results from the noise measurement are displayed in Fig. 3.35 for both polarities.

Since a valid hit is only generated when the lowest ADC threshold is exceeded, it is possible to estimate the effective system noise by considering only the contribution of the first discriminator. If a clear separation between the baseline and the first discriminator exists, it is expected that



(a) *ADC noise levels.* (b) *FAST discriminator noise levels.*

Figure 3.35: *Noise levels measured in the FEB-B_9 for the ADC and the FAST discriminator for both polarities.*

no difference can be found among the different discriminators. Figure 3.36 shows the result of repeated noise measurements in all the discriminators of a random selected channel. The noise levels fluctuate across the discriminators, and only small differences, below 50 electrons, can be distinguished between first and last discriminators. These discrepancies can be well included within the error bars of the fitting method. Although the fast path does not determine the system noise, large noise values do affect the precision of the time information.

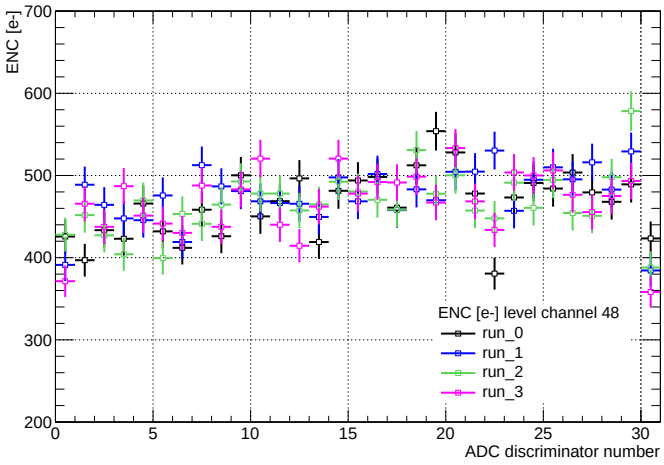
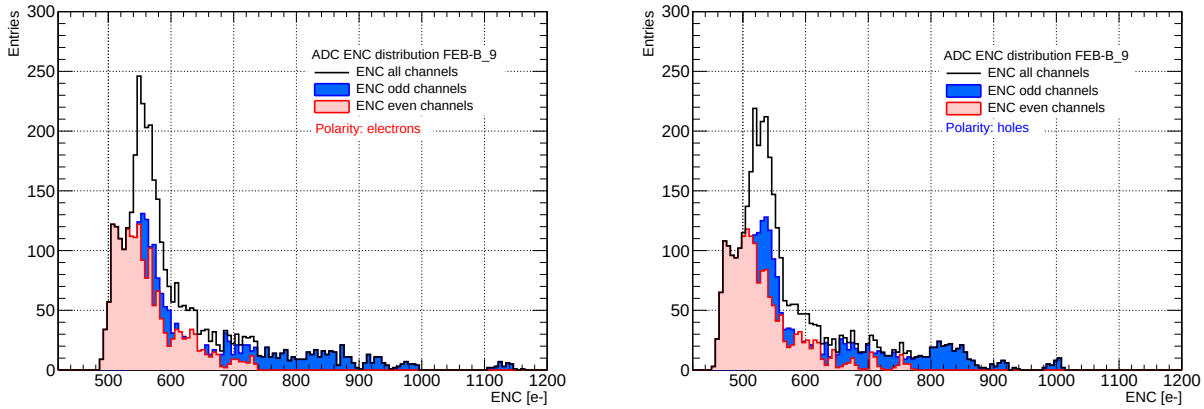


Figure 3.36: *Repeated measurements of the noise levels in every discriminator of a random selected channel of the STS-XYTERv2 ASIC.*

From the measured noise values, depicted in Fig. 3.35, two main findings can be observed: the first one is that absolute noise levels for electrons is slightly larger than for holes, due to the contribution from the polarity selection circuitry, which is bypassed in the case of holes. The second finding is presented as a pattern, showing the different performance of odd and even channels and the absolute noise increment towards larger channel numbers.

A more detailed analysis of the ADC noise is shown in Fig. 3.37. The ENC(e^-) distributions are filled from repeated noise measurements in every channel during 10 hours. The black histogram shows the overall noise, while the contributions for odd and even channels are separated in blue and red colors, respectively. A large difference can be observed between odd and even channels, which can reach up to 35%. This result is independent of the chosen polarities. The origin of this discrepancy has been extensively discussed and can be explained as follows. One of the main current source in the ASIC, used for powering the CSA, is separated in two DACs. This feature is exploited for the readout of the GEM detectors in the MUCH system, because it allows to selectively bias one specific set of channels. The biasing DACs are placed at one side of the chip, closer to channels with larger number. However, there are differences in the filtering scheme of this potential, i.e. for even channels the current is filtered right at the place of the DAC, while in odd channels this current source is filtered after biasing all the CSAs. These features are responsible for the observed difference between odd and even channels. In the revision v2.1 of the ASIC, this effect has been corrected. Figure C.1 in Appendix C illustrates the measured values of the noise for a single STS-XYTERv2.1 ASIC.



(a) *Noise distribution. Electron polarity.* (b) *Noise distribution. Hole polarity.*

Figure 3.37: *Noise levels acquired from multiple measurements in FEB-B_9 for both polarities.*

3.9.3 Effect of low-voltage powering on the ASIC's noise

The powering concept of the readout electronics in the STS conceives that the ASIC power in the front-end will be delivered via radiation hard, low-noise and linear voltage LDO regulators, located on the FEB. In the ASIC design, the tight area and noise requirements imposed the use of a single-ended amplifier instead of a differential one. This approach however, results in a significant susceptibility for power supply related interference. In general, the chip requires two different supply voltages (1.8 V analog and digital and 1.2 V analog). However, the architecture of the CSA uses an input transistor biased with a nominal 2 mA drain current and supplied from the 1.2 V line [69, 86, 103]. Particular attention is given to the CSA biasing since the amplifier contribution is one of the largest to the overall system noise.

The LDO regulators to be used in the final STS will be subject to very high irradiation doses, which can be estimated to be as large as 800 krad over the lifetime [56]. This constraint, together with the very small area and high current requirements on the voltage regulators, has launched the development of full-custom LDOs at the Semiconductor Laboratory SCL Chandigarh, Department of Space in India [103]. The aim of the project is to build a radiation hard, linear voltage regulator

(LTChandigarh) that satisfies the STS specifications: small footprint, high current capabilities and low noise (with special attention to the ASICs power supply noise rejection ratio characteristics).

During the developing phase, multiple prototype front-end boards have been built using commercially available LDOs capable to deliver a performance similar to the one expected in the final system. These devices, although not radiation hard, are suitable for the laboratory environment. The design of the prototype FEB-B makes use of the LT1963 and LT3045 regulators from Linear Technology to deliver the required 1.2 V. Some detailed features of these devices are the following:

- **LT1963:** A low-noise regulator optimized for fast transient response and capable of supplying 1.5 A current [104].
- **LT3045:** Ultra low-noise regulator developed with ultra high power supply rejection ratio for noise sensitive applications [105].

The CSA bias current has major influence on the chip performance and is crucial for the noise reduction. In order to assess its contribution and simultaneously compare the impact of the different regulators, a noise study was carried out. The amplifier current in the ASIC is controlled by two dedicated 6-bit DACs. They allow to change the channels current in the range 0 – 4 mA, with a typical operating value of 2 mA/channel (31 LSB). In addition, they provide another degree of freedom, allowing to power down half the channels of a chip, while operating the others. This feature is of special interest for the MUCH system.

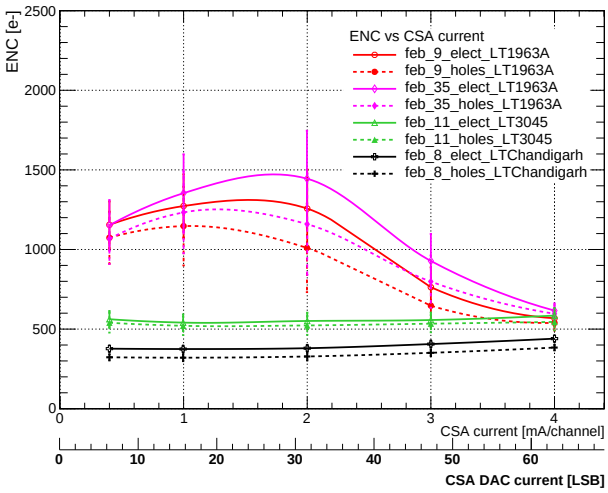


Figure 3.38: *Noise measurement as a function of the CSA current for different linear voltage regulators. Lines are drawn just to guide the eye.*

Figure 3.38 shows the overall noise in the chip, evaluated for several ASICs bonded onto the prototype FEBs-B equipped with different LDOs. Every measurement represents the average across all channels. When using the LT1963, we observe large variations in the noise at different transistor currents. At 2 mA the discrepancies with the expected performance can reach up to 800 ENC(e^-) and the dispersion among channels is larger. This is caused by fluctuations in the baseline of the amplifier, which resonates with the 1.2 V delivered power at a frequency of 220 kHz. This effect increases the contribution of series $1/f$ noise at low frequencies [59]. At larger values of the CSA current (4 mA/channel), these fluctuations are attenuated. The measured noise values are then comparable to those obtained with the FEB-B_11. Therefore, the recommendation is, while using FEB with the LT1963 LDOs, to set the current for the input transistor to maximum.

The FEB-B_11 and FEB-B_8 show the expected performance, where noise levels are kept approximately constant. The small noise rise at larger currents can be associated with a moderate increase of the chip temperature due to a larger power consumption. In the case of the FEB-8, the input bonds have been removed; this is recognized in the lowest noise level. In addition, this FEB carries an early prototype of the LTChandigarh. These results show a good precedent for the future developments of the regulators.

3.9.4 Noise dependency on the input load capacitance

The noise of the pre-amplifier strongly depends on the input capacitive load, i.e. the total capacitance of the detector module (sensor and microcables) [59]. On the final STS detector, multiple combinations of sensor sizes and cables will result in capacitance loads in the range 12-40 pF [106, 107]. For a feedback pre-amplifier such as the CSA of the STS-XYTERv2 ASIC, the signal output amplitude depends on the ratio between the detector and the pre-amplifier input capacitances.

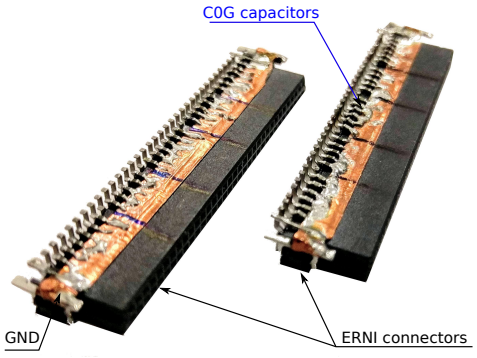


Figure 3.39: *Capacitor boards built with low leakage current C0G capacitors to evaluate the chip response for different load capacitances.*

In order to study the noise dependence on the capacitive load, a set of dedicated capacitor phantom boards is used (see Fig. 3.39). The two boards consist of simple ERNI connectors with 64 pins, where a set of low leakage C0G SMD[9] capacitors ranging from 1 to 40 pF are soldered to the even channels. Capacitors are distributed into groups of five or six devices with the same value. Every capacitance value is cross-checked using a Peak Tech 2155 LCR meter, in order to correct for parasitic values.

During measurements, boards are attached to the first ERNI connector of the FEBs, i.e. channels 0 – 63. Charge pulses are injected at the input of the CSA using the internal pulse generator. Output signals are read out on the dedicated counters of the ADC and the FAST discriminator. Similar studies are carried out for multiple boards in order to cross-check the results.

Figure 3.40 illustrates the noise distribution in the chip with the different capacitor boards. The effect of increasing capacitance is clearly noticeable. As reference, a background measurement (red line) is taken for each FEB-B with a single board where no capacitor has been attached.

The measurement of the noise level as a function of the input load capacitance is shown in Fig. 3.41 for three different ASICs. The rise of the noise levels with the load capacitance is the expected behavior, since the voltage and $1/f$ components of the noise rise with the capacitance. A good agreement is obtained among the different chips used in this study. The experimental data are fitted with a first order regression line, resulting in an average slope of 27.3 ENC(e^-)/pF

[9]Surface Mounting Device

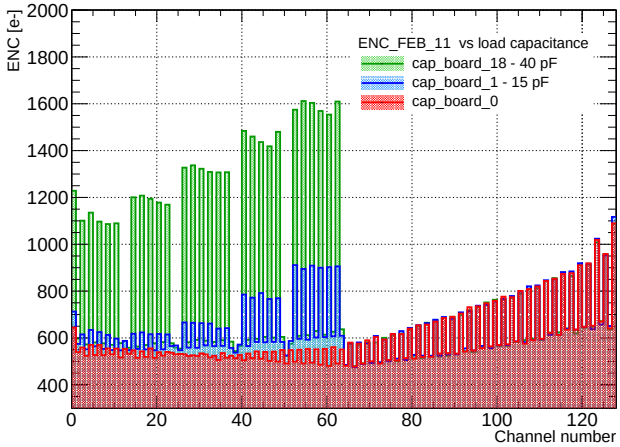
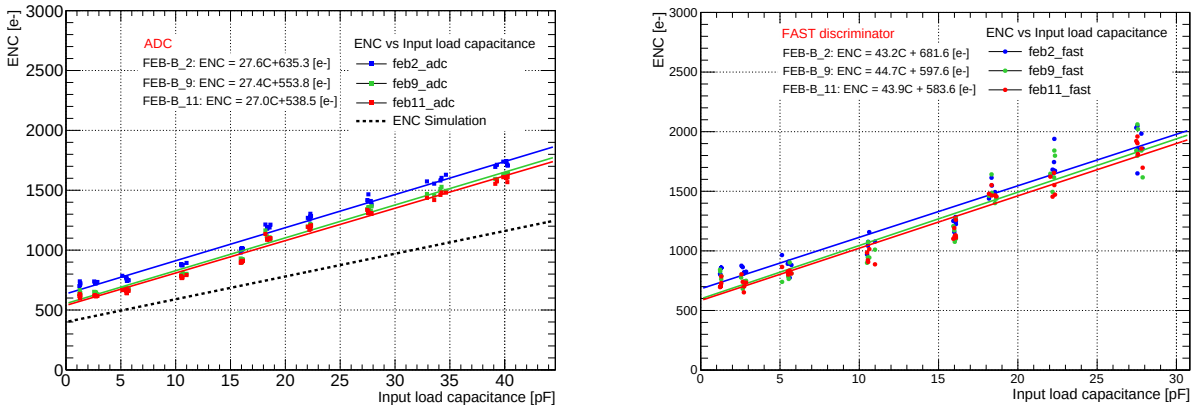


Figure 3.40: *Noise level in the STS-XYTERv2 measured with different capacitor boards.*

and 44 ENC(e^-)/pF for the ADC and FAST discriminator, respectively. The black dotted line represents the expected level from simulations. However, these values are exceeded 1.6 times by the measured ones. This discrepancy can not be explained. The regression average offset ($\sim$570 ENC(e^-)), reproduces the absolute noise level of the STS-XYTERv2 ASIC bonded onto a FEB-B.



(a) *ADC ENC(e^-) vs load capacitance.* (b) *Fast ENC(e^-) vs load capacitance.*

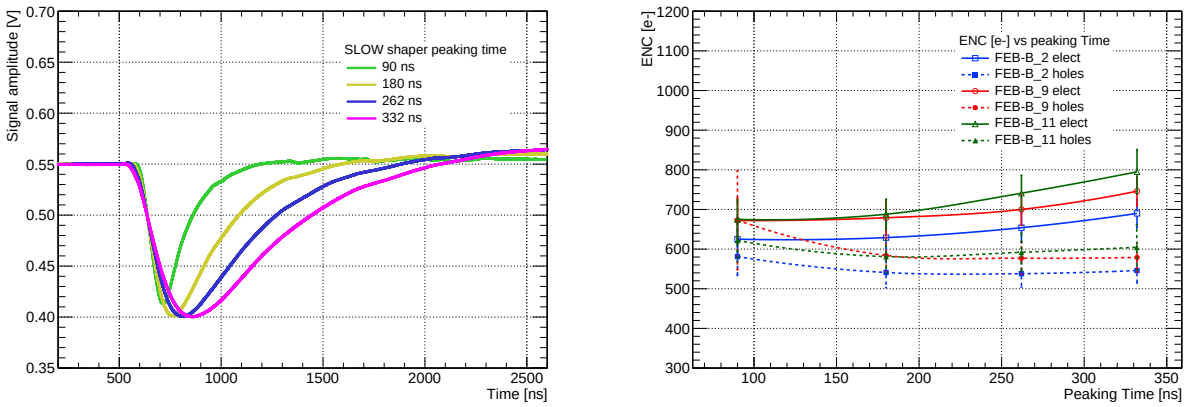
Figure 3.41: *The dependence of the noise measured as a function of the load capacitance.*

3.9.5 Noise dependency on the slow shaper peaking time

The design of the slow shaper [CR-(RC)^2] enables the selection of multiple peaking times. This feature is exploited to trade off between speed and noise [96, 100]. In addition, it is a key design parameter as it dominates the noise bandwidth, and it must accommodate the sensor response time and the hit rate. The optimum choice of a pulse shaper for a given application is based on the trade-offs performance among factors such as SNR, counting-rate behavior, sensitivity of rise-time fluctuations of the input signal and the suitability of the output pulse-shape for feeding a pulse height analyzer [59].

The time duration of a signal arriving at the input of the readout electronics is determined by two processes: the charge carrier collection time in the detector material and the pulse stretching in the transmission lines. In 300 μm thick non-irradiated silicon sensors, the collection time for electrons and holes is approximately 10 and 30 ns, respectively. To estimate the stretching of the signal in the transmission lines, we consider an extreme case of the final STS, where a 12 cm silicon sensor will be read out by a 41 cm long microcable, resulting in a total series resistance of approximately 30 Ω and capacitance of 37 pF [106, 107]. Therefore the signal stretching is $R_{Cable}C_{Total} \approx 1.2$ ns, which can be considered negligible.

In the slow shaper of the STS-XYTER, the selection of the signal peaking time is user-controlled via a 2-bit DAC (FS = 0..3). This register modifies the resistance values in the pulse processing chain that establishes the corresponding integration time (from nominal τ_p = 90 ns to 270 ns in 4 steps). The output waveforms for all possible settings are shown in Fig. 3.42a. Typical input signals of approximately 4 fC (holes polarity) are applied at the channels input. Waveforms are collected with a Tektronik 4054 oscilloscope. The measured peaking times are τ_p = 90 ns, 180 ns, 262 ns and 332 ns [85].



(a) *Slow shaper waveforms for different peaking times.*

(b) *Average ENC(e^-) as a function of the slow shaper peaking time.*

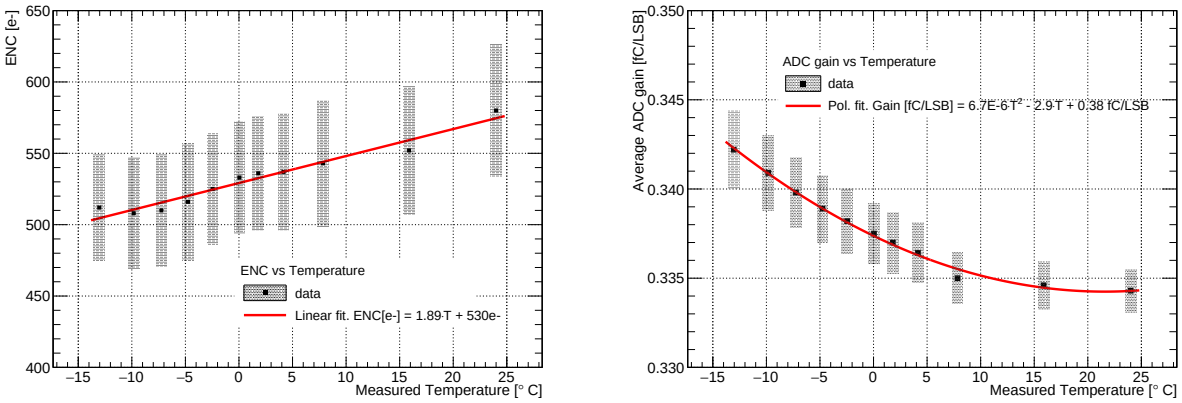
Figure 3.42: *Noise dependency on the slow shaper peaking time. a) Exemplary slow shaper waveforms for different peaking times. Positive input signals with amplitude Q_{inj} = 4 fC are applied at the channels input. b) Measurements of the ASIC's noise for different peaking times.*

The noise as a function of the peaking time is shown in Fig. 3.42b. These measurements are taken with three different ASICs, bonded in the prototype FEBs-B. Every point represents the average among all channels and error bars illustrate the spread. Even with large error bars, there is an evident divergence between electrons and holes. We consider that such difference is mainly due to the contribution of the PSC, which is present in the electron processing chain.

3.9.6 Noise and ADC gain dependence with chip temperature

Figure 3.43 shows the noise and gain dependences in the STS-XYTERv2 ASIC as a function of the temperature of the ASIC. During the measurements the chip is operated in a thermal enclosure that allows to control the temperature within a range of ±1℃. The chiller temperature is changed from -15 ℃ to 25 ℃ in different steps. After setting every temperature value, enough time is allowed for reaching the thermal equilibrium. The ASIC temperature is monitored via its corresponding thermistor and cross-checked using a reference probe placed at the bottom of the prototype FEB-B. The thermal monitoring circuit implemented in the chip is calibrated as described in section 3.5.

Overall noise and ADC gain are estimated for every temperature step as the mean value among all the ASIC channels. The vertical error bars correspond to the standard deviation. A linear fit of the electronic noise indicates the dependence with the chip temperature, with a variation of approximately 1.89 ENC(e^-)/℃. Similar results are obtained for other STS-XYTERv2 ASICs during the same tests. Since the expected temperature variation among the different ASICs in a FEB-8 is expected to be less than 15℃ [108], the noise and gain uncertainties for this range can be estimated to be below 30 ENC(e^-) and 0.002 fC/LSB. Therefore no correction is applied in subsequent tests.



(a) *Linear noise dependence with temperature.* (b) *ADC gain as a function of the temperature.*

Figure 3.43: *Dependence on the noise and ADC gain in the STS-XYTERv2 with the operation temperature.*

3.9.7 ASIC bonding mechanical protection. Noise for different glop-top materials

In the integration of the STS modules, several kinds of adhesives and protecting glues are used. According to their particular application, they differ in their consistency, viscosity, curing methods and mechanical strength. In addition, they are required to be radiation hard and thermally stable during the whole life cycle of STS [109]. The properties listed above can be considered as the main characteristics to test and select the proper glues.

To protect the wire bonds used to connect the ASIC to the FEB, a layer of protective glue is applied. It consists of a combination of two glues with different viscosities. At first, a rectangle dam is built around the ASIC with the higher viscosity glue, which is subsequently filled with a low viscosity glue. In this case an insulating, fast-curing adhesive is used to fully encapsulate (glob-top) the chip. During the research phase, different materials have been tested in order to choose a suitable candidate to be used in the final system. Another relevant property for comparison is

their effect on the performance, more specifically on the noise level of the ASICs.

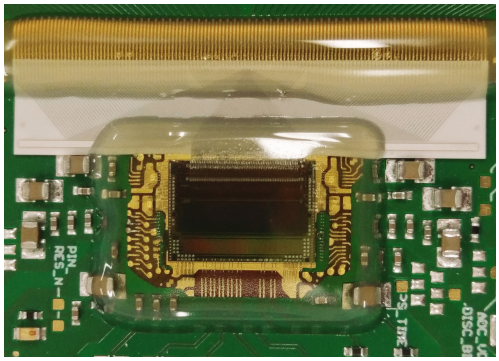


Figure 3.44: *STS-XYTERv2 ASIC bonded onto a prototype FEB-B and protected with Polytec UV 2257 glob-top glue.*

The characterization procedure consisted of measuring the overall noise before and after the application of the glob-top material. The different glues used in this study have several properties in common such as low viscosity, fast-curing under UV light, good resistance to temperature shock loads and excellent adhesion to printed circuit boards (PCB). UV-curing glues have the advantage of fast curing (few minutes), while curing processes in the oven take almost two hours and can affect the PCB negatively. The selected material for building the rectangular dam around the chip is Polytec UV 2249. Three different filling materials are examined during the tests: Polytec UV 2257 [110], Epo-tek 302 [111] and Dymax 9008 [112]. Candidates are selected by searching for commercially available glues matching the specified criteria. The glues from the three vendors have the advantage to be transparent, and hence the bonds quality can still be controlled. Figure 3.44 shows a picture of the STS-XYTERv2 ASIC mounted in a prototype FEB-B completely enclosed with the glop-top material.

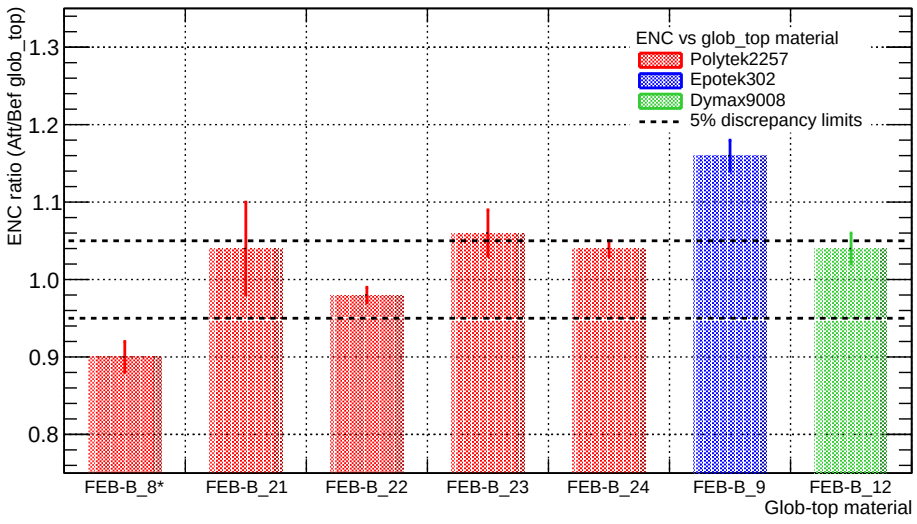


Figure 3.45: *Noise measurement as function of the ASIC bonding protective materials.*
** Input bonds on FEB-B_8 has been removed.*

The noise ratio (after/before the application of the glob-top) was measured for seven ASICs. Figure 3.45 shows the results for the selected materials. The error bars represent the standard deviation of the ratio among all channels. The unity value, which coincides with the expectations, indicates that the ASICs noise performance is not affected by the application of the glue. Two uncertainty bands are drawn to illustrate the 5% fluctuation limits. All the tested glues were found suitable for the protection of the readout chips because their contribution to the overall noise was not significant. Among the materials, the Polytec UV 2257 and Dymax 9008 show the best results within the selected limits. The extensive use of the Polytec UV 2257 and its easier manipulation has made it the preferred material for the assembly procedure.

This test intends to shed lights on the performance of the STS-XYTERv2 ASIC after the application of different protective glues. Other tests, such as radiation tolerance and thermal behavior of the glues, are mandatory in order to build a selection criteria.

3.9.8 Noise stability in the STS-XYTERv2

For a long-standing experiment, a reliable performance in time is considered to be an important parameter. Long-term stability tests study the noise evolution over time for a single STS-XYTERv2 ASIC and contribute to identify sources of malfunction that might not be easy to find during short running periods. Variations in the noise levels can result as a consequence of faulty ground connections, unstable biasing sources, connection of high consuming devices in the same power line, electromagnetic interferences or fluctuations in the chip working temperature.

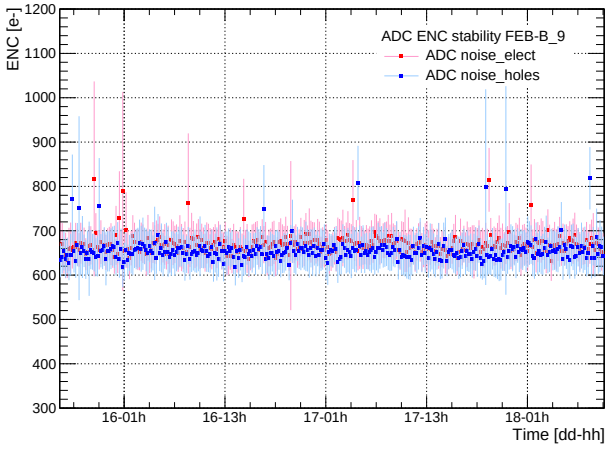


Figure 3.46: *Noise stability test carried out with a chip bonded in a prototype FEB-B. Measurements were taken every 12 minutes.*

Tests are carried out using a single ASIC bonded in a prototype FEB-B. Noise measurements for electrons and holes polarities are taken every 12 minutes for approximately 72 hours. The results are illustrated in Fig. 3.46. Every point represents the average noise value among all the even channels in the chip and the error bars indicate the spread.

Along the monitoring period, only small variations can be distinguished in both polarities. They are randomly distributed and their amplitude represent approximately 100 $e^-/650\ e^- = 15\%$ of the mean value. No significant fluctuation is observed during the test, which is considered as a satisfactory result.

3.10 Summary

The STS-XYTERv2 is a custom designed ASIC developed for the readout of the double-sided silicon sensors of the STS detector. The characterization of the chip is one of the major steps before its operation in the full readout chain. This chapter was devoted to describe some of the fundamental functionalities of the chip, to implement calibration procedures for the analog circuit and to extensively evaluate the noise performance of the ASIC.

The calibration of the ADC and FAST discriminator was a complex process, where multiple chip functionalities were used. Some of the most crucial steps can be summarized as follow:

- the calibration was carried out using the internal pulse generator. The operation of the generator showed a good linearity in the expected range (up to 14.5 fC) with small deviations, below 1% among different chips;
- the calibration procedure was based on the acquisition of the response function for all discriminators in every channel. This procedure, referred in the text as a *s-curve* scan, searched for the individual threshold that represents a switching point in the discriminator response. The outcome is an ASIC specific calibration matrix of 128 $\times$ 32 values;
- the accuracy of the procedure was evaluated as a function of the number of injected pulses and running time. The optimal results were achieved by injecting at least 50 pulses in the calibration of the ADC and 100 pulses in the FAST discriminator. These values defined a minimum running time of approximately 360 s per ASIC;
- in the optimization of the procedure, it was found that more than 98% of the running time corresponded to write/read actions, limited by the speed of the slow control protocol, based for the time being on the IPBus communication protocol. Another important constraint is the internal pulse generator, which allowed to excite only 32 channels simultaneously;
- verification and reproducibility of the results were checked using an external pulse generator and a gamma source. In addition, the stability of the calibration parameters were tested in a long run.

Among the multiple operation requirements of the STS-XYTERv2 ASIC, the noise performance is of paramount importance. The characterization of the chip noise was carried out as a function of a large number of parameters such as: low-voltage power regulators, input capacitance, shaping time, temperature and bond's protective glue. These studies allowed to optimize the configuration settings and to identify possible malfunctions on the low voltage powering scheme. The dependence of the noise with the detector capacitance showed significant discrepancies with simulated values. Moreover, serious differences were found among odd and even channels, which main cause laid behind the bias scheme of the CSA for the two groups of channels. This last effect was corrected in the v2.1 of the ASIC. The contribution of the different noise sources were also analytically estimated.

Within this chapter, some of the most important requirements in the chip design, tests and operation results have been highlighted. The tests and procedures discussed here represent essential elements to understand the content of the next chapters.

Chapter 4

Radiation hardness studies of the STS-XYTERv2 ASIC

Radiation damage to electronic components is an important consideration for the experiments at the future FAIR accelerator facility. In the CBM-STS detector, the front-end electronics are located outside of the physics acceptance. Nevertheless, they will be exposed to high charged particle fluxes. Considering the SIS100 running scenario, the lifetime dose at the location of the electronics is expected to not exceed 800 krad. In order to ensure proper functionality in this hostile environment and to reduce Single Event Effects (SEE), the ASIC implements a radiation hard architecture for the configuration settings of every channel and other critical global settings.

The purpose of this chapter is to describe the effects of radiation on highly integrated electronics. Special attention is drawn to test the radiation hard design of the STS-XYTERv2 ASIC and to evaluate its performance after a lifetime irradiation. It also intends to improve the understanding of upset events in the chip, to measure their cross section and to provide a detailed feedback to the chip designers in order to mitigate their occurrence in the new version of ASIC.

4.1 Phenomenological description of radiation damage in integrated circuits

The long-term performance of electronic devices in a radiation environment depends on the level of damage caused by the impinging highly energetic particles. Since no technology yet exists for developing completely immune integrated circuits, the decision for a specific architecture must consider the possible operational and irradiation scenarios and their effects. When designing a front-end chip, two important goals must be considered regarding radiation hardness: to withstand the damaging effects of the total irradiation dose (TID) and to achieve a robustness against SEE.

Nowadays, the usage of Metal-Oxide-Semiconductor (MOS) processes has become the optimal technology due to the wide availability, reduced leakage currents and their low price compared to bipolar developments. The availability of Complementary MOS (CMOS) processes with structure sizes of less than 350 nm and their high radiation tolerance, has further driven the use of standard CMOS as a basis for the development of radiation hard microelectronics [113, 114, 115]. One of the preferred technologies for ASIC developments is the 180 nm UMC CMOS process. Several front-end electronics for different CBM detector subsystems, are developed using this technology (STS-XYTER for STS [85], PADI for ToF [116], SPADIC for TRD [117]), leading also to synergies in prototype-production cycles of the various devices.

4.1.1 Total irradiation dose

Cumulative radiation effects occur during the complete lifetime of a transistor as long as it is exposed to radiation. The total ionizing dose effects are caused by passage of charged particles. Neutrons and γ-radiation do not ionize directly, but they can induce ionization by energy deposition.

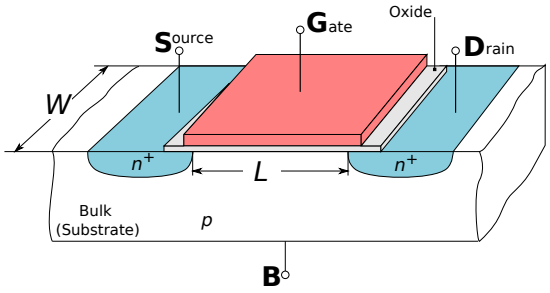


Figure 4.1: *Structure of a nMOS transistor.*

In contrast to bulk devices like e.g. silicon sensors, MOS structures are surface devices. Their implants penetrate only a few micrometers into the bulk. The primary sources of MOS device's degradation are damages in the surface layers caused by ionization effects [113, 118]. The most sensitive part of a MOS field effect transistor is the thin insulation layer (silicon dioxide) between the silicon substrate and the electrodes, see Fig. 4.1. Underneath the gate electrode (gate oxide), the insulation layer is only a few nanometers thick increasing to some tens of nanometers above the source and drain diffusion regions (field oxide).

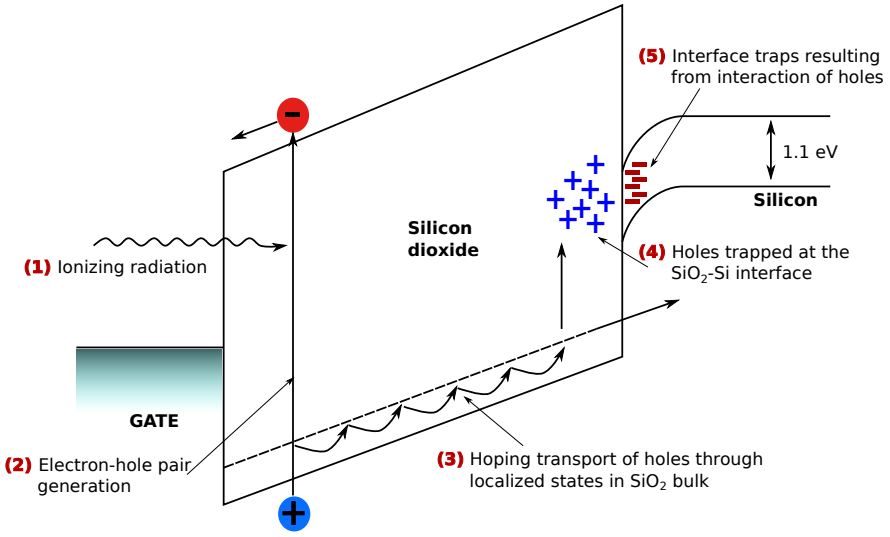


Figure 4.2: *Mechanism of radiation damage in MOS transistors [118].*

The two major radiation induced effects in MOS transistors can be classified as the trapping of holes in the silicon oxide near the $SiO_2 - Si$ interface and the creation of $SiO_2 - Si$ interface traps, which produce inter-bandgap states in the silicon [113, 118]. The mechanisms of the generation, distribution and trapping of the holes and electrons in the silicon oxide are visualized in Fig. 4.2. They can be understood as follow: when an ionizing particle passes through a MOS transistor (Fig. 4.2 ①) electron-hole pairs are generated (Fig. 4.2 ②). In the gate (metal or polysilicon) and in the substrate the electron-hole pairs quickly disappear since these are materials of small

resistance. In the oxide, which is an insulator, electrons and holes have different behaviors as their mobilities differ by five to twelve orders of magnitude [118]. A fraction of the radiation-induced electron-hole pairs will recombine immediately after being generated. The rest of the electron-hole pairs, which do not recombine, are separated in the oxide by the electrical field. In case of a positively biased gate, the electrons drift to the gate in a very short time (order of picoseconds). The holes movement towards the $SiO_2 - Si$ interface (Fig. 4.2 ③) is in the order of 1 s at room temperature. Close to the interface, but still in the oxide, some of the holes may be captured in long-time traps, giving origin to a fixed positive charge in the oxide (Fig. 4.2 ④). This causes a negative voltage shift that can persist in time from hours to years.

Effects on the performance of trapped charges in the gate oxide depend on the transistor type. In an nMOS transistor, the field of the positive trapped charges (holes) adds to the one that is generated by supplying a positive voltage to the gate. In a pMOS transistor, the trapped holes attenuate the electrical field generated by a negative voltage applied to the gate.

In an nMOS transistor, trapped holes in the field oxide at the interface to the silicon can create a leakage path from the source to the drain of the transistor. Figure 4.3 *left* illustrates the current path in a standard transistor geometry. The size of this parasitic leakage current rises with the total amount of holes trapped in the lateral oxide, and therefore with the TID. The absolute value of the leakage current depends on the detailed geometrical structure of the lateral oxide and can hardly be predicted. Several methods to prevent the rise of the leakage current in nMOS transistors due to ionizing radiation have been reported [113, 119]. Most of them use different processing steps and manufacturing techniques to achieve the goal. When processes with structure sizes of 350 nm or less became available, the approach of closed gate structures has become an alternative. By using a gate geometry as pointed out in Fig. 4.3 *right*, any leakage path between source and drain under the field oxide of the transistor is avoided [119]. This method, known as enclosed layout transistor (ELT), has the price of a larger area for transistors. Also, modeling of the effective behavior of enclosed transistors is not as well established as for standard transistor geometries. This approach has been used in the design of the analog front-end of the STS-XYTERv2 as an experimental trial to improve the TID immunity [85].

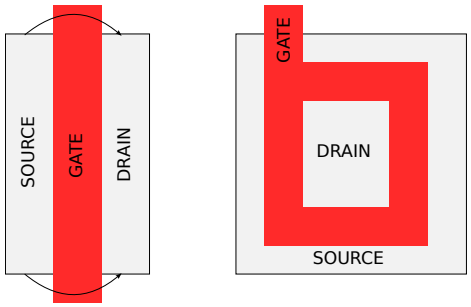


Figure 4.3: *The parasitic leakage path between source and drain as in a regularly laid out transistor (left) is prevented in an enclosed layout transistor (ELT) (right).*

Another radiation effect in MOS devices is the increase of the trap density at the $SiO_2 - Si$ interface by several orders of magnitude (Fig 4.2 ⑤) [113]. These traps have an energy level between the valence and the conduction bands of the silicon. They can act as acceptors or donors, according to their position relative to the midgap. Therefore, the threshold of both n-channel and p-channel MOS transistors, changes in absolute value after irradiation due to the creation of new interface traps. The creation depends on different parameters like dose and dose rate, electric field, temperature, radiation energy, oxide thickness and others. The consequences on the transistors behavior manifest as three important effects:

- shift in the threshold voltage;
- decrease of mobility and transconductance;
- increase of leakage currents.

4.1.2 Single Event Effects

In contrast to cumulative ionizing effects, SEEs manifest instantaneously. They are caused by the released charge of single particles passing through a sensitive node in the device. The deposited charge can be collected by drift and diffusion in semiconductor structures, causing current transients that can result in circuit malfunction. The actual effect occurs very localized, but can propagate across the whole system. SEE can be classified depending on their impact on the systems behavior:

- transient effects: yield asynchronous signals, which propagate through the system. They can appear in analog as well as in digital circuits and can become static if they are latched;
- static effects: change the content of a memory cell;
- permanent effects: are destructive events that cannot be recovered. In some cases, they can be prevented by a fast current limitation.

In high energy physics experiments and aerospace applications, SEE induced by heavy ions, protons and neutrons become an increasing limitation of the reliability of electronic components, and have stimulated abundant past and undergoing work to understand and develop mitigation techniques [115, 119]. Of great interest for the future FAIR experiments are the so-called Single Event Upset (SEU), since they limit the reliability of the electronic systems and affect their functionalities [120].

A SEU is the instantaneous reversible modification of the logic state of an elementary memory cell like a Static Random Access Memory (SRAM) cell or a Dynamic flip-flop (DFF) [114, 121]. It is induced by the charges created along the track of an incoming ionizing particle (electron-hole pairs produced by Coulomb-scattering with the lattice atoms). Charges are then collected in a sensitive node of the circuit due to the electrical field giving rise to a current spike [122, 123]. This current has two components:

- a fast component, in the order of 100 ps that results from the electron-hole pairs drift in the depletion region of the pn-junction;
- a second component which is rather slow (in the order of ns) and arises from the diffusion regions outside of the active area.

Depending on the energy loss of the ionizing particle, the current spike can be rather large, and the impact on the circuit cannot be neglected. The number of electron-hole pairs created in the silicon depends on the total amount of energy deposited in the matter by the incident particle or recoil nucleus. This amount is related to the Linear Energy Transfer (LET) from the particle to the material. The LET depends on the type of particle, its energy and on the absorbing material. It is expressed by:

$$LET\ [MeVcm^2mg^{-1}] = \frac{1}{\rho_{Si}}\frac{dE}{dx} \tag{4.1}$$

where ρ_{Si} is the density of the silicon material and dE/dx is the mean energy transferred to the material per unit path length. To determine the amount of charge created, the total absorbed energy is divided by the energy needed to create an electron-hole pair in silicon (3.6 eV).

The minimum LET needed to change the state of a given device e.g. a *flip-flop*[1], is called critical or threshold LET. It depends strongly on the fabrication process of the device. It can be theoretically estimated by knowing the minimum charge, injected in a node, that is necessary to alter its state. The critical charge (Q_{crit}) depends on the load capacitance of the node.

$$LET_{crit} = \frac{Q_{crit} \cdot 3.6}{e^{-}\rho_{Si} d} \tag{4.2}$$

where d is the depth or thickness of the material for the collection of the charge. If the incident particle has a LET higher than the critical LET, the device will be vulnerable to SEUs. Particles that have low LET and do not create enough charge for a SEU to occur (like protons or pions) can initiate nuclear reactions, whose recoil products are heavy enough to produce direct ionization.

Two experimental measurements can be done in order to test the chip sensitivity to SEUs. One is to measure the upset rate by placing the device in a working environment similar to the real experiment. The second one, and most commonly used, is to expose the device to a beam of heavy ions (e.g. O, Li, Na) that have a large stopping power, or hadrons such as protons, pions or neutrons. The radiation environment of the future CBM experiment has an energy spectrum that covers a wide LET range.

SEUs are then characterized using a beam of known particle species and energies. An accepted method is to evaluate the upset probability in a so-called beam threshold measurement. The threshold is defined as the minimum perturbation that produces an error in the test device, and the upset cross section is the maximum sensitivity to SEU caused by the ion beam. The upset cross section σ is then calculated as:

$$\sigma = \frac{N_{SEU}}{\Phi \cdot t} \tag{4.3}$$

where N_{SEU} is the absolute number of upsets during the time interval t and Φ is the particle flux.

The dependence of the SEU cross section from the incident ion LET can be described by the Weibull function. This function has no underlying physical significance but provides a convenient method for parametrizing data and extracting the threshold LET (LET_{thr}) as well as saturated cross section (σ_{sat}) [124]. It is given by:

$$\sigma = \sigma_{sat}\left\{1 - exp\left[-\left(\frac{LET - LET_{thr}}{W}\right)^{s}\right]\right\} \tag{4.4}$$

where s and W are free parameters.

Figure 4.4 shows an exemplary result from the measurement taken with the APV25 readout ASIC used in the CMS experiment [124]. This curve represents the Weibull fit for the SEU data of the pipeline circuit of the chip. The measurement was performed with different ion species at 100 MeV/u energy.

4.2 Radiation hard design of the STS-XYTERv2 ASIC

The architecture of the STS-XYTERv2 ASIC is designed to mitigate the effects of SEU and to steadily operate in a heavily irradiated environment during the lifetime of the detector. The version 1 of the ASIC was previously tested in a dedicated high-intensity proton beam line. Based on the test results [125], the cell layout was improved towards better SEU immunity.

[1] *Flip-flop* or latch is a circuit that has two stable states and can be used to store state information.

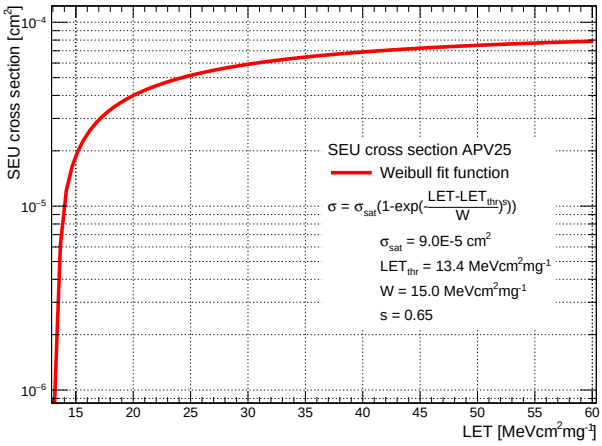


Figure 4.4: *The Weibull function and the SEU cross section measurements performed on the APV25 chip[124].*

The front-end of the STS-XYTERv2 ASIC is designed using nMOS ELT transistors to reduce the influence of the TID. Moreover, channel's registers are based on dual interlocked storage cell (DICE) and *flip-flops*. Even if traditional *flip-flops* are not suitable for this environment, they are only used for complementary counters. DICE cells, on the contrary, store the discriminator threshold values and the common global settings for all ASIC channels. These represent all the relevant functionalities of the analog front-end. SEU protection of the digital back-end is enhanced by using logic triplication for the registers and data parity in FIFO-based circuits of the data path [126]. The Triple Modular Redundancy (TMR) implies that every register is triplicated. The register state is decided by a majority-voting system. In case of a bit upset in one of the three registers, the other two can correct and mask the fault. This method, although simple, is very robust, easy to implement and widely used in high energy applications [67, 127, 128]. In addition, the ASIC implements a SEU counter for the file registers [96, 90].

DICE cells have redundant storage nodes and restore the cell original state when a SEU error is introduced in a single node [114, 115]. The probability that multiple nodes are affected by an upset is low, making the DICE latch less sensitive to SEUs. However, for highly scaled processes as the UMC 180 nm, where the transistor sizes are very small, the data in this latch can be corrupted by SEUs due to charge sharing between adjacent nodes [114].

4.3 Evaluation of the SEU tolerance in a proton beam

During the operation of the STS detector, the front-end electronics will be exposed to high particle fluxes, which rises concerns that the ASIC will occasionally suffer from SEU. In these cases, devices require to be re-configured in a reasonable time that depends on the severity of the error. These reasons motivated the study of the chip radiation hard design in an extensive irradiation campaign, which main goals were:

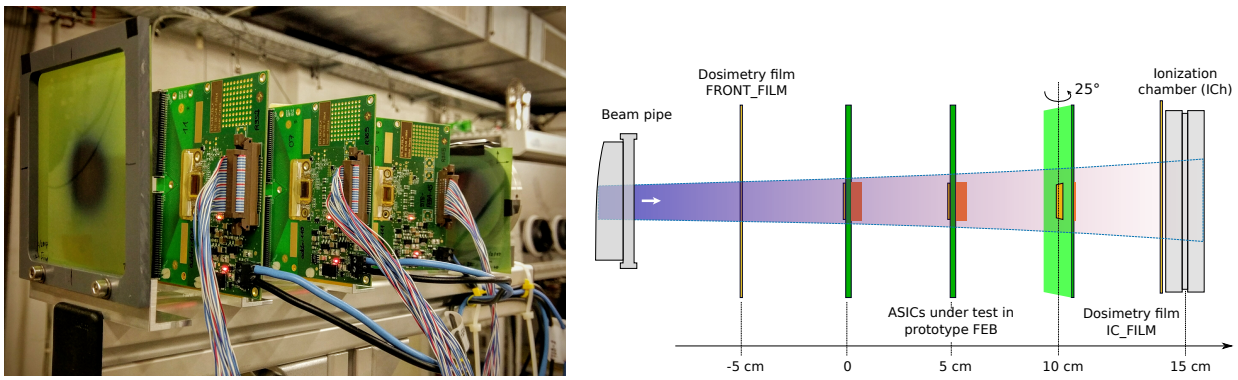
- to characterize upset errors for DICE and *flip-flop* architectures;
- to determine the relative improvement by using DICE cell architecture instead of *flip-flops* and to compare results with the STS-XYTERv1 ASIC;

- to measure the absolute SEU cross section using beam intensity monitor;
- to estimate the absolute SEU rate for the STS in CBM.

Irradiation tests were carried out in a high-intensity proton line at the COoling SYnchrotron (COSY), Research Center Jülich (Germany) [129]. The facility has been used for multiple detector and electronics studies within the CBM collaboration. The synchrotron delivered a low-spread momentum beam of protons at 1.6 GeV/c. The duration of each spill was in average 4.5 s in a super-cycle of approximatively 18 s. The beam intensity was varied in the range 2-8·10^9 protons/spill, a good compromise between sufficient statistics and a stable readout interface. The tests were done for a total of 45.5 hours of effective irradiation.

4.3.1 Experimental setup

Figure 4.5 illustrates the test setup for SEU evaluation. Three STS-XYTERv2 ASICs bonded onto prototype FEBs were placed in the beam line. During the irradiation, the beam arrived to the first two chips with an incident angle normal to the die area. The third ASIC was tilted 25° with respect to the beam axis, which corresponds to the typical incident angle in the final STS detector. Two gafchromic dosimetry films [130] were fixed along the beam path for monitoring the beam profile at the front and back of the FEBs. An ionization chamber (ICh) with a charge to frequency (QFW) based readout [131] was placed behind the ASICs to provide a continuous measurement of the beam intensity.



(a) *Picture of the test setup at the beam line.* (b) *Schematics of the beam setup.*

Figure 4.5: *Experimental setup for SEU tests in the STS-XYTERv2 ASIC at COSY.*

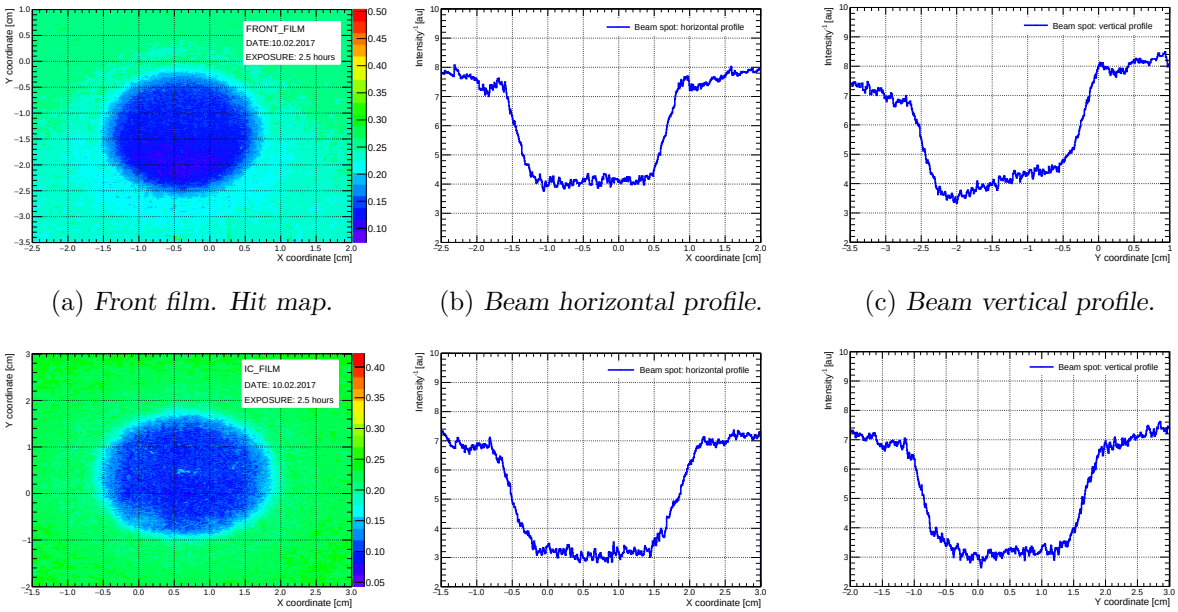
The FEBs were interfaced by a gDPB FMC card to a standard readout and control chain with an AFCK processing board implementing the protocol-tester firmware. Register status were read out using the ASIC command path over IPBus connected to the acquisition computer. The test procedure monitors 32240 bits of DICE cells and 48360 bits of *flip-flops* per chip as a reference, arranged in a two dimensional array of 8-bit and 12-bit registers, respectively. They correspond to the 31 ADC discriminators and counters from all channels (128 + 2 test channels). The chip addresses were hardware encoded as 5, 6 and 7.

4.3.2 Beam monitoring system

The beam monitoring tools represent an important element in the experimental setup. The system alignment, the determination of the TID and a proper measurement of the SEU cross section depend on them. For monitoring the beam profile, two radiochromic films were placed at the beginning of every run. The films were placed upstream of the first ASIC and right in front of the ICh. They were not used to estimate the total dose for two main reasons. The first one is due to the very high irradiation doses at which they were exposed; this causes saturation and the loss of the color grading sensitivity. Secondly, they require a dose calibration, which was not done because time limitations during the experiment.

Films were analyzed with ROOTv5.34 [132] framework after being digitized using a 300 dpi resolution scanner. Results from a 2.5 hours beam exposure are shown in Fig. 4.6. The hit maps exhibit a color saturated area, where the spot size can be estimated. The full width at half maximum (FWHM) of the X-Y beam profiles have more than 2.0 cm in diameter. This value is considered sufficiently good as the beam covers the full chip area 0.67×1.0 cm^2, and fits within the acceptance of the ICh.

The beam spot has an ellipsoidal shape, whose area can be determined considering the vertical (a) and horizontal (b) profiles. To estimate the dimensions, profiles were fitted using a convolution of a Gaussian and square function. The area was determined as $A = \pi ab$, resulting in 4.81 ± 0.48 cm^2 right in front of the ICh.

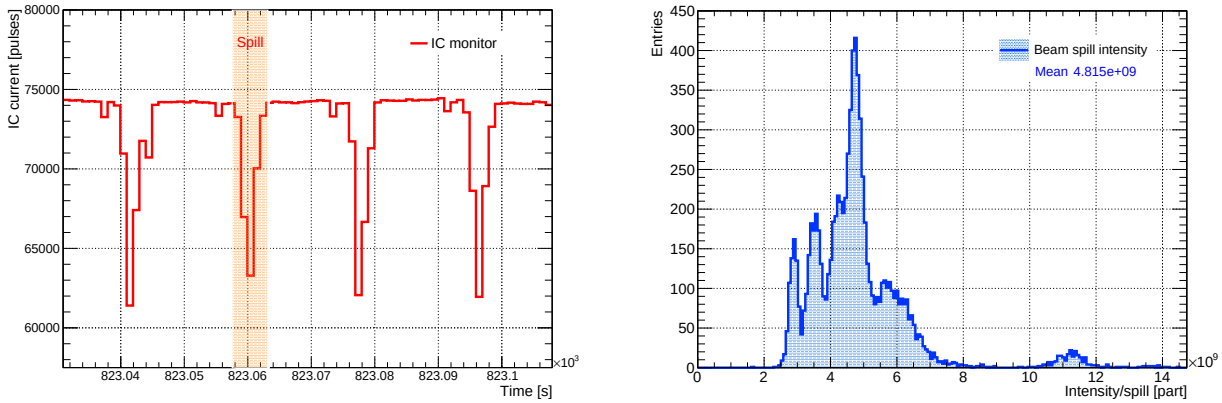


(a) *Front film. Hit map.* (b) *Beam horizontal profile.* (c) *Beam vertical profile.*

(d) *ICh film. Hit map.* (e) *Beam horizontal profile.* (f) *Beam vertical profile.*

Figure 4.6: *Analysis of the dosimetry films, exposed during 2.5 hours.* ***Top:*** *Front film.* ***Bottom:*** *ICh film. Horizontal (middle) and vertical (right) profiles show that the beam spot size is larger than the ASIC dimensions.*

The beam intensity was continuously measured with an ICh. The active volume of the detector consists of a thin air gap of 1.31 cm thickness at atmospheric pressure. The current pulses created by the radiation passage are amplified and integrated onto a 2.5 pF capacitor and digitized in a QFW, giving a charge resolution of 2.5 pC. The output frequency increases linearly with the input current and provides a large dynamic range [131, 133, 134].



(a) *Beam spill structure.* (b) *Distribution of the spill intensity.*

Figure 4.7: *The beam intensity is continuously monitored using an ionization chamber with QFW readout.*

The integrated signal from the ICh is read out every second, allowing to uncover the spill structure of the beam. An example is illustrated in Fig. 4.7a, where the spill has an average length of 4.5 s. To determine the number of crossing particles, the spill area is integrated and normalized it with a factor $\eta = 18414$ *particles/pulse*. The η factor is calculated taking into account the energy losses of protons in the detection volume and the feedback capacitance of the input amplifier. The dependency of the energy losses of protons in the air gap of the ICh is shown in Fig. 4.8. It also shows the magnitude of the losses in 300 μm of silicon, representing the ASIC thickness. The black points mark the energy losses of 1.6 GeV/c protons used in this study. Values of the mean energy loss are taken from the NIST Standard Reference Database [135].

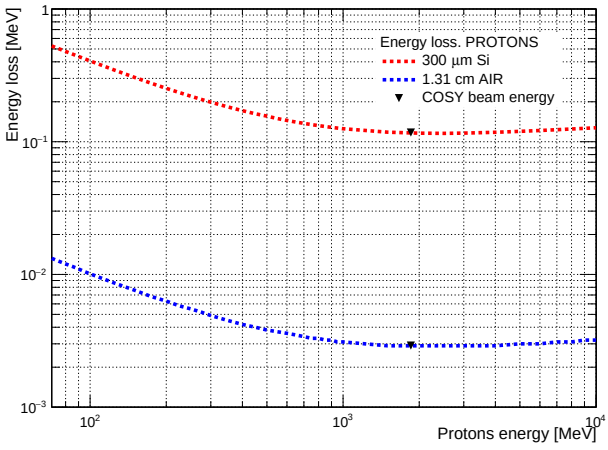


Figure 4.8: *Energy loss of protons in the ASIC and the air gap of the ionization chamber with 300 μm and 1.31 cm thickness, respectively. The black points mark the energy of the proton beam used in this study.*

Over the full data taking period, the beam intensity fluctuates in the range $2.5 \cdot 10^9$ to $1.2 \cdot 10^{10}$ protons/spill; this is shown in Fig. 4.7b. Values higher than $8 \cdot 10^{10}$ protons/spill are correlated with beam optimization periods. The cumulative intensity along the full irradiation period is shown in Fig. 4.9. The total number of particles was estimated to be $4.07 \cdot 10^{13}$ protons.

Considering the beam profile and the ASIC area, the total absorbed dose can be estimated as approximately 250 krad.

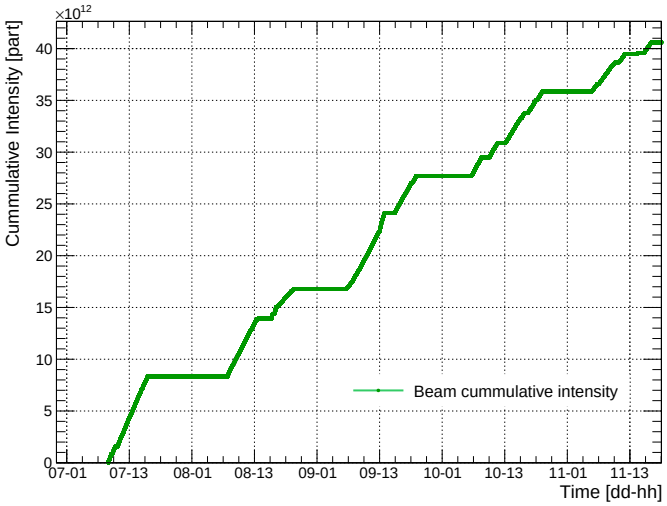


Figure 4.9: *Cumulative intensity monitored with the ionization chamber.*

4.3.3 SEU read-back procedure

The different steps of the SEU monitoring procedure are illustrated in the flow diagram depicted in Fig. 4.10. The read-back procedure consists of the following phases:

- before starting the irradiation procedure, the ASICs are configured. Fixed 8-bit patterns are set in all trim registers. These patterns have been chosen because they have an alternate sequence of states and are DC balanced (01010101 and 10101010). The default value in every *flip-flop* counter, which can not be directly written, is set by injecting a predefined number of test pulses in the ASIC;
- the ASICs are continuously read-back during irradiation. The procedure is done sequentially, starting from ASIC level, channels, discriminator trim values and finally counters. Repeated register read-back allows to distinguish SEUs from errors in the read-back. The read-back process takes approximately 10 s for the whole system;
- when repeated read-backs show identical values but different from expected ones, it is considered that a SEU error has occurred;
- the next step depends upon whether the SEU is in the DICE cells or in the *flip-flops*. In case a trim value is corrupted, the system writes back the original patterns. If a counter is affected, the read-back value becomes now the default one. The system is then ready to continue.

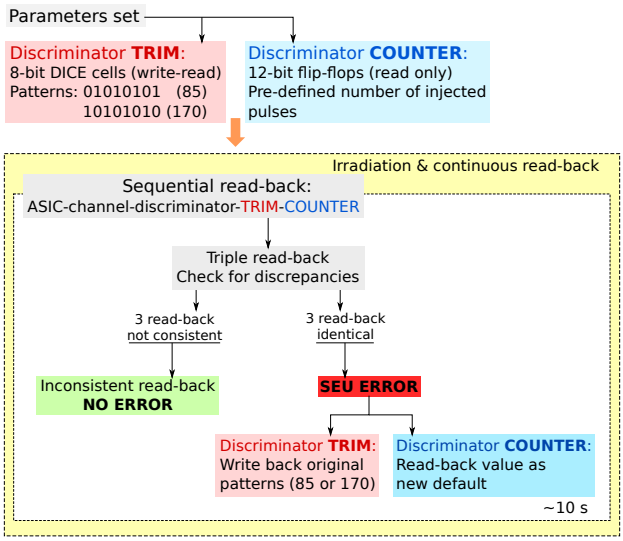


Figure 4.10: *Flow diagram of the SEU read-back procedure.*

4.4 Results of SEU error measurements in the STS-XYTERv2

SEU errors in numbers

During the irradiation tests, the total number of SEU errors registered was 758 and 75057 for DICE cells and *flip-flops*, respectively. The distribution of SEUs per ASIC is displayed in Table 4.1. The first data column is reserved for the test results from version 1 of the ASIC [125]. The factor $(flip-flops/DICE)$ provides a direct quantification of the relative SEU rate between DICE and *flip-flops*. The value is normalized to the number of bits for the different architectures. This also allows to confirm the improvements implemented in the new version. A significant enhancement of the SEU immunity of factor 2 is observed with respect to its predecessor.

Table 4.1: *Number of SEUs registered during irradiation tests.*

	STS-XYTERv1	**STS-XYTERv2**			
	Addr:0	Addr:5	Addr:6	Addr:7	Total
Flip-flops	3467	30406	18150	26493	75057
DICE cells	116	288	223	247	758
*Ratio**	29.9	70.4	54.3	71.5	66.0

** Ratios are normalized to the number of bits for the different architectures.*

Two-dimensional histograms show the distribution of SEU errors across the chips. They are presented for DICE cells in Fig. 4.11 and for *flip-flops* in Fig. 4.12. Histogram bin sizes are increased to help to recognize patterns in the distribution of SEU in the chips. Every upset event can be tracked down to the discriminator level and thus to the geometrical location on the chip. The 2D maps contribute to identify the most irradiated areas in the ASICs. Since all channels are identical, the distribution patterns can only result from the position of the ASICs with respect to the beam. For DICE cells this effect is not visible because of the low statistics.

Flip-flops on the contrary, show that channels in the range 0 - 63 and discriminators between 0 - 15 sustained higher damage than the rest of the chip. The pattern is consistent for all ASICs.

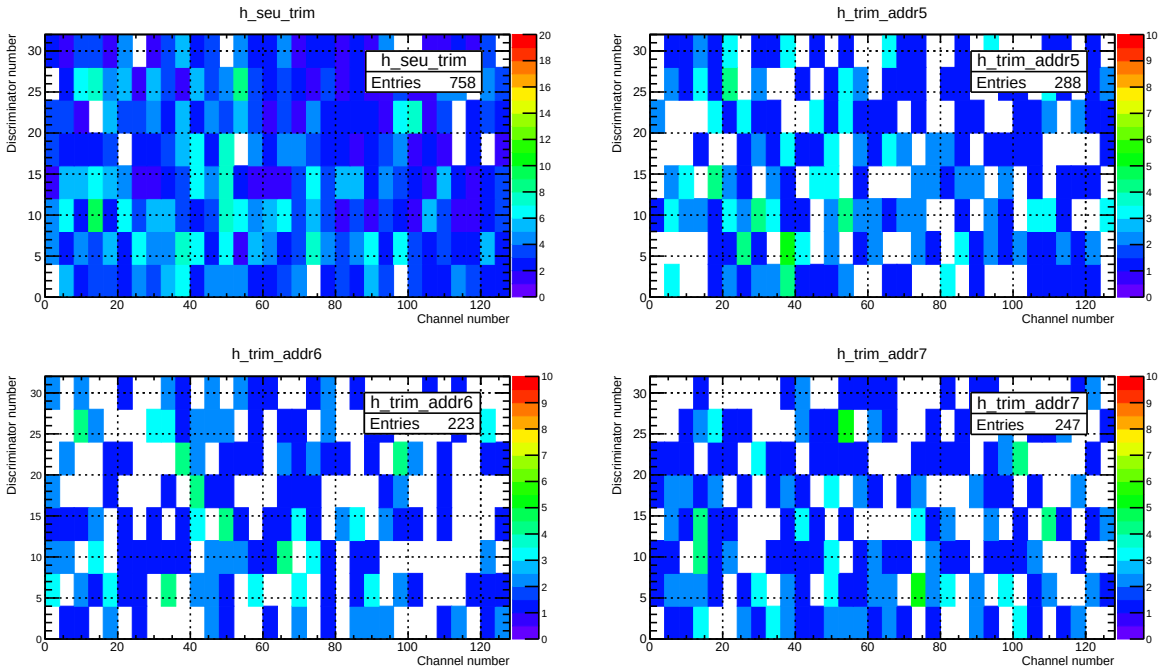


Figure 4.11: *Distribution of SEU for DICE cells within the tested ASICs..*

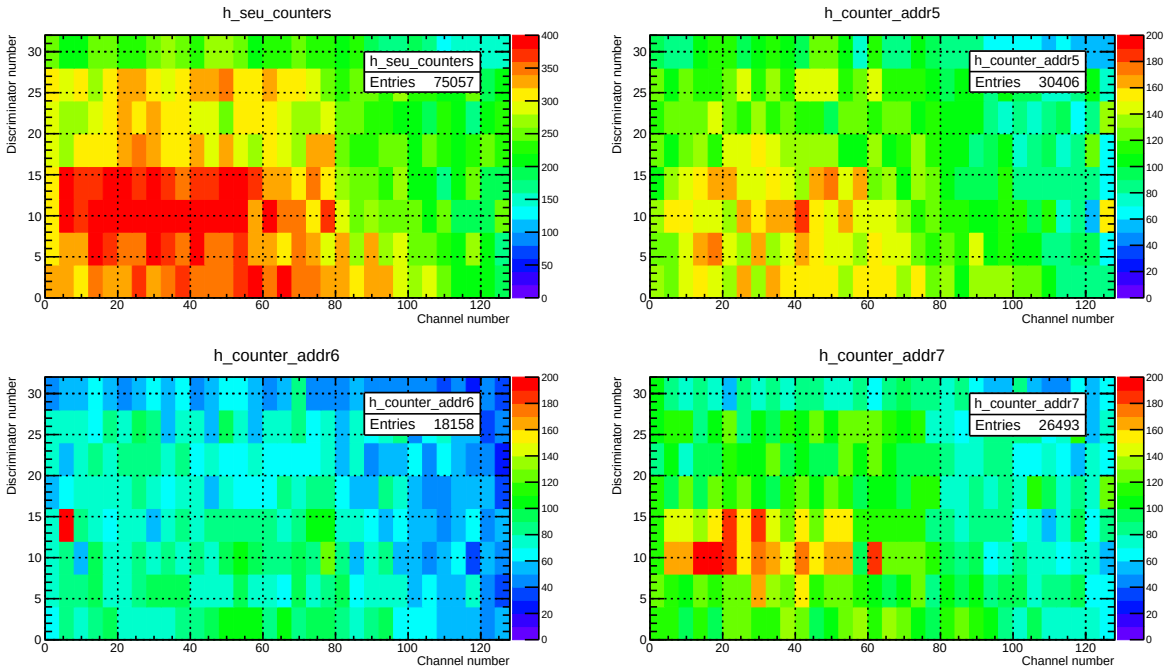
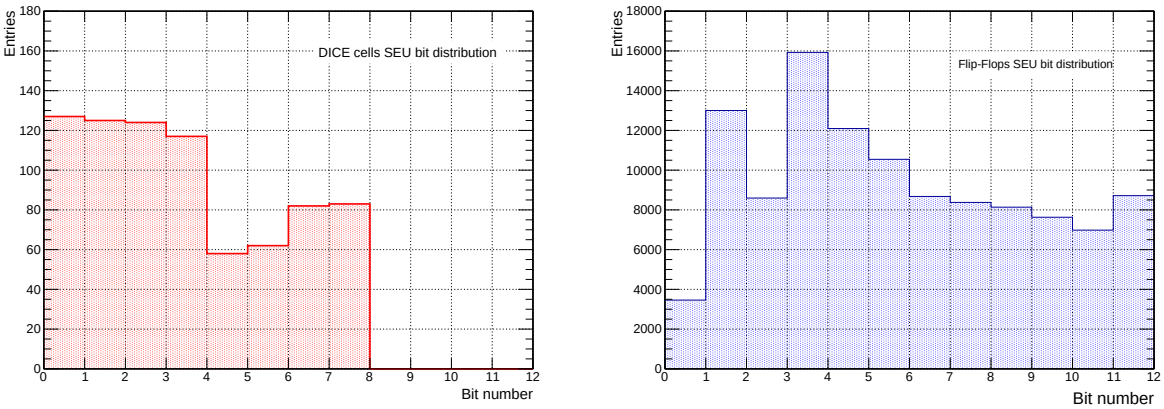


Figure 4.12: *Distribution of SEU for flip-flops within the tested ASICs. Due to the beam position, counters corresponding to lower discriminators of the first channels experience more SEU.*

SEU distribution within a cell

This study also allows to look into the SEU distribution within a register. The architecture of the DICE cells and *flip-flops* can be inspected regarding the probability of bit flips, the multiplicity of the event and the flip orientation (i.e. 1 to 0 or 0 to 1). The distributions of SEUs as a function of the bit number within the registers are shown in Fig. 4.13. Both architectures exhibit differences among the bits. The large fluctuation in the first 4-bits of the *flip-flop* architecture is not well understood. DICE cell results are of crucial importance since they are responsible for storing the threshold values. A substantial discrepancy between the first 4-bits with respect to the last ones can be correlated with the asymmetry in the potential connection to the guard rings in the ASIC layout. Figure 4.14 shows the structure of an 8-bit DICE cell array built from 8 identical latches. The resulting imbalance makes bits 0 - 3 more vulnerable to SEUs.



(a) *SEU distribution in 8-bit DICE cells.* (b) *SEU distribution in 12-bit flip-flops.*

Figure 4.13: *Distribution of SEU within a cell for the implemented architectures (DICE cells and flip-flops). Difference among bits might be correlated to power asymmetries.*

Multiplicity of SEU errors

When a SEU error occurs and more than 1 bit flips in the same structure it is called multiple bit upset (MBU). MBU can be related to multiple factors:

- a particle traverses the device at an angle very close to 0° with respect to its surface, crossing in this way the sensitive volume of more than one cell;
- a particle strikes the device almost perpendicularly (90°) but has enough energy to change the information contained in more than one sensitive node;
- two particles hit two adjacent cells, modifying the information contained in them.

The multiplicity of SEU errors can be studied to determine the probability of MBU and their size. Figure 4.15a shows the measured SEU size distribution. The mean values 1.03 and 1.50 for DICE cells and *flip-flops*, respectively, show that single bit flip is the most probable outcome in a SEU event. The probability of having a MBU in two different DICE cells is approximately 0.7%. However, for standard *flip-flops*, this value is around 30%.

Since the state of a cell is defined by setting a fixed pattern, the probability that a bit flip occurs in any direction (i.e. 1 to 0 or vice-versa) should be the same. The recorded data, depicted

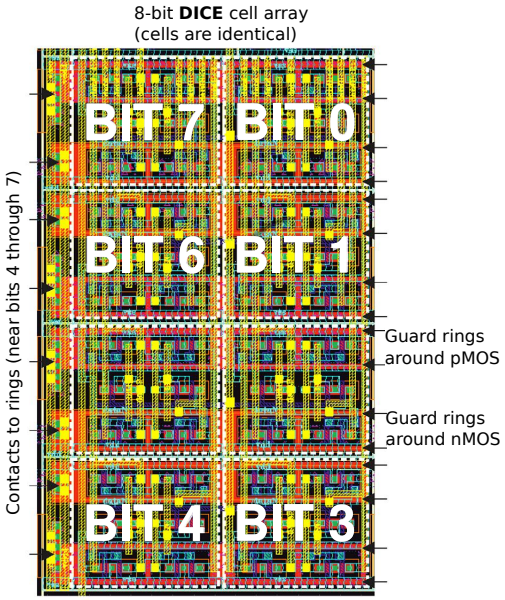
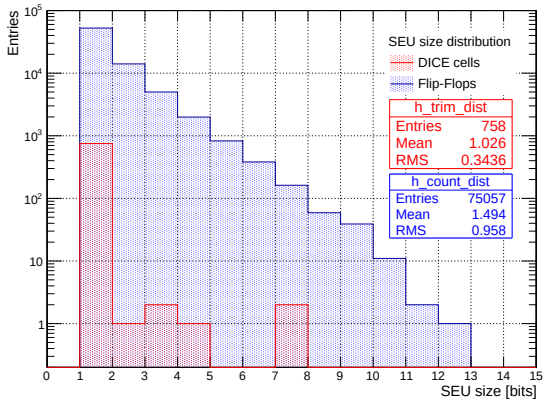
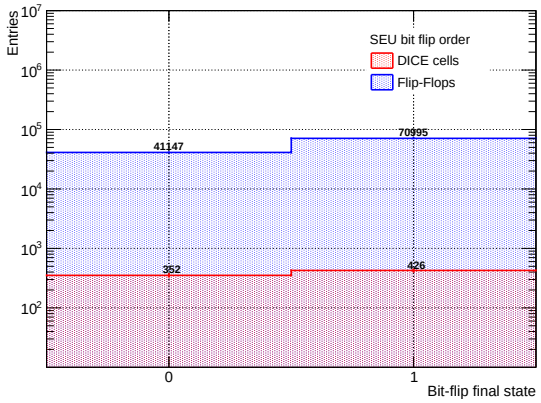


Figure 4.14: *The implementation of the 8-bit trim registers uses 8 identical DICE cells. There is an asymmetry regarding the number of guard ring contacts between the first and the last 4-bits.*

in Fig. 4.15b, illustrates the number of bit flips in both directions for the tested architectures. It shows that for DICE cells, bit flips in the order 0 to 1 are more likely to occur. In the case of *flip-flops* the data require to be normalized to the number of bits in every state. The final probabilities are then expressed as cross section values and discussed in the next subsection.



(a) *SEU size distribution.*



(b) *Bit flip orientation.*

Figure 4.15: *Multiplicity of SEU errors. a) SEU size distribution in the tested architectures. b) Bit flip orientation in numbers. For DICE cells, data do not require normalization since the number of bits for both states is the same. In the case of flip-flops, the data require to be normalized to the number of bits in every state.*

4.4.1 SEU cross section and uncertainty estimation

The average cross section is estimated considering the total number of SEU errors divided by the fluence Φ and the number of tested latches. This can be expressed as:

$$\sigma = \frac{N_{SEU}}{\Phi \cdot N_{latches}} \tag{4.5}$$

The total number of tested latches per chip is 32240 and 48360 for DICE cells and *flip-flops*, respectively. Integrating the flux over the whole irradiation time, a total of $4.07 \cdot 10^{13}$ protons crossing an area of 4.8 cm^2 is obtained. This leads to the following cross section values:

$$\sigma_{DICE} = (9.26 \pm 0.98) \cdot 10^{-16} \text{ cm}^2/\text{bit}$$
$$\sigma_{flip-flops} = (6.11 \pm 0.61) \cdot 10^{-14} \text{ cm}^2/\text{bit}$$

The cross section results are consistent with literature values [114]; they also confirm that typical *flip-flops* are two order of magnitude more sensitive to SEU errors than DICE cells. When determining the absolute cross section for bit flip orders, it is necessary to normalize the upset counts to the total number of bits in every state. For DICE cells, since it is possible to write the desired pattern, the number of bits is the same for 0 or 1 state. In the *flip-flops* architecture, no defined value can be written on the counters, therefore it is necessary to always consider the number of bits in every state before the occurrence of a SEU. By examining the cross section for bit flip orders, shown in Table 4.2, we can deduce that DICE latches are more perceptive to "0 to 1" upsets, contrary to *flip-flops* behavior.

Table 4.2: *SEU cross section according to bit flip order.*

	SEU cross section [cm^2/bit]	
	0 to 1	1 to 0
Flip-flops	$(8.41 \pm 0.84) \cdot 10^{-14}$	$(1.07 \pm 0.11) \cdot 10^{-13}$
DICE cells	$(1.04 \pm 0.12) \cdot 10^{-15}$	$(8.60 \pm 0.98) \cdot 10^{-16}$

There are major contributions to the statistic uncertainty in the cross section measurement. The measurement of the flux relies on the determination of the total number of primary protons ($N_{protons}$) detected by the ICh, and the size of the beam spot area. The latter has been obtained based on the measurement with the dosimetry films. Another uncertainty is related to the number of detected SEU events. The generation of a SEU in the chip has an underlying stochastic mechanism, since charge deposition, diffusion and collection within a silicon cell are intrinsically probabilistic processes. Some systematic errors are related to the detection efficiency of the ionization chamber, which was assumed to be 100% at the operation voltage. This uncertainty can be considered smaller than the ones described above and its contribution it is not taking into account. The total cross section error is then estimated as:

$$\left(\frac{E_\sigma}{\sigma}\right)^2 = \left(\frac{1}{\sqrt{N_{SEU}}}\right)^2 + \left(\frac{1}{\sqrt{N_{protons}}}\right)^2 + \underbrace{\left(\frac{\Delta A}{A}\right)^2}_{\text{Beam spot area}} \tag{4.6}$$

4.4.2 Radiation environment of the CBM experiment

A fundamental tool to understand the requirements for the experiment in terms of radiation hardness are the simulation studies of the radiation environment. They shed lights on the expected damage that detector and readout components should withstand while operating. Calculations of the ionizing dose, non-ionizing energy loss, and hadron fluxes in all areas of the CBM cave have been performed using the FLUKA [136] simulation framework [137]. The results discussed below correspond to one of the worst CBM running scenario at SIS100. In the simulation it has been considered minimum bias collisions of a high intensity beam (10^9 Au ions/s) and kinetic energy of 11 AGeV in a 1% Au interaction target. The system is set in the CBM-MUCH configuration, where the radiation level in the STS stations is slightly higher than in the CBM-RICH configuration, due to the backscattering effect in the first muon absorber layer.

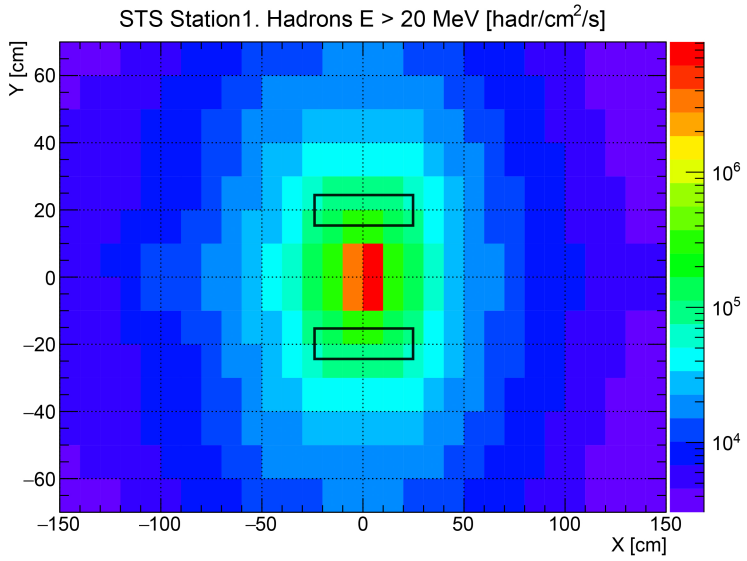
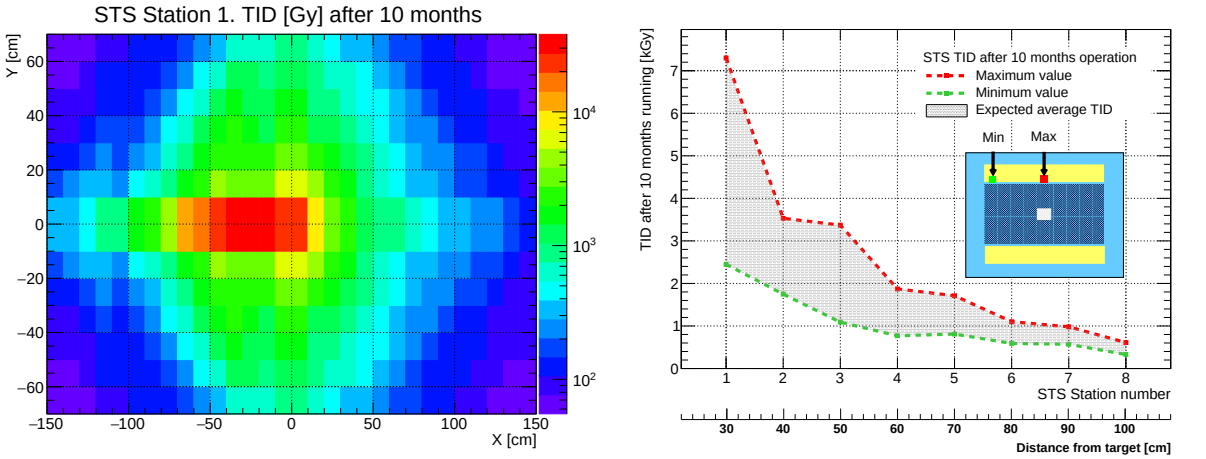


Figure 4.16: *Flux of hadrons with $E > 20$ MeV in the plane of the first STS station placed at 30 cm behind the target. The areas occupied by the front-end electronics are highlighted in black. Simulation performed using FLUKA framework [137].*

Figure 4.16 illustrates the flux of hadrons with energy larger than 20 MeV traversing the area of the first STS station at 30 cm downstream the target. The areas occupied by the front-end electronics are indicated in black lines. The proximity of the first station to the target results in higher flux of hadrons, therefore, a larger number of SEUs is expected.

In the determination of the TID (STS Station 1), it is considered 10 months of continuous operation in the conditions described above, see Fig. 4.17a. Even if this might differ from the real running scenario, it allows to establish an upper limit for the conditions. The dose, as well as the hadron flux, is also a function of the radial distance from the beam and it varies moderately over the area covered by the front-end electronics. The most exposed ASICs of the first station receive a maximum ionizing dose of 7.3 kGy over 10 months at 10 MHz interaction rate.

Figure 4.17b shows how the dose decreases with the distance from the target. The red dotted line represents the maximum estimated dose in every station; it was calculated at the center of the electronics plane. The green line describes the trend of the minimum dose, evaluated at the furthest position of the electronics place with respect to the beam axis. The shadowed area marks the expected average TID for every station plane. The noticeable difference between upper and lower limits in the first station decreases towards the last ones.



(a) *2D map of the TID in the first STS station.* (b) *Calculated TID limits for the STS stations.*

Figure 4.17: *FLUKA simulations of the TID in the STS detector [137].*

4.4.3 SEU rate in the CBM experiment

From the operation point of view, only DICE cells performance is of crucial interest in the STS detector. The full AFE control in the chip is based on this architecture. For simplicity, this study only uses the ADC trim registers, however, the FAST discriminator and other global references are also built using the same type of DICE cells. They represent a total of 35946 bits/chip.

Considering the running scenario of the CBM experiment at SIS100, it is possible to predict the rate of SEUs based on the calculated flux of hadrons. The results are shown in Fig. 4.18 where values are normalized to the number of ASICs in every station. In the calculation, some assumptions are made:

- only the registers of the analog ADC and FAST discriminator are considered (34816 bit/ASIC). This value represents 98.1% of the total number of bits in the AFE;
- the average LET for all particle species is the same as for the protons in this study, which allows to use the measured cross section;
- the hadron flux in every station is considered homogeneous across the area occupied by the front-end electronics.

The approach followed in this study was to estimate the extreme cases of the SEU rate based on the upper and lower limits of the hadron flux. The prediction of a more accurate value is a complex task that requires the exact knowledge of the SEU cross section for the different energies and particle species. In addition, the flux over the area varies with the radial distance, which implies a difference of twice the value between the hottest and coldest spot in the first stations, see Appendix D. Therefore, the assumption of a homogeneous field is not entirely correct. A more precise description would also require the exact position of every ASIC and hence a finer granularity in the simulations.

The study of the extreme cases (maximum and minimum values), illustrated in Fig. 4.18, is a simplified approach that can contribute to our understanding of the occurrence of SEU in the STS detector. The prediction of less than 1 SEU/ASIC/day is in general a good result. This does not imply a total immunity to errors, but it shows that ASICs can reliably operate in the

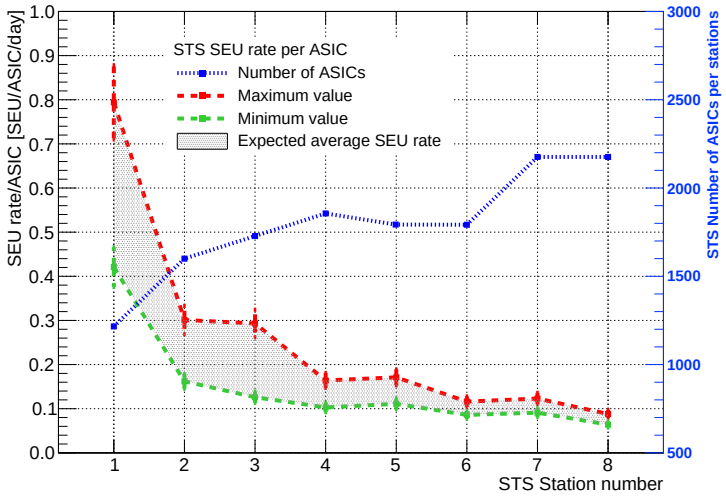


Figure 4.18: *Estimated SEU rate in the STS stations. Values are normalized to the number of ASICs per station. Two scenarios are considered in this study based on the FLUKA calculations of the hadrons flux described in Subsection 4.4.2: maximum and minimum flux. In both cases it is assumed a homogeneous field over the front-end electronics plane.*

CBM environment and keep a good upset immunity. This is a valid approximation on account that synthesized registers in the back-end, built with TMR architecture, exhibit better performance than DICE cells [85]. Some of the most important implications that a single SEU might have in the operation of the STS detector are summarized in Table 4.3.

Table 4.3: *Most important effects induced by a single SEU in the operation of the STS-XYTERv2 ASIC.*

Register	**Consequence**	**Affected channels**	**Priority**
CSA current	Change on the ASIC current consumption	64	Medium
Polarity	Change in the polarity for signal readout	128	High
VRef_T	Decrement of the absolute threshold of the ADC, therefore an increment in the absolute noise level	128	High
Global gate	Disable the channels readout from the back-end	128	High
Shaping time	Change on the ADC shaping time	128	Low
Trim value	Corrupted trim value. Change on the discriminator threshold	1	Low

The maximum error rate in the whole STS detector is expected to be approximately 22 SEU every 10 min. If we consider that SEU errors can equally occur in all AFE registers, the most probable error type is expected to affect mostly the trim registers.

$$P_{SEU} = \underbrace{P_{TRIM}}_{98.1\%} + P_{others} \tag{4.7}$$

A corrupted trim value, depending on the affected bit, can represent a dramatic change on the threshold of the discriminator. If it also coincides with the first discriminator of the ADC, this might result in an undesirable increment of the noise for a specific channel; otherwise it just modifies the amplitude response. This effect can be considered of small priority for the full detector operation. Under the studied conditions, it is then expected the occurrence of a high priority error after approximately 30 min. Therefore, this can be considered as a good time to reconfigured the affected ASICs.

4.5 Performance of the STS-XYTERv2 after a lifetime irradiation

The STS front-end electronics, located at the periphery of the detector stations, will be exposed to a lifetime dose of no more than 800 krad. However, the average value among all the ASICs of the first STS station is approximately 500 krad. These values arise from an extensive study using FLUKA simulations, described in subsection 4.4.2 and illustrated in Fig. 4.17a. During the ASIC design and development, much care was taken to ensure a high degree of TID tolerance. To reduce the effect of the rising parasitic currents due to irradiation, the AFE design uses nMOS ELT transistors. The advantages of such architecture have been outlined in Subsection 4.1.1.

This section summarizes the results of different tests carried out to evaluate the effects of high radiation levels on the STS-XYTERv2 ASIC and to investigate the implications for the STS operation. Tests have been performed in two facilities using different approaches. The first one consisted of irradiating the chip in different steps using a gamma irradiation facility in the Variable Energy Cyclotron Centre (VECC), Kolkata, India. After every irradiation period, the performance of the ASIC was checked. This allowed to monitor the operation of the chip as a function of the accumulated dose. The second tests were carried out at the Proteus C-235 facility at the Nuclear Physics Institute in Krakow, Poland. The ASIC response was repeatedly monitored after a TID of 400 krad.

4.5.1 Results from a TID delivered by a gamma irradiation

The STS-XYTERv2 bonded onto a prototype FEB-B was placed inside a self-contained dry-storage ^{60}Co gamma irradiator that could provide high doses in short time while keeping a good uniformity. The chip response was studied as a reference before starting the tests. Typical configuration read-back and noise scan were performed. Doses were delivered in the following steps: 40 krad, 100 krad, 200 krad and 500 krad. After every irradiation period, the same functional tests were carried out.

Exemplary *s-curves* from a typical discriminator channel are displayed in Fig. 4.19. They illustrate how the performance degrades with the received dose. The steepness of the curves determine the noise level in the discriminator. After 340 krad it is also possible to observe multiple spikes along the voltage scan. They are correlated to the damage caused by the high irradiation level.

The noise and ADC gain measurements are shown in Fig. 4.20 for different doses. Every point represents the channels average while the shaded area illustrates the statistical errors. Values are normalized to the reference measurement taken before the tests. In some cases (i.e. 140 krad and 840 krad), measurements were performed several hours after irradiation, favoring the annealing process at room temperature.

The effects of radiation are more visible in the noise fluctuations than in the ADC gain. Bonded channels exhibit larger variations compared to not-bonded ones, as a consequence of the capacitive load at the amplifier input. Even if the performance tests were carried out with a standalone ASIC instead of a real detector module, the results shed light on the expected noise levels after a lifetime irradiation. These values indicate that the system noise can be expected to increase by 40 to 60%.

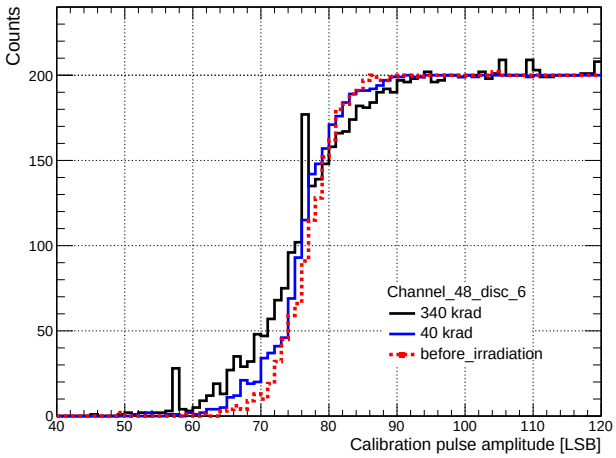
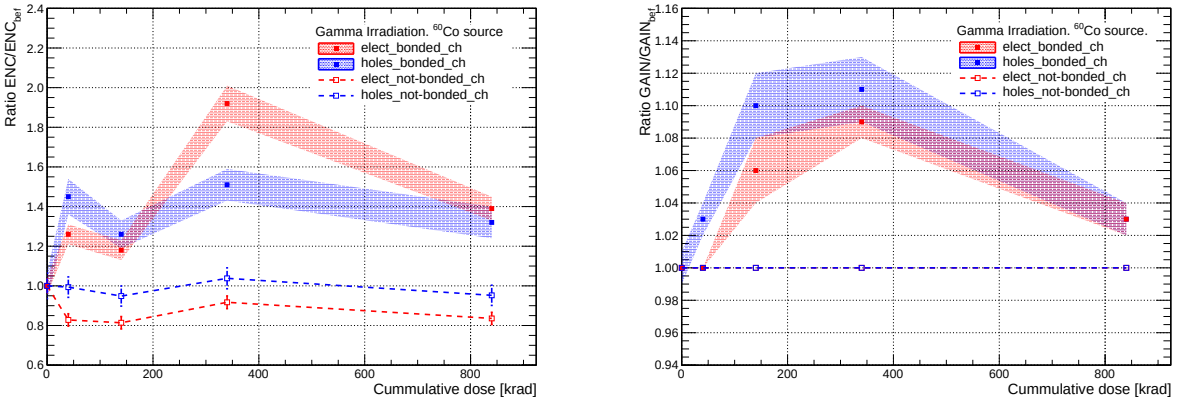


Figure 4.19: *Exemplary s-curves recorded from a discriminator in channel 48. The effect of the irradiation in the discriminator response function was monitored after different irradiation periods.*



(a) *ENC(e-) performance in the STS-XYTERv2.* (b) *ADC gain performance in the STS-XYTERv2.*

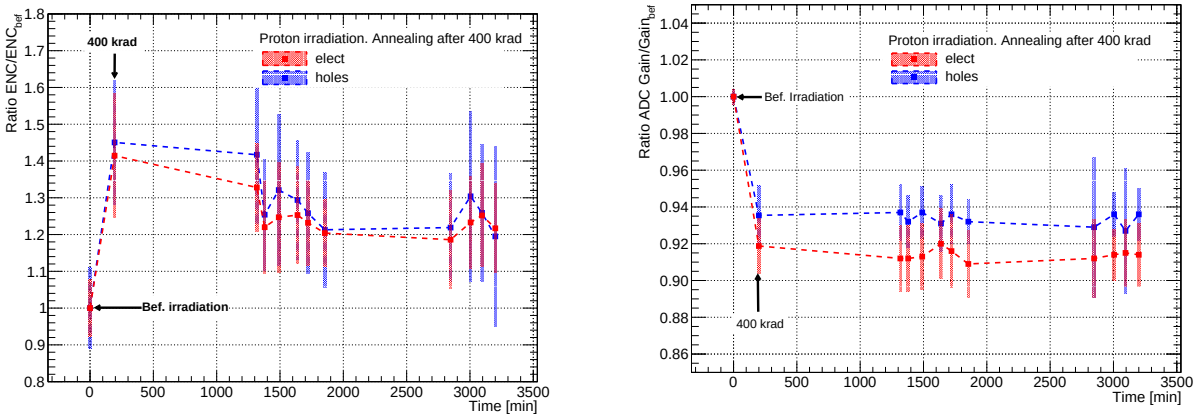
Figure 4.20: *Monitoring of performance parameters in the STS-XYTERv2 for different irradiation doses.*

4.5.2 Effect of annealing process on the ASIC response

The STS-XYTERv2 ASIC was tested in the experimental area of the Proteus C-235 facility. The chip, bonded onto a prototype FEB-B, was exposed to a continuous 50 MeV proton beam delivered by a high intensity cyclotron. The facility allowed to deliver high doses in short times (200 krad/hour). The chip received a cumulative dose of approximately 400 krad. Rather than providing a deep and thorough analysis of the ASIC annealing, this study complements the understanding on how changes the chip response with irradiation and brings insights in the advantages of having short annealing periods.

The ASIC response was sequentially monitored after irradiation in order to check if its performance could be restored by carrying out an annealing process at room temperature. To provide a reference measurement, noise levels and ADC parameters were evaluated before irradiation. Figure 4.21 shows the noise and ADC gain relative to the reference measurement as a function of

the time. Every point represents the average value across all channels, while error bars indicates the standard deviation. Time $t = 0$ depicts the measurement before irradiation. The irradiation effects evidenced immediately as an increment of ∼40% in the ASIC noise and an average reduction of 7% for the ADC gain. Results were consistent in both polarities. The annealing process at room temperature began right after irradiation. The ASIC remained powered and its response was monitored for more than 40 hours at irregular intervals.



(a) *ENC(e-) performance as a function of time.* (b) *ADC gain performance as a function of time.*

Figure 4.21: *The performance of the STS-XYTERv2 ASIC after being exposed to a TID of 400 krad is monitored as a function of time.*

At the end of the monitoring period, the average noise level was approximately 1.2 times larger than the reference, which represents a 20% reduction from the measurement after irradiation. The ADC gain remained constant during this time. Higher temperatures or longer annealing times might also contribute positively to restore the performance of the ASIC. Results evidence that the radiation hard design of the chip is robust and has a reliable tolerance for high irradiation doses, which is a crucial requirement for the operation in the final STS detector.

4.6 Summary

This chapter showed an overview on the STS-XYTERv2 radiation hard design and two different tests carried out in order to evaluate its performance. The effects of SEU have been studied in an irradiation campaign performed with high-intensity proton beams at the Research Center Jülich, Germany. Goals were to characterize upset errors, compare the improvements in the circuit layout and to assess the SEU cross section for two different architectures (DICE cells and *flip-flops*). The number of upset errors registered was 758 and 75057 for DICE cells and *flip-flops*, respectively. These results represent a significant improvement of the SEU immunity in the STS-XYTERv2 compared to its predecessor. The DICE cells cross section has been measured, $(9.26 \pm 0.98) \cdot 10^{-16}$ cm^2/bit, showing a good agreement with literature values. This value allows to estimate the upset rate in the CBM running scenario, resulting in less than one SEU/ASIC/day.

To evaluate the effects of high irradiation doses on the STS-XYTERv2 ASIC two different tests were performed with the help of the VECC Institute, Kolkata, India and the Nuclear Physics Institute in Krakow, Poland. The goals of these campaigns were to monitor the ASIC response as a function of the dose and to study the effect of a short annealing period after high irradiation doses. Two system parameters, ADC gain and overall noise, were systematically evaluated in

every campaign. During the process, these parameters were monitored and compared to reference measurements. It showed that the overall noise increases more significantly than the ADC gain. The noise levels in the ASIC at the end of the experiment lifetime are expected to be approximately 1.4 – 1.6 times larger than the initial values. Moreover, it was demonstrated that a short period of annealing at room temperature has a beneficial influence the noise performance of the chip. In general, results indicates that the radiation hard design of the chip is robust and has a reliable tolerance for high irradiation doses, which is a crucial requirement for the operation in the final STS detector.

Chapter 5

Test of STS prototype modules in a relativistic proton beam

A very important step towards the final design of the STS is the test of the first prototype modules with dedicated readout electronics and the DAQ. These tests allow studying not only the detector response and parameters such as signal amplitude, noise level and time resolution, but also evaluating the performance of the ASIC in the readout of the silicon sensor. In addition, it is also a fundamental platform for developing the DAQ system which is vital for its further extension towards a larger integration stage. Under these goals, two detector modules with components close to their final version, have been assembled and tested. The studies have been conducted with a relativistic proton beam of 1.7 GeV/c momentum at the COSY [129], Research Center Jülich, Germany, in March 2018. Results of this study are presented and discussed in this chapter.

5.1 Experimental setup

The experimental study of prototype STS modules was carried out with a beam of minimum ionizing particles, which provides the best achievable approximation to the real experimental conditions. The tests were performed in a 1.7 GeV/c proton beam extracted from COSY [129] with adjustable intensities between 10^4 - 10^6 particles/s and spill length of approximately 60 s. The main goals were to characterize the latest module prototype and to evaluate the SNR using the STS-XYTERv2 based readout.

The test system comprised two STS tracking stations (labeled T3 and T5) and two reference scintillators (Hodoscopes 1 and 2). Every station hosted a detector module. The schematic representation of the beam line and a photo of the installed setup are shown in Fig. 5.1.

The hodoscope pair monitored the beam position, intensity and also provided spatial information for each crossing particle. Each hodoscope has 64 $\times$ 64 effective pixels, built from 4 layers of scintillating fibers. The diameter of a fibre is 1 mm, which provides a spatial resolution of about 0.3 mm. The hodoscopes were read out using prototype FEB-B carrying one STS-XYTERv2 ASIC. Thy were interfaced to the FEB-B by means of an attenuator board. In order to avoid amplitude saturation, the STS-XYTERv2 was operated in MUCH mode (dynamic range up to 100 fC).

The modules were built using the prototype FEB-B. Each board carried one STS-XYTERv2 chip which allows to read out 128 strips per sensor side. The electronics were attached to a 4.2 $\times$ 6.2 mm^2 silicon sensor via microcables of about 25 cm length. Taking into consideration the strip pitch of 58 μm and the stereo angle of 7.5°, the contact area on the *p-side* was shifted by 2.63 mm horizontally as depicted in Fig. 5.2a. The sensor active area, i.e. where strips on both sides were read out, resulted in approximately 2.18 cm^2. Mechanical supporting elements were produced of acrylonitrile butadiene styrene (ABS) using 3D printing technology, see Fig. 5.2b [138].

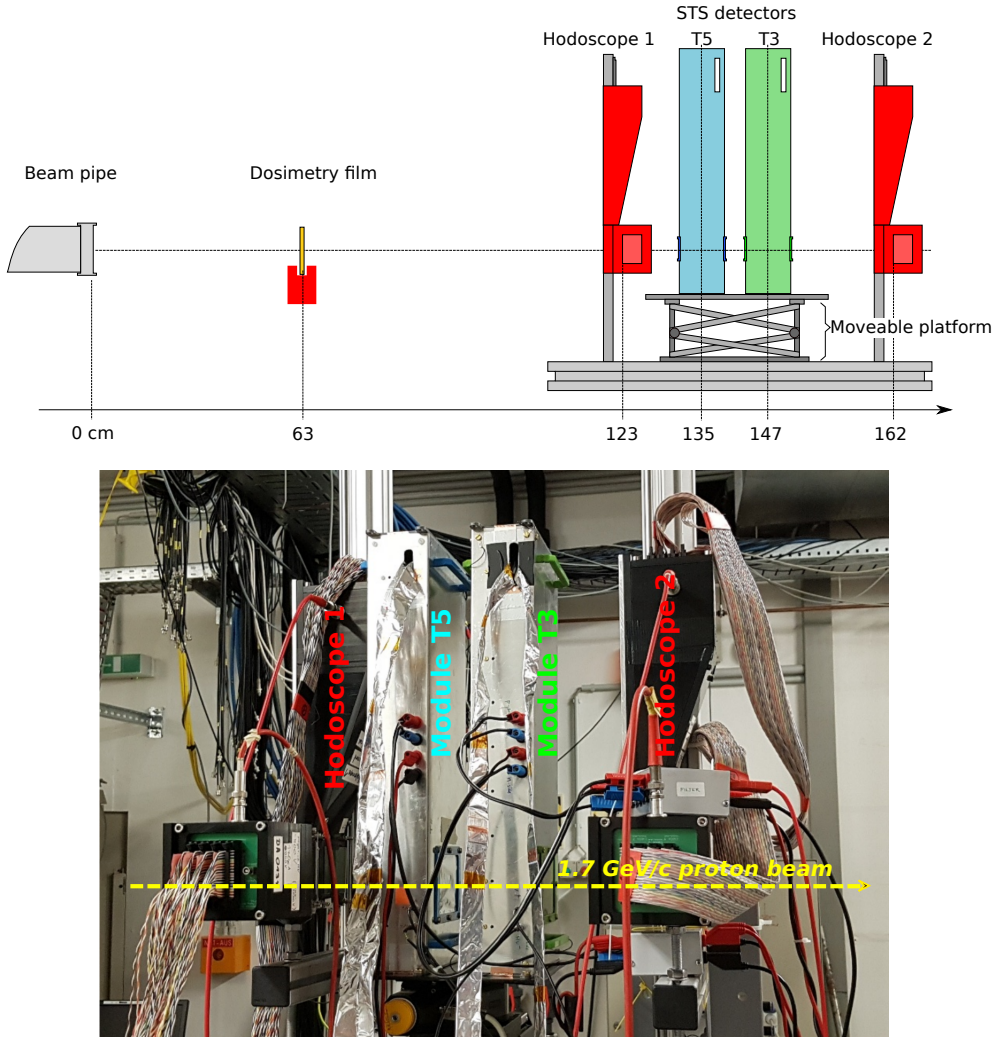
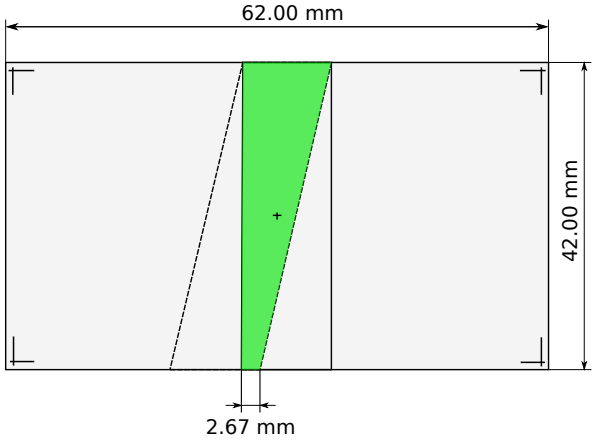


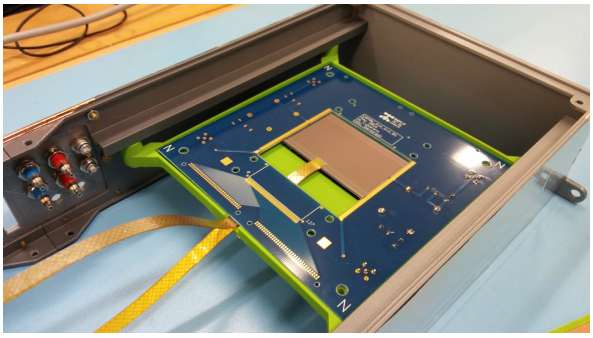
Figure 5.1: *Experimental setup at the beam line extracted from COSY.*

A fully assembled module is shown in Fig. 5.3, where the main components are highlighted. The station served as mechanical support, light-tight enclosure and as an interface for cooling and power distribution. The sensors, microcables and front-end electronics were shielded from electromagnetic interferences using custom-built copper structures.

The detectors under test were placed on a movable platform, which allowed manual vertical adjustment. The platform was also equipped with two step motors, remotely controlled for adjusting the transverse position and the azimuthal angle of the detectors.



(a) *Schematics of the sensor active are.*



(b) *Sensor board of a module.*

Figure 5.2: *Assembly of a prototype module. A single STS-XYTERv2 ASIC is used for the readout of every sensor side, i.e. 128 channels connected through the visible microcables. The active sensor area, resulting from the coincidence between both sides, is approximately 2.18 cm^2.*

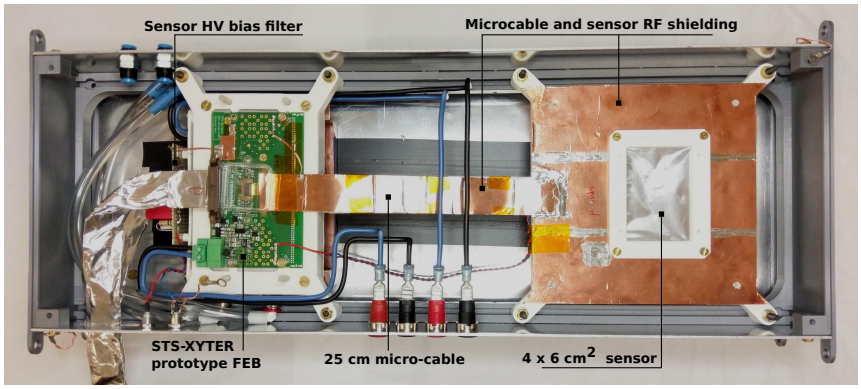


Figure 5.3: *Detector module placed inside the custom-built station.*

5.1.1 Filtering and ground scheme

Before system operation, it was mandatory to establish a ground and filtering scheme for the detectors. The adopted biasing scheme is known as floating bias, in which the ground of the front-end electronics are connected to the respective sensor side. The shielding of sensors and microcables are also kept at the biasing potential of each side.

Figure 5.4 illustrates the powering and filtering scheme used during the tests. In the sensor high voltage biasing chain, two stages low pass RCL[1] filters were used to reduce the high frequency component of the noise. The filters were built symmetrically for mitigating common and differential mode. The so-called "on-board filter" refers to the high frequency filter placed on the sensor board. The low voltage line for powering the ASICs was also connected via an external LCL filter. The filter was optimized to suppress the common-mode in the front-end electronics power supply. For operating both sensor sides, a cross-capacitor of value 1 nF is connected across the terminal of the low voltage filter. However, the fluctuations in the ground line of one FEB was immediately sensed by the other side.

[1]RCL: Passive filter using resistive, capacitive and inductive components.

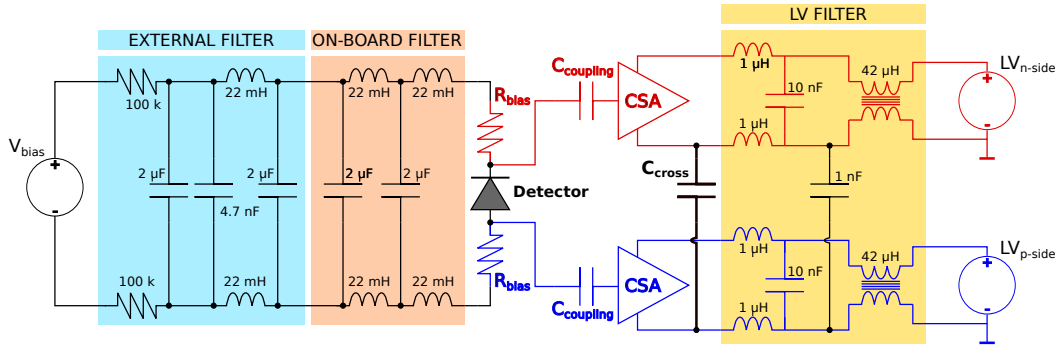


Figure 5.4: *Powering scheme used during module tests at COSY. The scheme includes the different filtering stages for low and high voltage.*

An important step in the noise mitigation was to identify that FEBs references should be connected via a cross-capacitor as close as possible. This is marked in the Fig 5.4 as C_{cross}. The capacitance value was chosen based on the impact on the overall system noise. Figure 5.5 presents the result of the study carried out with module T3 in the laboratory. This result showed that noise can only be considerable reduced with a capacitor larger than 100 nF. The dimensions of such capacitor may pose a challenge in the final system due to free-space constraints. However, this was not an issue during the tests in the accelerator line, therefore a 2.2 μF capacitor was used.

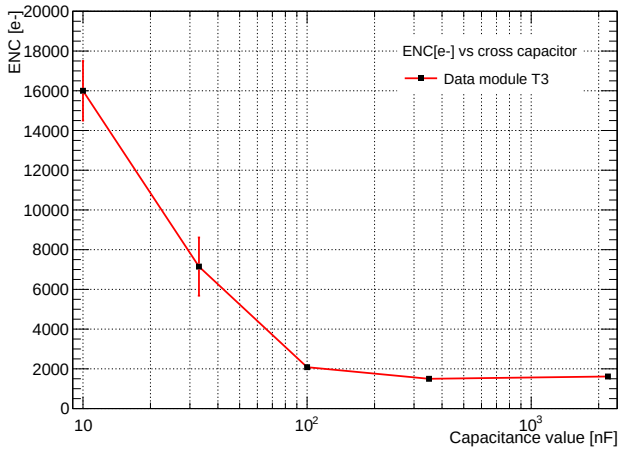


Figure 5.5: *FEB reference potentials have to be connected with a capacitor placed as close as possible. The value of the capacitor significantly reduces the overall noise.*

5.1.2 Readout chain for the STS test modules

The block diagram of the readout chain, conceived for reading out the modules, is shown in Fig. 5.6. Front-end electronics from detectors under test and the hodoscopes reference system were connected to a single AFCK board acting as DPB. The DPB implemented the latest available version of the STS-XYTERv2 firmware, which allowed to interface up to 6 ASICs simultaneously. This layer was also responsible for interfacing the slow and fast control, data preprocessing and time sorting.

In order to synchronize the time stamp information in the front-end electronics, a time synchronization system (TSS) was implemented in another AFCK board. The data were continuously read out and fed to a FLES processing computer, where all hit information for a given time interval was merged.

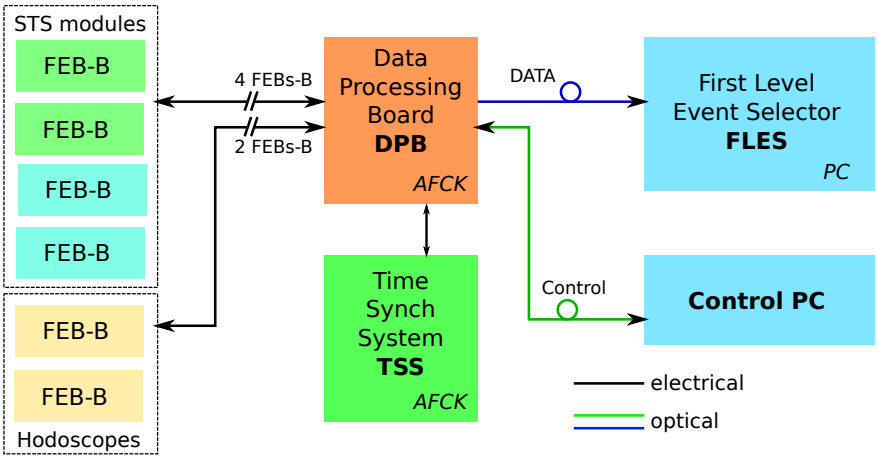


Figure 5.6: *Scheme of the DAQ employed during the beam tests at COSY for reading out first STS prototype modules.*

5.1.3 Results from module calibration

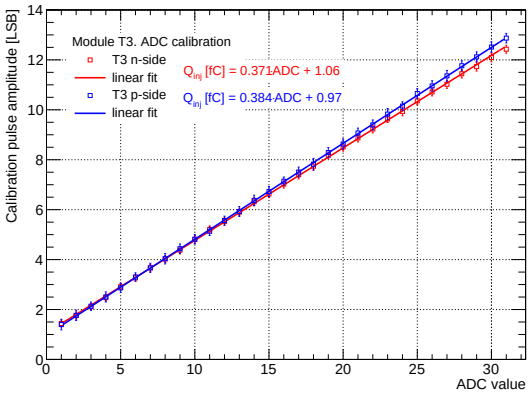
Before the module assembly, every component undergoes a quality assurance process. The STS-XYTERv2 ASICs were calibrated in both polarities before TAB-bonding microcables and sensor. The calibration was done using the internal pulse generator for an ADC range of approximately 10.4 fC, determining a resolution of 0.34 fC/LSB.

An important step before the operation of the modules in the beam line was to check their performance in the laboratory. This allowed to detect operating issues and also broken or unconnected channels. After the assembly of all components, the system capacitance changed. The effect of a larger capacitance at the amplifier's input influences not only the system noise but also the measured charge. The collected charge in the detector is now distributed between the total module capacitance C_d and the dynamic input capacitance of the amplifier C_{CSA}.

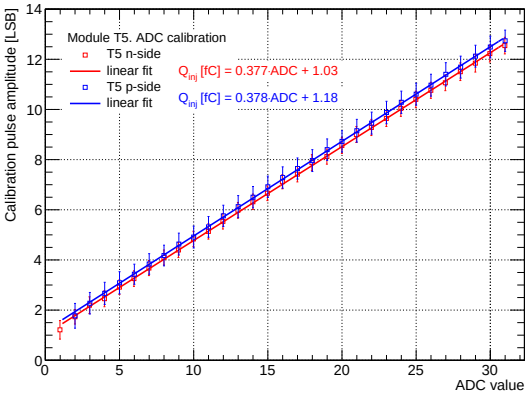
To measure the parameters of the charge calibration in every channel, a *s-curve* scan was performed. ADC reference potentials were set to $VRef\_P,N,T$ = (53, 26, 55) LSB. Pulses with amplitude between 0 – 14 fC were injected on every channel and the discriminator's output was recorded using dedicated counters. The value at which each *s-curve* reaches the 50% defines the effective threshold of the discriminator. The procedure is detailed in Chapter 3, subsection 3.7.2. Figure 5.7 shows the ADC response function for a typical channel, where values are read out from each detector side. Error bars correspond to the noise level in every discriminator.

The measured data is fitted with a first order polynomial to extract the parameters of the calibration. The slope of every fitting curve represents the ADC gain, while the intercept shows the ADC offset. The distributions of the ADC parameters for all channels in every chip are shown in Fig. 5.8 and Fig. 5.9.

In module T3, a small difference between the ADC gain for electrons and holes polarity can be observed. This discrepancy (0.013 fC) represents only 3.5 % of the average gain for electrons. Since both ASICs were calibrated in the same way and previously checked, this discrepancy is not well understood. Results show a good agreement between *n-side* and *p-side* of module T5.

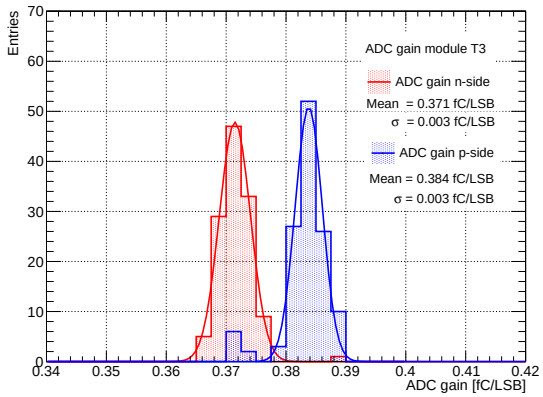


(a) *T3: ADC response function.*

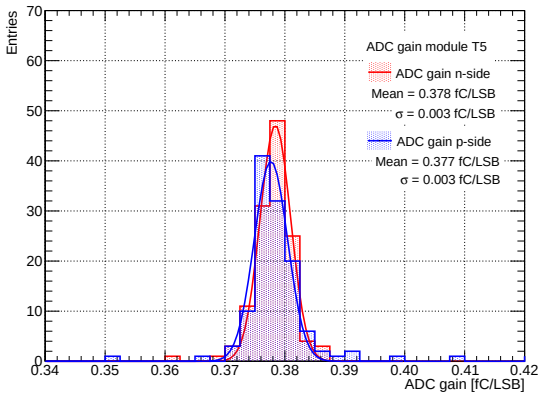


(b) *T5: ADC response function.*

Figure 5.7: *ADC response function for a random-selected channel. Error bars represents the noise level on each discriminator.*

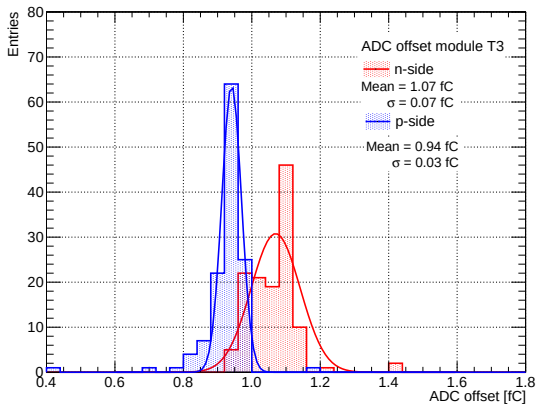


(a) *T3: ADC gain distribution.*

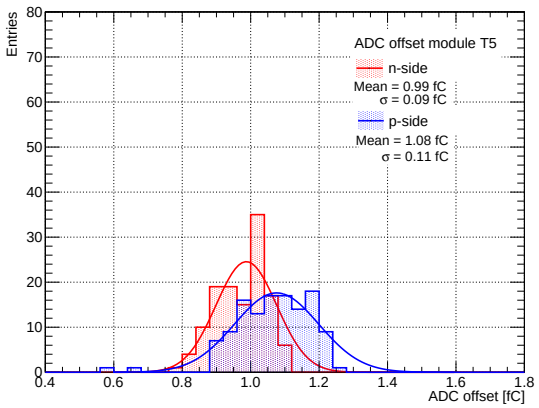


(b) *T5: ADC gain distribution.*

Figure 5.8: *Distribution of the ADC gain for all channels.*



(a) *T3: ADC threshold distribution.*



(b) *T5: ADC threshold distribution.*

Figure 5.9: *Measured ADC threshold offset during in-beam test.*

However, the average gain on each module has been shifted by approximately 10% with respect to the calibration value (0.34 fC/LSB) as a consequence of the detector load capacitance. This represented an important correction in order to properly understand the data.

To reduce the overall noise levels in the detectors, signals were shaped using the largest possible peaking time of the ASIC. This value is encoded into the slow shaper of every channel and corresponds to approximately $\tau_3 = 332$ ns, see Chapter 3, subsection 3.9.5. Changing the time constant does not only change the noise bandwidth, but also the signal amplitude [59]. Since the calibration curves described above were acquired using the shortest peaking time (approximately $\tau_0 = 90$ ns), gain and offset corrections are also required in both cases.

Corrections were done offline after finalizing the beam campaign. The ASIC response function was evaluated at the respective peaking times. The ratio between values at largest $\tau_3 = 332$ ns to shortest $\tau_0 = 90$ ns times were calculated and applied as correction factors ($\gamma_X = X_{\tau_3}/X_{\tau_0}$). The systematic uncertainties were considered by measuring the spread among all ASIC channels.

To read out the *p-side* of module T5, the baseline register was adjusted to the value $VRef\_T = 56$, resulting in an offset 0.6 fC larger than the corresponding *n-side*. This has no consequences on the measured gain but on the ADC offset. For a further analysis of the experimental data, the corresponding ADC transfer functions are used, see Table 5.1.

Table 5.1: *ADC transfer functions for modules T3 and T5 after shaping time correction.*

	n-side	*p-side*
Module T3	$A_-[LSB] = 1.89 \cdot Q - 2.64$	$A_+[LSB] = 1.89 \cdot Q - 2.66$
	$Q_-[fC] = 0.53 \cdot A + 1.40$	$Q_+[fC] = 0.53 \cdot A + 0.41$
Module T5	$A_-[LSB] = 1.67 \cdot Q - 2.06$	$A_+[LSB] = 2.0 \cdot Q - 4.08$
	$Q_-[fC] = 0.60 \cdot A + 1.24$	$Q_+[fC] = 0.50 \cdot A + 2.04$

The systematic uncertainties of the measured charge, which originate from the calibration parameters, are estimated according to Eq. 5.1 and Eq. 5.2.

Module T3:

$$\begin{aligned} \Delta Q_-[fC] &= 0.015 \cdot A + 0.19 \\ \Delta Q_+[fC] &= 0.016 \cdot A + 0.12 \end{aligned} \tag{5.1}$$

Module T5:

$$\begin{aligned} \Delta Q_-[fC] &= 0.012 \cdot A + 0.16 \\ \Delta Q_+[fC] &= 0.011 \cdot A + 0.23 \end{aligned} \tag{5.2}$$

5.2 Identification of a logic error in the STS-XYTERv2

The module read out in beam with the STS-XYTERv2 ASIC revealed a critical error in the logic of the chip. The error is triggered when many channels are fired within a narrow time window. In the particular case when only one out of the five available data links is used, the problem appears when at least seven channels are in coincidence. This implies that either extra hits are seen at the output of some channels (hit copies) or hits are never seen in some channels (hit losses). This is of utmost importance, since losing hits can lead to missed events and/or distorted measurements. After a careful revision, the error was confirmed by the ASIC developers and fixed in the next revision of the chip.

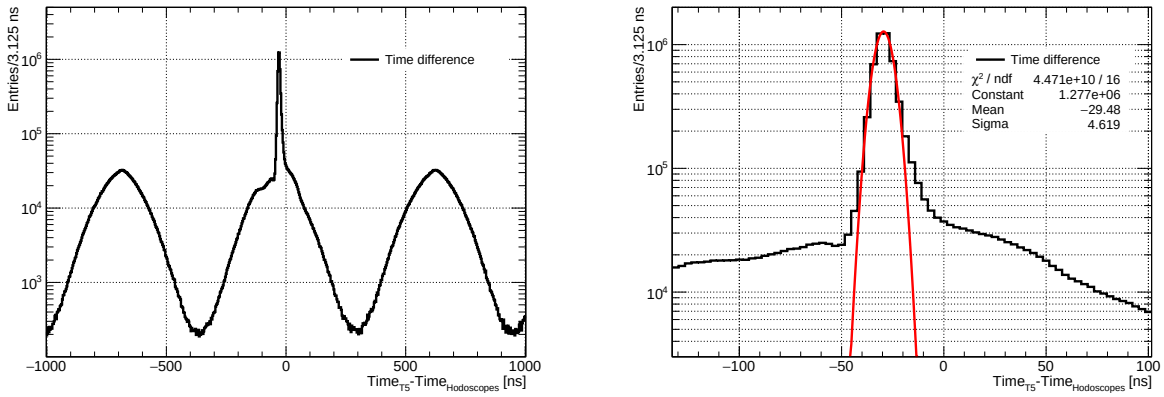
The characterization of the logic error leads to a thorough test of the ASIC back-end. First goal was to find the exact coincidence conditions under which hit losses were possible. For this purpose, a dedicated setup was built, using an external arbitrary waveform generator and a prototype FEB-B connected to the current readout chain described in subsection 5.1.2. The waveform generator was operated at a fixed frequency using two output channels connected to two groups of six channels each. The delay between the output signals in the pulser was scanned in a range of ± 1000 ns [139].

The delay window in which hit losses or copies occurred was calculated based on the collected data and the time delay. Once the limits for the coincidence window were extracted, they were applied to the stored data of the beam campaign. This allowed to select realistic events and to filter considerably the data volume.

The effects of this logic error were visible in the rate and quality of the collected data. In each run, the conditions to tag the hit multiplication and losses might differ, based on the beam intensity, noise levels and the duration for which the problem was present.

5.3 Time correlations with the hodoscope reference signal

The full system was operational and run in self-triggered mode during all data taking process. As a first step, the time correlation between the hits in the STS modules and the signals from the reference hodoscopes (H1-H2) was checked. The time correlation between both systems is shown in Fig. 5.10a. The correlation peak can be seen at 30 ns in this example. It corresponds to the time difference between hodoscopes and module T5. Together with the main peak, a series of minor peaks can be seen. These are consequence of the combinatorial background, modulated by the time structure of the beam.



(a) *Time correlation between hodoscopes and T5.* (b) *Zoom in the time correlation peak.*

Figure 5.10: *Time difference with respect to the hodoscope signals for module T5. a) All the hits. b) Zoom in the peak area. The distribution is shown before time-walk correction.*

The time correlation analysis allows to observe potential malfunction of the synchronization system and it also gives a direct access to the intrinsic time resolution of the detectors. To study the correlation, the time difference between sensor hits and scintillators signals within the same time micro-slice is calculated. The distribution is shown in Fig. 5.10b before applying time-walk amplitude corrections. The peak has been fitted using a Gaussian function in order to estimate the system time resolution. The result, $\sigma_T = 4.62$ ns, is the sum of module and hodoscopes contributions, as shown in Eq. 5.3:

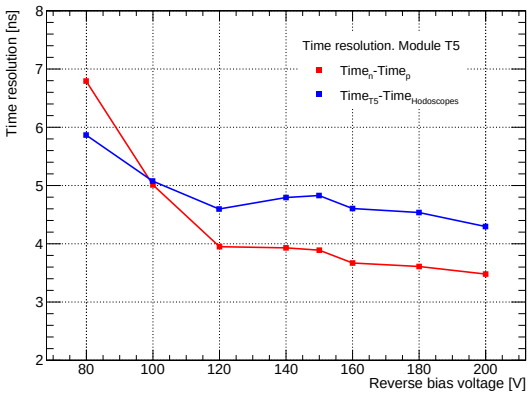
$$\sigma_T^2 = \sigma_{T5}^2 + \sigma_{H1-H2}^2 \tag{5.3}$$

where every element can be decomposed in the intrinsic detector and readout electronics resolution, see Eq. 5.4. The same relationship applies for the reference system:

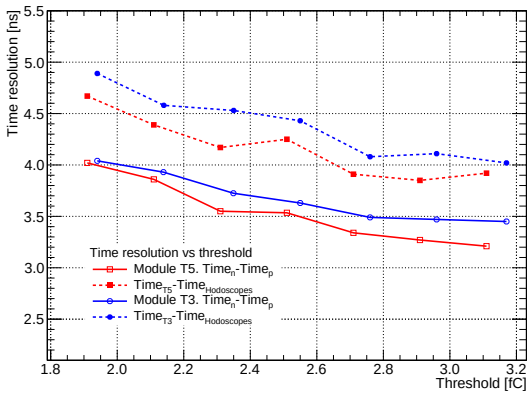
$$\sigma_{T5}^2 = \sigma_{Si-sensor}^2 + \sigma_{STS-XYTERv2}^2 \tag{5.4}$$

Assuming that the overall time resolution in every system is mainly dominated by the contribution of the STS-XYTERv2 ASIC, it is possible to estimate an upper limit for the chip as $\sigma_{STS-XYTERv2} = \sigma_T/\sqrt{2} = 3.26$ ns.

The time resolution of the STS-XYTERv2 ASIC has also been studied in different system tests. Results from a bias voltage scan performed with module T5 are presented in Fig. 5.11a. The plot shows the time resolution determined by two methods. The first one, described above and shown in blue, includes the comparison with the reference signal of the hodoscopes. The second method compares the measured time for each event in *n-side* and *p-side*. Results show the improvement of the overall time resolution with the sensor bias. For a fully depleted sensor not only the amount of collected charge is larger, but the signal generation is faster, since the velocity of the charge carriers depends on the strength of the electric filed. Moreover, the overall system noise decreases, which improves the signal detection and reduces the long tails in the time difference spectra.



(a) *Time resolution as a function of the bias potential.*



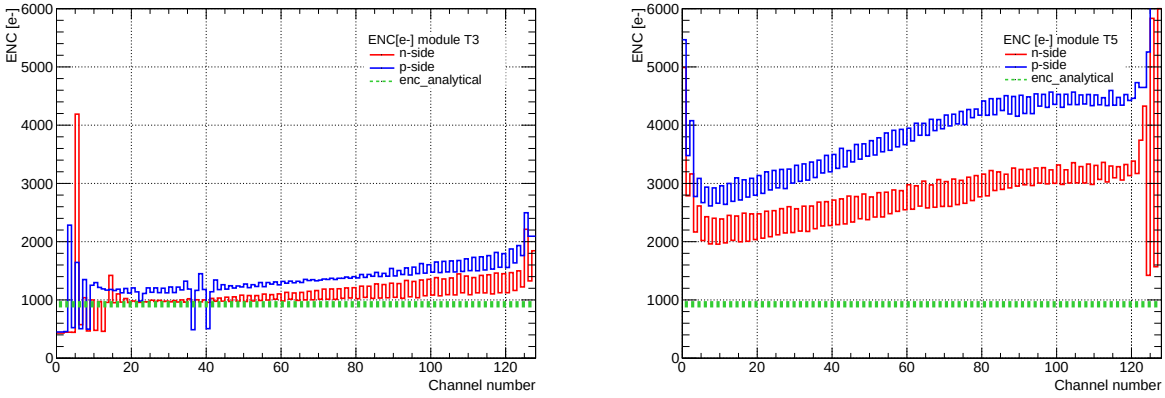
(b) *Time resolution as a function of the signal threshold.*

Figure 5.11: *System time resolution. a) Time resolution estimated with module T5 at different biasing potentials. b) Time resolution in modules as a function of the signal threshold.*

Figure 5.11b illustrates the time resolution as a function of the threshold for both modules. Only signals with larger amplitudes and therefore faster rise times are digitized at higher thresholds. The time jitter also decreases, since it is related to the system noise and the slope of the signal's rising edge, as described in Chapter 3, section 3.8. The data show an improvement of the time resolution in approximately 1 ns for a change in the threshold of 1.2 fC. Results are not only consistent in both modules, but also in agreement with the ASIC time-walk, described in Fig. 3.30b. The measured time resolution is also considered very good for the STS-XYTERv2 ASIC.

5.4 System noise estimation

Low noise levels are essential for working with self-triggered systems. As the modules and the full readout chain are operated without a trigger signal, it is necessary to pay special attention to the overall noise. This also includes mitigating all possible sources of electromagnetic interferences and their effect in the detectors with proper shielding and grounding. After multiple trials, a method to read out simultaneously both detector sides was established. This was achieved by placing a capacitor between the FEBs reference grounds, as shown in subsection 5.1.1. For some specific runs, the thresholds were kept high since the noise levels in conjunction with the generation of duplicated hits could overflow the data acquisition system.



(a) *Module T3.* (b) *Module T5.*

Figure 5.12: *ENC(e-) for modules T3 and T5 with sensor biased at 160 V.*

To estimate the system noise levels a *s-curve* scan was done. The acquired *s-curves* represent the discriminator response; their standard deviation is an effective measurement of the overall noise. Noise measurements are acquired with a fully biased sensor. Results are shown in Fig. 5.12 for all channels of each module.

Even if both detectors were assembled identically, a significant difference can be seen among their noise performance. This discrepancy is considered to be associated with two main factors. The first one is related to parasitic capacitances that might appear during the construction of T5. The second one could be consequence of an insufficient or improper grounding point. Another important observation is concerning the odd-even pattern among the channels, which is more pronounced in module T5. This effect has been identified as an undesirable issue of the STS-XYTERv2 and is explained in Chapter 3, subsection 3.9.2.

A realistic estimation of the system noise can be obtained based on the total detector capacitance. Its contribution is related to the series voltage noise and $1/f$ noise as described in Chapter 3, subsection 3.9.1. It was demonstrated that the overall system noise has a linear dependence with the input load capacitance following the law:

$$ENC\ [e^-] = \alpha \cdot C_T + ENC_{ASIC} \tag{5.5}$$

where C_T represents the total channel capacitance, α is a proportional coefficient that relates the noise performance in the chip with the input capacitance. The α value has been determined for the STS-XYTERv2 ASIC as 27.3 ENC(e^-)/pF, see Chapter 3, subsection 3.9.4. The ENC_{ASIC} term is the intrinsic contribution from the chip itself. For a fully bonded ASIC into a prototype

FEB-B, this value results in approximately 600 ENC(e^-). However, it includes the contribution of the input connectors and their traces in the PCB. A more accurate value is calculated in Chapter 6, subsection 6.4 for a single ASIC without input bonds, resulting in approximately 494 ± 46 ENC(e^-).

The total capacitance of the module is estimated according to the dimensions of their components, see Eq. 5.6. The two main contributions are the aluminum strips in the sensor and the microcable traces, see Eq. 5.6. The prototype sensors used in the module construction are developed by CiS Forschungsinstitut für Mikrosensorik GmbH. In CiS silicon sensors, the equivalent strip capacitance differs between *n-side* and *p-side* (1.52 pF/cm and 1.74 pF/cm) [140]. The total microcable capacitance is 0.38 ± 0.02 pF/cm [106].

$$C_T = \underbrace{l_{Al} \cdot C_{Al}}_{\sim 40\%} + \underbrace{l_{cable} \cdot C_{cable}}_{\sim 60\%} \tag{5.6}$$

The estimated noise values are 929 ± 46 ENC(e^-) for *n-side* and 956 ± 46 ENC(e^-) for *p-side*. Their relative difference is contained within the error bars, so their average is assumed as a representative value. This result is represented in Fig. 5.12 with a shaded green line. The error bars are contained within the width of the line. It can be seen that module T5 shows the large discrepancy with the calculated values.

The average noise levels for every module side are summarized in Table 5.2. The error represents the standard deviation among all channels excluding unconnected and highly noisy ones at the edges of the active area.

Table 5.2: *Overall detector noise measured at 160 V.*

	ENC(e^-)	
Module/Polarity	*n-side*	*p-side*
Module T3	1101 ± 146	1365 ± 190
Module T5	2750 ± 413	3717 ± 577

The overall noise in the modules ENC(e^-) is also studied as a function of the reverse bias voltage applied to the sensor. Results are shown in Fig. 5.13. The error bars correspond to the standard deviation among all the channels. While the noise remains approximately constant for the *p-side*, the effect of the bias voltage is clearly visible for the *n-side*. This allowed to confirm the proper operational voltage for the system to be above 120 V, where the noise contribution stabilizes.

Unconnected channels are recognized by a significant reduction in the noise level compared to connected ones. For module T3, this level is about 500 ENC(e^-), which indicates that the channels might be disconnected at the ASIC bond. On module T5, 3 channels are in total disconnected. However, it is difficult to judge where the bonds are exactly broken due to the high and uneven levels of noise. This can be also an indication that noise is introduced via the system common ground or induced by a large cross-talk among channels. Since the module T3 and other ASIC tests have not shown a large electronic cross-talk effect, this hypothesis is rejected.

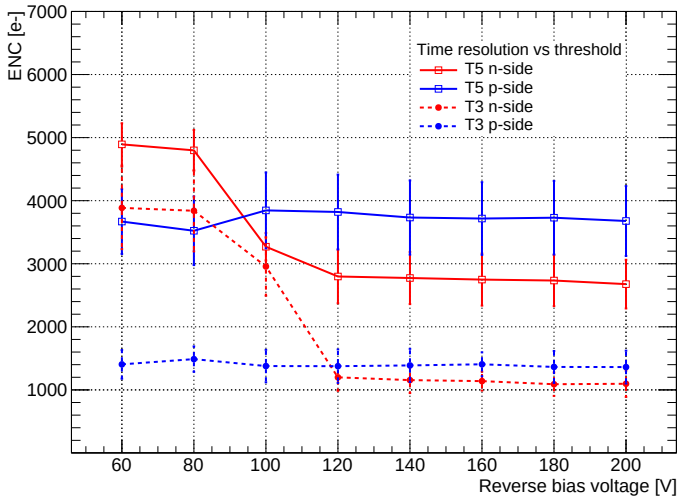
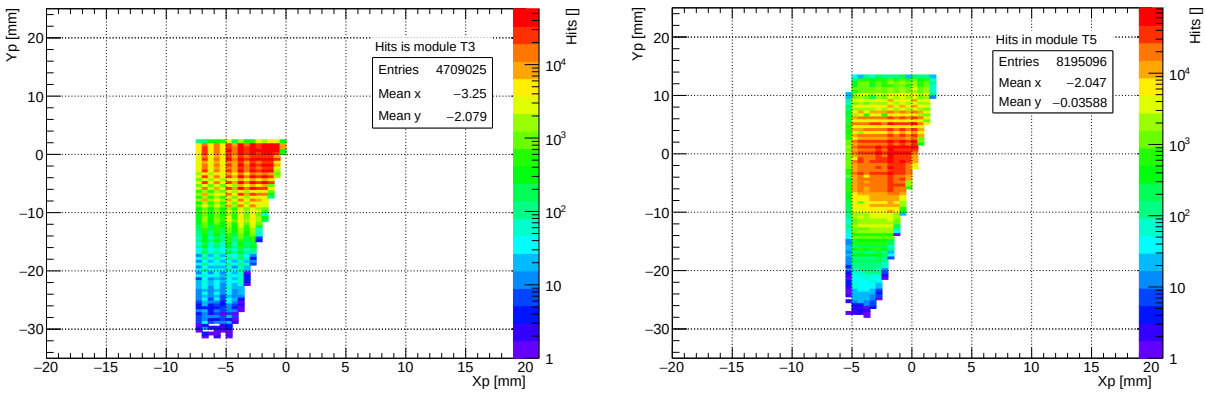


Figure 5.13: *Overall noise levels measured for modules T3 and T5 as a function of the sensor reverse bias.*

5.5 Hit maps

The hit density maps for modules T3 and T5 are shown in Fig. 5.14. To simplify the representation of the data, several selection criteria were applied. At first the temporal coincidence between each module and the two hodoscopes is required. A geometrical constraint is also applied, requesting that the hit is located within the area formed by the sensitive surface of the sensor, see Fig. 5.2a.

The displayed structure results from the readout overlap of *p* and *n-side* strips on each sensor. Noisy and unconnected channels have been removed. The active area can be estimated in the range between 1.85 and 2.00 cm^2 for both modules. The beam profile is clearly visible on the histograms. The beam intensity was monitored between 10^4 to 10^6 protons/s for different runs. For these event rates, no hit overlap is expected and the ASIC AFE should be capable to handle such rate.



(a) *Module T3.* (b) *Module T5.*

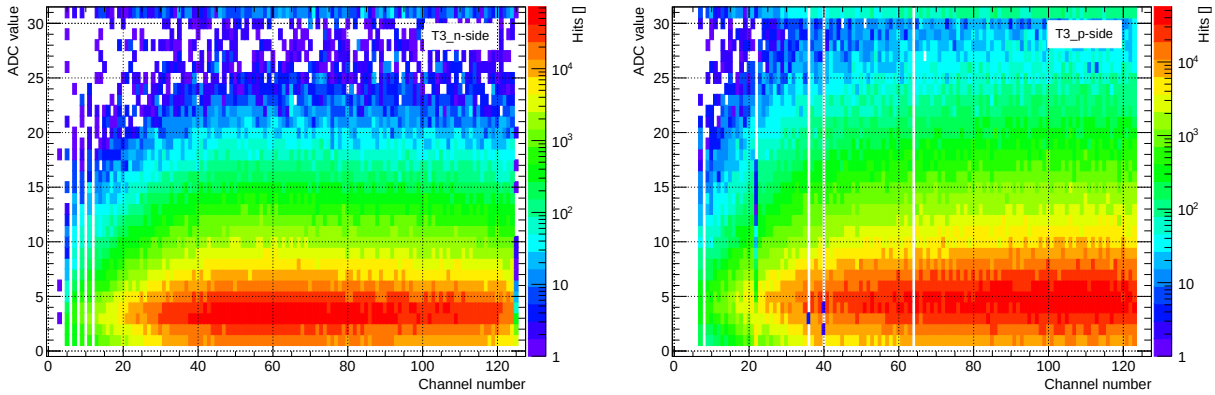
Figure 5.14: *Hit density maps of the modules T3 and T5 after timing and geometrical cuts. The shape indicates the readout-overlap between n-side and p-side.*

A large fraction of hits shows a duplicated pattern, where the main indications resulted from an identical timestamp and ADC information. As explained in Section 5.2, this is a consequence of the logic error identified in the ASIC back-end. The presented data have been already filtered and duplicated hits removed.

5.6 Signal readout

The total signal amplitude is one of the most important characteristics of a detector. For a proton beam with momentum 1.7 GeV/c, the mean deposited energy is approximately 1.08 times larger than MIPs. Consequently, the generated charge in a non-irradiated 300 μm silicon sensor is approximately 24 ke$^-$.

The histograms in Fig. 5.15 show the raw ADC distribution of the signal in the module T3. In this example, the data have been filtered to reduce the effect of duplicated hits and noisy channels. After this stage, the hits produced by the same particle are combined into clusters and the amplitude within each cluster is summed up. The raw ADC signal, cluster amplitude and cluster size for module T5 are illustrated in Appendix E.



(a) *Raw ADC distribution for n-side.* (b) *Raw ADC distribution for p-side.*

Figure 5.15: *Module T3: Raw ADC distributions.*

A simple clustering algorithm implements timing and geometrical cuts to select proper events. The selection criteria also includes the necessary coincidence with the hodoscope system and between the signal on the *n* or *p-side*. This contributes to clean the data by rejecting hits caused by the electronic noise. In a self-triggered system, the digitization threshold plays a key role. If the threshold is kept too high, the signal remains undetected; however, if the level is too low, noise-related hits would overflow the channels and create dead time. Moreover, in a silicon sensor, a fraction of the collected charge always couples to the neighboring strips. This implies that the full signal amplitude can be only reconstructed if the threshold is sufficiently low.

The cluster amplitude spectra from module T3 are shown in Fig. 5.16 after applying the criteria described above. The reconstruction yields mostly 1 strip-cluster. Two and three strip-clusters are one to two orders of magnitude lower as observed in the distributions of the cluster size, see Fig. 5.17. The absolute thresholds in the modules are kept relatively high to avoid a saturation of the data acquisition system due to noise and duplicated hits. This results in a suppression of the 2 and 3-srips clusters, because the signal on the minor of the strips, appears repeatedly below the threshold.

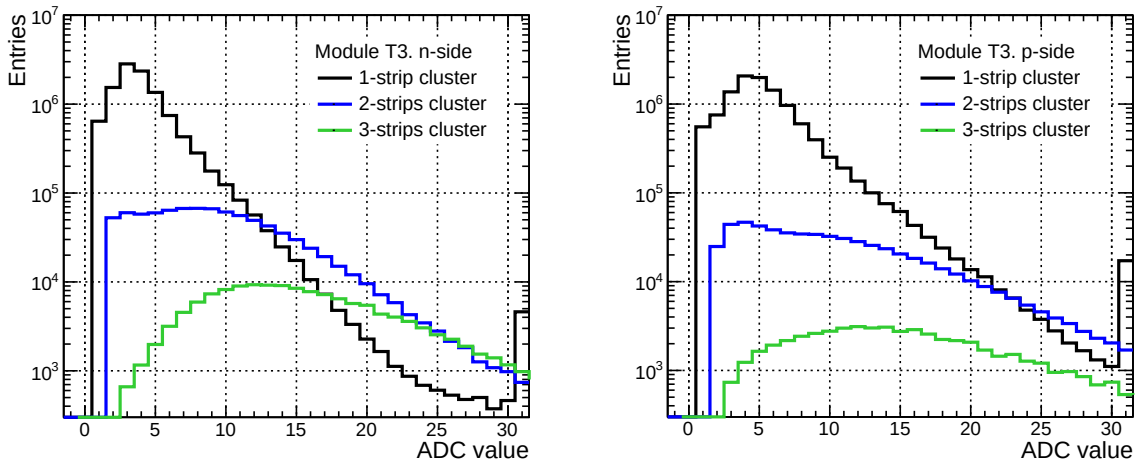


Figure 5.16: *Spectra of the total cluster amplitude, taken from module T3 at V_{bias} = 160 V.*

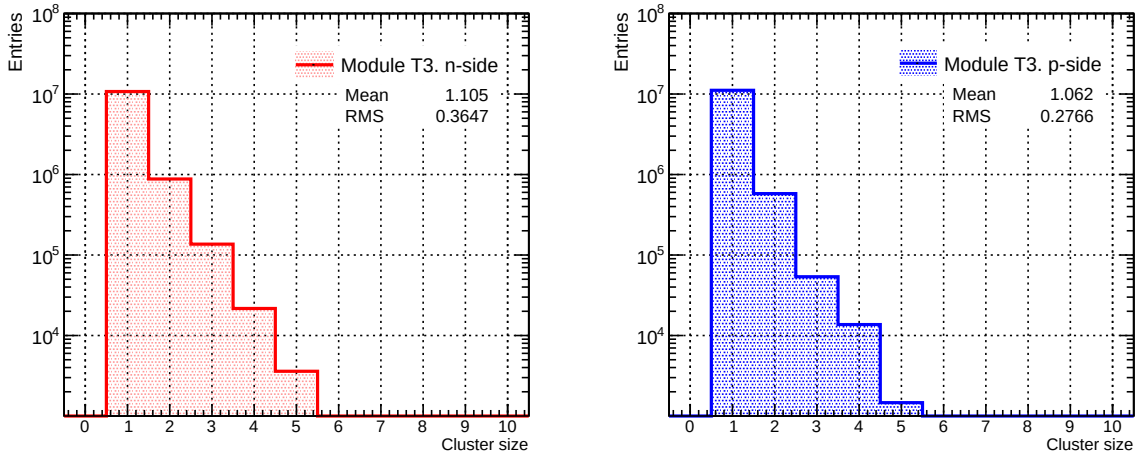


Figure 5.17: *Cluster size distribution for protons inciding perpendicular to the sensor area of module T3.*

In the simplest approach, a signal amplitude spectrum of a silicon sensor can be approximated with a Landau-Gaussian convolution [141]. Exemplary spectra from 1-strip clusters are shown in Fig. 5.18. They represent amplitude distributions acquired with the module T3 at an operating voltage of 160 V. The spectra are fitted with a Landau-Gaussian function using $Q_{min} = 3\sigma_{noise}$ as selection criteria. The most probable value (MPV) is interpreted as the collected charge.

The error estimation considers the statistical and the systematic uncertainties summed quadratically. The systematic error is evaluated considering the amplitude dispersion of the threshold and the gain in all channels of the chip. Spectra from module T5 are shown in Appendix E.

To analyze the signal from 2 strip-clusters, it is primarily necessary to understand the shape of spectra. Figure 5.19 illustrates the measured charge spectra in module T3 at different thresholds. It can be noticed that a large number of low amplitude counts is present at lower threshold ($VRef\_T = 183$). This effect is more pronounced for *p-side* of both detectors, where the noise levels are higher. The mixed spectra can be decomposed into a low amplitude component, mainly from the electronic noise, and a Landau-Gaussian distribution at higher amplitudes. The left edge of 2 strip-clusters have been cut by the threshold. At larger threshold values, the noise contribution de-

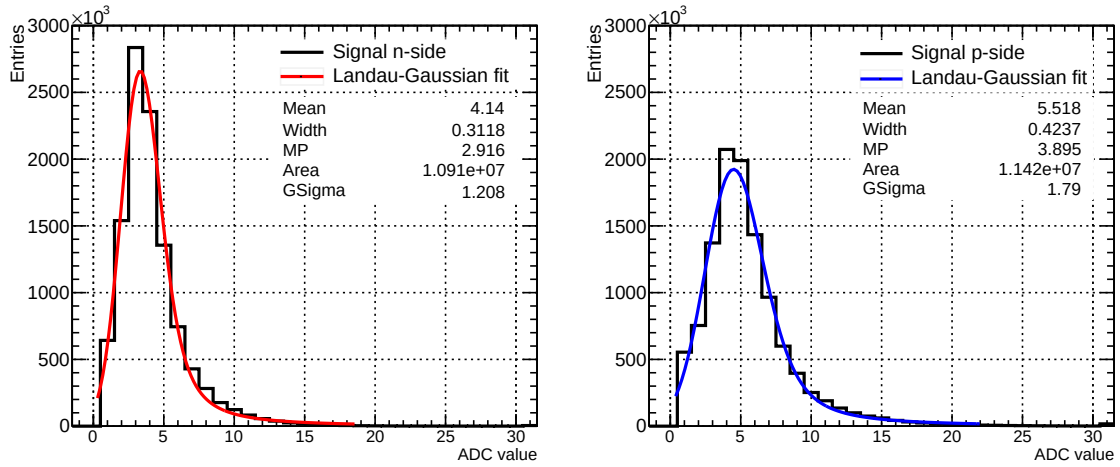


Figure 5.18: *Spectra of 1 strip-cluster amplitude from module T3.* ***Left:*** *n-side.* ***Right:*** *p-side.*

creases and part of spectrum shape is restored. In these cases it is not clear, whether the maximum on the spectrum corresponds to the maximum of the Landau peak.

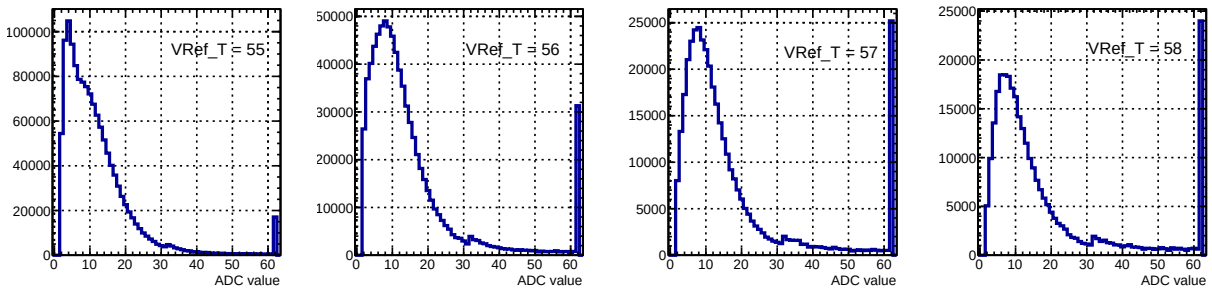


Figure 5.19: *Spectra of 2 strips-clusters measured at different thresholds with module T3.*

Multiple runs at the same bias voltage are performed and analyzed in order to check whether the results are reproducible in both detectors. The data are taken without making any modifications to the setup. Results are summarized in Fig. 5.20 for 1 strip-clusters. The variations in the signal amplitude across the different runs are relatively small and contained within the margins of the error bars. The collected charge for *p-side* (blue circles) coincides in both detectors. This result is consistent for all runs. The average signal amplitude for *n-side* in module T3 is approximately 18.5 ke$^-$. This represents a 14% difference relative to the amplitude measured by the *p-side*.

The expected signal amplitude for 1-strip cluster signals is marked in Fig. 5.20 with a magenta line. This value is calculated according to a simple, but realistic detector model explained in more details in reference [142]. The principle behind it can be explained as the following. In a microstrip detector, when a particle hits the active volume, not all the released charge is injected into the readout electronics. This is caused by effects such as: charge collection inefficiency, charge sharing among the strips, charge division between the sensor and the CSA and ballistic deficit. The ratio of the charge integrated in the front-end electronics to the collected charge in the sensor can be analytically estimated considering mainly the capacitance scheme of a silicon sensor. The time structure of the signal is completely ignored in this approximation and no ballistic deficit is

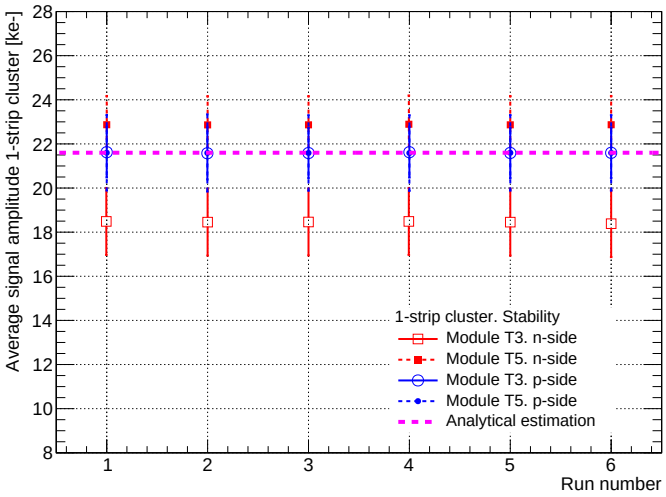


Figure 5.20: *Signal amplitude for 1 strip-clusters measured in both detectors for multiple runs.*

considered since the peaking time of the STS-XYTERv2 is larger than 90 ns [85]. The measured signal amplitude Q_{meas} in the ASIC is related to the collected signal in the implants Q_0 according to Eq. 5.7 for 1 strip-cluster signals.

$$\left(\frac{Q_{meas}}{Q_0}\right)_1 = \frac{C_c}{C_c + C_{p-p_{Total}} + C_b} \cdot \frac{C_{CSA}}{C_{CSA} + C_{cable} + C_{imp_{Total}} + C_b} \tag{5.7}$$

where C_C represents the coupling capacitance, C_b the implant to bulk capacitance, $C_{imp_{Total}}$ is the total implant-strip capacitance including the effect of the neighboring strips. The dynamic input capacitance of the ASIC C_{CSA} can be estimated using the open-loop gain ($A_V = 4.8\ kV/V$) and the value of the feed-back capacitor ($C_{fb} = 100fF$) [90]. This results in approximately $C_{in} = C_{fb}(A_V + 1) = 480$ pF.

Considering the mean energy losses of the proton beam in the sensor volume, and assuming that charge collection efficiency is maximum for non-irradiated sensors, the ratio of charge integrated in the front-end electronics is approximately 0.9 ± 0.1. Among the measured values, the largest discrepancies ($\sim$14%) arise from *n-side* measurements of module T3.

5.6.1 Signal amplitude dependence with the detector bias voltage

As part of a systematic study, the performance of the module T5 is evaluated in a voltage scan. At low biasing, the digitization threshold is changed as a compromise between a reasonable spectra quality and the data rate. The values are shown in Fig. 5.21, where every point has been normalized according to the threshold.

The quality of the data below 80 V is not considered satisfactory. Convergence for *n-side* and *p-side* in 1 and 2 strip-clusters, is achieved at voltages higher than 140 V. This could be also recognized as an indication that the sensor is fully depleted. Error bars are estimated considering the errors of the fitting procedure, the systematic fluctuations in the digitization threshold and the ADC gain of the STS-XYTERv2.

Another observation that can be made from Fig. 5.21 is that amplitudes of the 2 strip-clusters are systematically higher than of the 1 strip-clusters. The reason for this can be understood as the following. When a particle hits an inter-strip gap, a 2 strip-cluster is reconstructed when

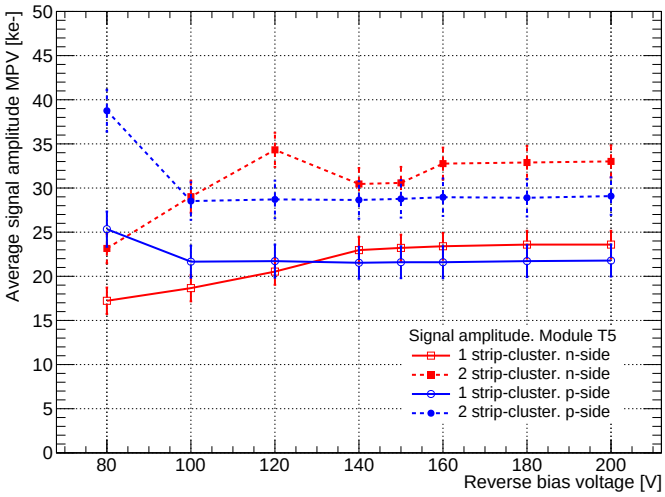


Figure 5.21: *Dependence of the total cluster amplitude with the sensor bias voltage.*

the amplitude on the both nearest strips exceeds the threshold. Given a constant position of the particle in the interstrip gap, and a constant ratio of the charge sharing between the strips, the particles that deposit more energy in the sensor are more likely to create 2 strip-clusters.

5.6.2 Angular scan

The monochromatic, well focused proton beam with energy close to MIP facilitates to test the detector response function for inclined tracks. During the operation of the final STS detector, particle tracks at different incident angles will reach the sensors. The incident angle determines the minimum physical size of the clusters. Other effects like charge sharing among the strips, diffusion, cross-talk and electronic noise dictate the size of the signal in every channel. The collected signal is then finally shaped by the front-end electronics according to the digitization threshold.

Several tests have been carried out with different detector modules and readout electronics during the STS irradiation campaigns in 2013 and 2014. Such studies allowed to test the detector response model [84]. This test complements the results obtained during the previous campaigns. In this case, the STS-XYTERv2 ASIC was used to read out the sensors and due to high noise and data rate issues, the threshold was kept relatively high in the chip. As explained in previous sections, this limited the cluster size distributions.

During the tests, the module T5 was placed at different angles with respect to the perpendicular beam direction. The module was mounted in a movable platform with automated control. The system enabled to adjust the azimuthal position with precision of 0.5°. The scan was carried out on both sides of the perpendicular direction at angles between 5° and 20°, as shown in Fig. 5.22.

The module T5 was operated at a bias voltage of 160 V and thresholds were kept at 11.4 ke^- for *n-side* and 14.9 ke^- for *p-side*. The event selection procedure described in previous sections was applied to the data. Since the cluster size distribution is sensitive to the charge sharing effects, it was chosen to compare the results. Figure 5.23 illustrates the mean cluster size as a function of the track inclination angle for both sensor sides. The distributions are symmetric with respect to the perpendicular direction.

Even for heavily inclined tracks ($\geqslant 20°$), the measured outcome are mainly clusters with size below 2-strips. This result can be explained as a consequence of the large threshold and possible

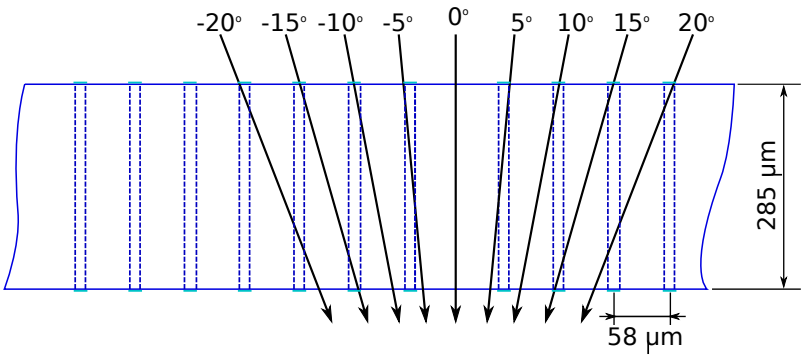


Figure 5.22: *Schematic representation of particle tracks crossing the silicon sensor at different angles.*

hit losses. The effect is more evident in the *p-side* of the module, where the threshold is 1.3 times larger than the *n-side*.

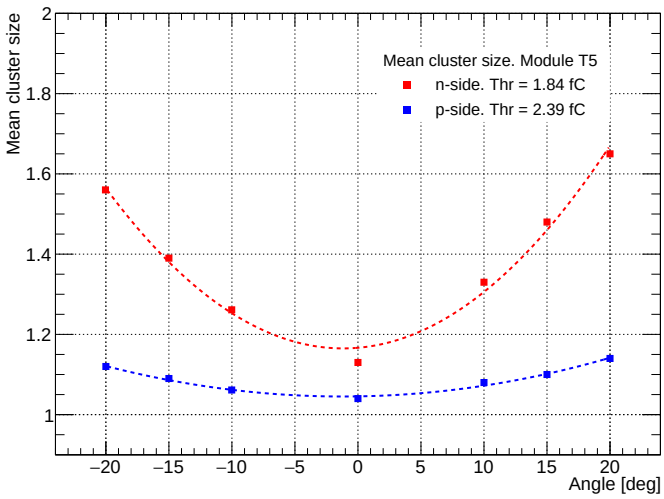


Figure 5.23: *Mean cluster size as a function of the particle's incident angle.*

5.6.3 Evaluation of signal-to-noise ratio

One of the key parameters to evaluate the detector performance is the SNR. To estimate this value a fully integrated system is required: sensor, microcables, and readout electronics. The test modules are built using prototype components close to their final version and they are operated within a data acquisition system that resembles the definite one. These reasons explain why they are considered a convenient setup to assess the SNR. Moreover, the beam line with protons of 1.7 GeV/c momentum is also a good platform for such purpose, since it provides an approximation to the real CBM environment.

Along this chapter, it has been reported the value of the signal amplitude for both modules. Taking into consideration the noise levels described in Table 5.2, the SNR is calculated for every detector side. It is important to mention that only 1 strip-cluster signals are considered, since the measured amplitude for 2 strip-clusters are not considered MIPs. Results from the modules are summarized in Table 5.3 [143].

Table 5.3: *Values of SNR measured with modues T3 and T5.*

		Signal to noise ratio
Module	Polarity	1-strip cluster
Module T3	*n-side*	16.8 ± 2.6
	p-side	16.3 ± 2.4
Module T5	*n-side*	8.3 ± 1.3
	p-side	5.8 ± 1.0

It can be noticed that this ratio includes all effects, for example, noise due to the stray and parasitic capacitances, strip resistance, not proper ground connection as well as signal losses due to charge sharing and higher thresholds. Even if the measured amplitude is approximately the same for both modules, the ratio degrades mostly in module T5 due to the poor noise performance. Module T3 shows good SNR, which coincides for both detector sides.

The SNRs in module T3 proved the detector reliability, although they are close to the safety margins for acceptable performance. To understand whether the obtained values of SNR are sufficient, it is also necessary to consider the impact on the reconstruction efficiency and the momentum resolution of the full detector. The effect on these observables has been studied using realistic simulations [84] and highlighted in Chapter 2, section 2.8. They have shown that system performance deteriorates significantly at SNR values lower than 10 and noise levels above 1500 ENC(e^-).

5.7 Summary

The tests carried out in the beamtime at COSY, Research Center Jülich, with a relativistic proton beam of 1.7 GeV/c momentum, allowed to study the performance of the first STS prototype modules. Each module was read out using the STS-XYTERv2 front-end electronics bonded onto a FEB-B, i.e. interfacing 128 strips per sensor side. Two detector modules proved operational in the beam line and were used to determine system time resolution and to characterize the signal amplitude distribution for different thresholds and beam incidence angles. An effective ground and powering scheme was developed for operating double-sided silicon sensors in a symmetric and floating configuration. An important step towards the mitigation of the system noise was using a cross-capacitor for connecting the FEB reference potentials. The overall system noise was measured as a function of the sensor reverse bias voltage, resulting in levels of approximately 1200 ENC(e^-) for one of the modules. The SNR was evaluated for 1 strip-cluster signals in both modules. Module T3 show ratios above 15 for both sides, while performance in module T5 was moderated by the large noise.

A logic error in the ASIC, triggered when more than seven channels are fired within a narrow time window, badly affects the readout rate and quality of the data. These studies allowed the identification of the error, which has been fixed in the next revision of the chip.

Chapter 6

Assembly and test of STS modules for CBM Phase 0

Towards the realization of STS, the assembly and operation of the first fully assembled modules were necessary and essential achievements. A small-scale prototype of the STS detector, named mini-STS (mSTS), has been built as part of the activities of the CBM Phase 0. mSTS has been conceived as two small tracking stations built from 13 STS prototype modules. Along the module assembly procedure, the quality assurance (QA) of the ASICs is a prerequisite to ensure that the chips are operational and they correspond to the CBM specifications. The following chapter describes in a first part, the development of QA procedures for testing the STS-XYTERv2 ASIC. The second part highlights the results of testing the FEB-8 and the first produced modules in a custom designed setup. The final section illustrates the recent activities of the mSTS project, its installation in the beam line and the first experimental results obtained in Ag+Au collisions at 1.58 AGeV at SIS18.

6.1 The mCBM experiment

In the context of the FAIR Phase 0 activities, mini-CBM (mCBM) is a precursor of the CBM experiment, a test setup whose main purpose is to prove the concept of free-streaming data generation, transport and reconstruction as to be applied in the final experiment [71]. By now, the detector design and front-end electronics components for CBM are largely completed; therefore, mCBM represents the next step in testing, integrating and optimizing the full system under realistic experimental conditions.

The mCBM project runs during the period 2018-2021 using the existing GSI/FAIR accelerator facilities [71]. The experiment uses heavy ion beams from SIS18 at energies between 1 – 2 AGeV and intensities up to 10^8 ions/s. The compact setup is about 3 m long and is positioned downstream a solid target under a polar angle of about 20°–25° with respect to the primary beam axis. mCBM includes detector modules from most CBM subsystems (STS, RICH, MUCH, TRD, TOF) and has been successfully installed in the detector test area HTD, situated at the beam entrance of the experimental area Cave-C (HTC) [71, 144]. The mCBM setup intends to shed lights on how to test and optimizes:

- the operation of the detector prototypes in a high-rate nucleus-nucleus collision environment;
- the free-streaming readout chain including the data transport to a high-performance computer farm;
- the detector control system;

- online tracking and event reconstruction as well as event selection algorithms;
- offline data analysis.

Commissioning and running mCBM will complete our knowledge on proper functioning as well as on the performance of every CBM subsystem and significantly shorten the commissioning period for the full experiment at SIS100.

6.1.1 mSTS in the context of CBM Phase 0 activities

The mSTS detector has been conceived as two small tracking stations, built from prototype elements of the STS detector. In comparison with the full STS detector, several simplifications have been made, giving room to focus on a few essential components and system design aspects [145]. The demonstrator is placed close to the target, in the angular range from 2.5°–25°. mSTS stations will accommodate in total 13 silicon modules, arranged in five carbon-fiber support structures, also called ladders. The upstream station uses two ladders carrying two modules each, while the downstream station is built with three ladders of three modules each [71, 145].

Figure 6.1 shows the scheme of the first station, where every ladder is mounted into an aluminum C-frame. Every module comprises a double-sided silicon microstrip sensor, segmented into 1024 strips per side. Each sensor side is read out by a custom designed FEB-8. The 13 microstrip sensors represent a total of 13 × 2048 strips and thus more than 26 000 readout channels grouped in 208 STS-XYTER ASICs. The front-end boards are attached to water-cooled plates to remove the dissipated heat. In the vicinity of the stations are mounted the C-ROBs and power boards (POB). The two stations are housed in a box, that provides shielding against light and electromagnetic interferences. The box has a low-mass beam window directly in front of the sensors. Inside of the box, the sensors are operated at ambient temperature [145].

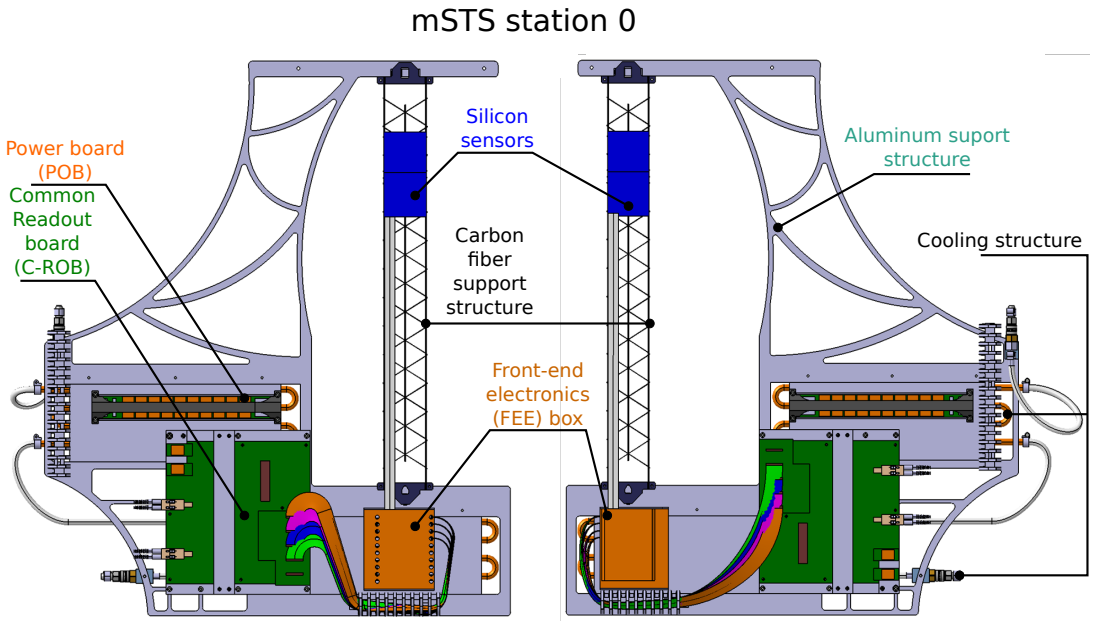


Figure 6.1: *Schematic representation of Station 0 in mSTS. Besides the detector modules, other components such as POB, C-ROB and the cooling services are integrated in the aluminum support structure. The C-frame on the right is flipped in the final setup.*

6.2 Assembly of the first STS detector modules

The assembly of the first STS fully assembled modules was an important and essential achievement for the STS project. Every module was assembled following a well tested workflow [146], developed to guarantee reliable and reproducible results. This process is summarized in the flow diagram in Fig. 6.2.

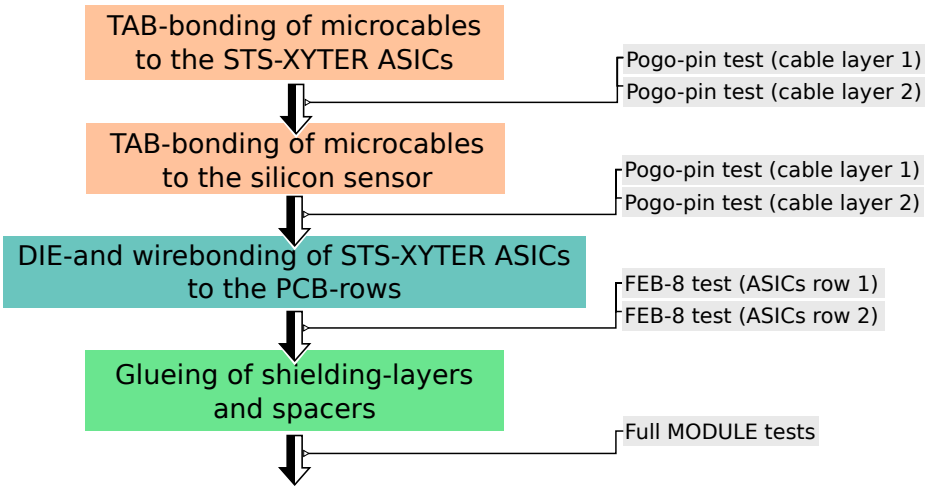


Figure 6.2: *Workflow diagram of the CBM-STS module assembly and the different tests carried out during the procedure. The different steps are ordered to optimize aligning, bonding and glueing processes, and hence to obtain reliable and reproducible results.*

Modules were built using silicon sensors of 6.2 × 6.2 cm^2 size, the longest existing microcables of approximately 50 cm length and two FEBs-8 carrying 8 STS-XYTERv2 ASICs each one [147]. Two external shielding layers were soldered to the ground point on the FEBs-8. Sensors and ASICs were also tested in advance and the quality of the TAB and wire bonding was checked during the different assembly steps [147]. A completed module, before the soldering of the shielding layer is depicted in Fig. 6.3. For the completion of the first mSTS station, four modules were assembled using the STS-XYTERv2 ASIC. According to their position in the ladder and the right or left orientation on the half units station, they are labeled as 01_Tr, 02_Tr, 01_Tl_2 and 02_Tl.

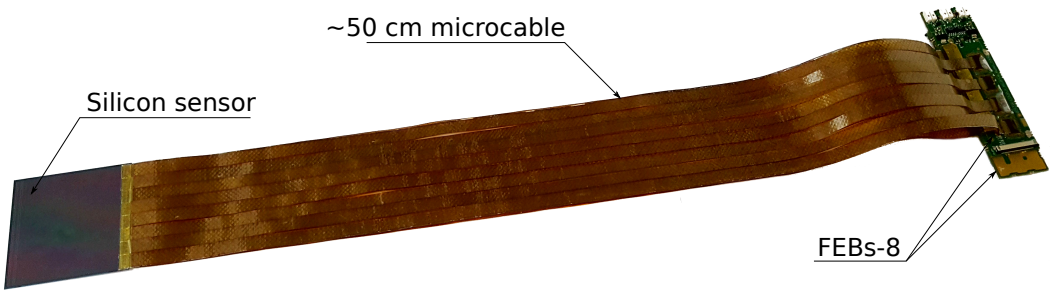


Figure 6.3: *STS detector module assembled with a 6.2 × 6.2 cm^2 silicon sensor, microcables of ~50 cm and two FEBs-8 carrying the STS-XYTERv2 ASIC.*

6.3 Quality assurance procedures for ASIC testing

A prerequisite for the assembly of functional detector modules is a rigorous QA of the components, i.e. sensors, microcables and readout ASICs. The aim of these procedures is to ensure that all constituents are functional, without defects and that they correspond to the CBM specifications [143]. For each detector component, elaborated QA procedures have been further developed. Optical inspection tools have been used to check any damage caused by handling the sensors and/or imperfections in the sensors structure [148], as well as to measure the position of silicon sensors mounted onto a carbon fiber structure with a few microns precision [149]. Electrical inspection reveals electrical properties of the sensor and provides a complete map of good/bad strips [150].

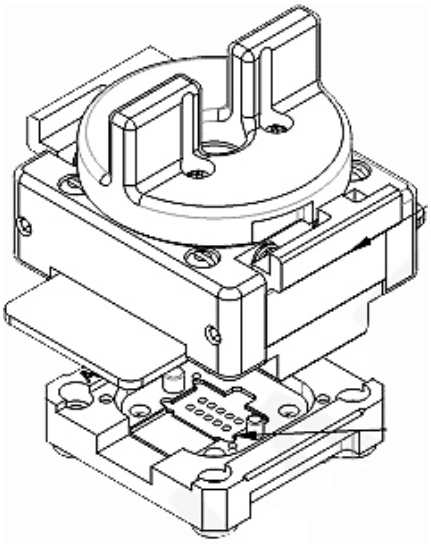
Acceptance criteria are also required to decide whether each component, or the full assembled module complies with the requirements. In this direction, an important element to consider is the influence of the fraction of defective (dead or broken) channels on the STS tracking performance. The impact of the number of dead channels in the reconstruction efficiency, momentum resolution and amount of ghost tracks has been investigated using realistic simulations [143]. It has been proven that having in total 3% of dead channels drops the track reconstruction efficiency from 95.5% to 94.4%. Based on this precedent, realistic acceptance criteria for sensors (below 1.5% dead channels) are applied, leaving margin for other issues that might appear during the assembly.

Besides the optical and electrical QA for every sensor, ASICs are also an important component to check before the modules production. The development and test of a QA procedure to evaluate each ASIC must assess the correct operation of the chip, and also establish a decision criteria based on the number of defective channels, power consumption and other operational aspects. The description of the ASICs QA procedure is detailed in subsection 6.3.2.

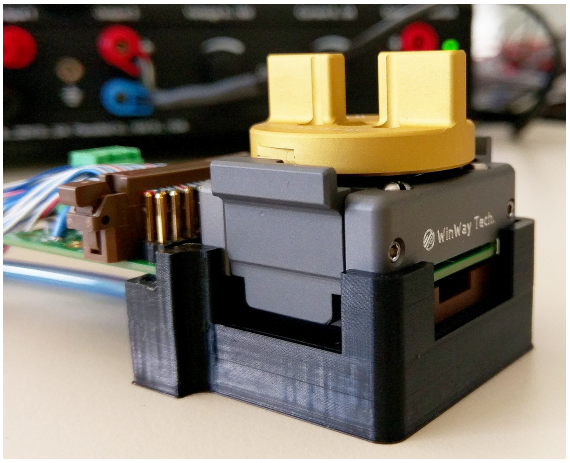
6.3.1 Experimental setup

The basic component of the ASIC test setup is the pogo-pin station, see Fig. 6.4a. It consists of a custom-designed socket developed by the WinWay Technology Company [151]. The ASICs are placed and fixed in a bottom socket using vacuum. The closing lid contains a set of spring-loaded needles that interfaces the chip via its dedicated pogo pads. In total, the STS-XYTERv2 possesses 53 square pogo-pads, built on the surface of the chip [147]. Pogo-pads have larger area $150 \times 150\ \mu m^2$ compared to the typical bonding pads and allow biasing the chip and enabling test functionalities [85].

A picture of the latest version of the pogo-pin station is shown in Fig. 6.4b. A custom-designed PCB interfaces the test station with a standard STS-XYTERv2 readout chain. The board is designed with certain flexibilities such that some chip potentials can be routed to external input/output pins. In addition, LVDS signals are routed to an external connector as in the prototype FEB-B. This feature permits to make use of the same testing firmware without further modifications. To read out the ASICs, the chain of components is the same as in a standalone FEB-B readout. It consists of a FPGA layer implemented on the AFCK board and an interface card for the pogo-pin board. Figure 6.5 shows the STS-XYTERv2 ASIC placed inside the holder. A thin entrance window on the side of the channel's input allows testing ASICs with bonded microcables.



(a) *Schematics of the pogo-pin station with latches and knob to get the pins in contact with the ASIC. Bottom socket with the cavity for the ASIC and vacuum fixation [151].*



(b) *Picture of the prototype pogo-pin station. The bottom socket is held by a custom 3D printed support.*

Figure 6.4: *The pogo-pin station is the main tool for QA tests of the STS-XYTERv2 ASIC.*

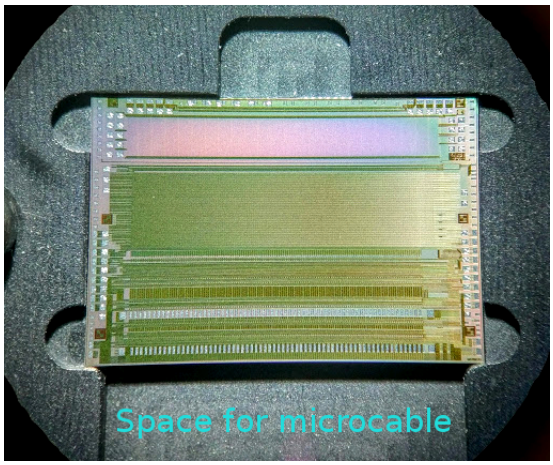


Figure 6.5: *STS-XYTERv2 ASIC placed on the bottom socket of the pogo-pin station.*

6.3.2 Development of the ASIC testing protocol

While some general electrical tests are carried out for every ASIC at the wafer level, in-depth QA is done exclusively in every center before the module assembly. The QA checks for any damage caused during the wafer tests, ASICs dicing, handling and production issues that can result in malfunction of the chips.

The ASIC QA procedure focuses on testing whether communication and basic functionalities on the chip are operational. It also assesses the power consumption of the chip as an indicator of possible failure. Moreover, it implements a general check for each channel [147]. The testing protocol is divided in five main phases. Each of them addresses a critical point in the ASIC

operation. The different stages are ordered according to their functional complexity level. Figure 6.6 shows the workflow during the ASIC testing stage. The main phases are:

- **Synchronization:** This is the first step in the full chain and it checks that communication with the ASIC via the digital back-end is possible. In case of a failure during this stage, the synchronization process is relaunched. In case of 3 consecutive failures, the chip under test is marked with communication problems and the entire procedure is terminated. Otherwise, the ASIC is ready for next phase.

- **Configuration:** During this stage writing/reading actions are checked. Ahead of this process, the ASIC unique ID is read back. This information has been fused into the chip during the wafer level tests. In case this step was not yet implemented, an identification code is given to every ASIC based on its position in the packaging box 6×9, following the labeling format *"box_No._asic_POS[col,row]"*. This method demands a special attention from the user point of view, since every ASIC must be traceable along the full assembly.

  Every ASIC is then configured with typical operational values. This translates into writing and reading more than 4400 and 8500 registers, respectively. In case of errors in one or more registers, the process is repeated to confirm the mismatch. The current of the ASIC is measured immediately after the first configuration is loaded. The standard current value corresponds to approximately 0.6 A.

- **Analog response check:** This test relies on the internal pulse generator to check whether a selected channel responds to injected pulses of different amplitudes. The process is performed for both polarities, which also allows to test the operation of the polarity selection circuit. In case no hits are generated, the process is repeated for two other channels. Three channels without analog response set the "ASIC with problems" flag and terminate the procedure.

- **ADC and FAST discriminator check:** This step is essentially an extension of the previous one to all channels. It allows to check channels with problems. Pulses with different amplitudes, up to 14 fC, are injected at the channels input. Amplitude and time response in the discriminators are checked by using the dedicated counters. A channel is marked broken, when no signal is found in the timing discriminator or at least four ADC discriminators. The total number of broken channels defines the QA criteria (QA = 1 - $broken/128$). This process finishes the sequence of basic tests in the ASIC.

- **ADC and FAST discriminator calibration:** This process is only executed if it is required by the user. It is meant to be performed before bonding the ASIC to the microcables and only for those chips that matched the QA $\geqslant$ 98% criteria. The calibration procedure, as described in Chapter 3, subsection 3.7.2, is performed for a specific polarity defined by the user.

The collected data are initially stored in the format of ".txt" file that also contains the date and time of the measurement as well as the assembly stage. Afterwards, data is saved in FAIRDB [152], a dedicated data base branch for storing the QA results of every assembly components in the CBM experiment.

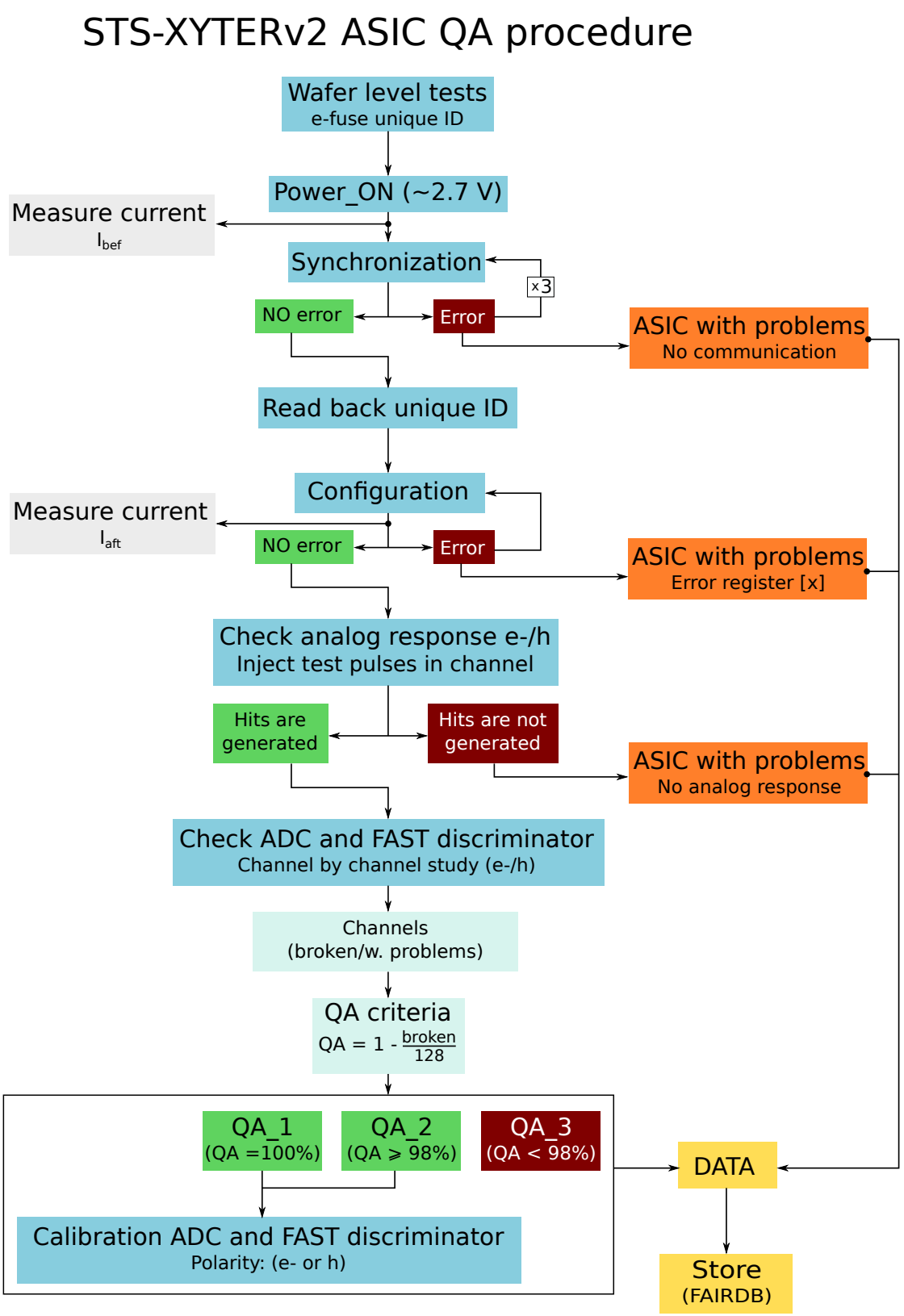


Figure 6.6: *Testing protocol for QA of the STS-XYTER ASIC.*

Across one year and a half of research and production phase, a total of 339 STS-XTYTERv2 ASICs have been tested and used in the assembly of prototype FEB-B and detector modules. At this stage, only 20 chips have shown problems, which can be considered as a satisfactory result. Out of them, 14 ASICs have been identified with critical issues. These have not been used in the next assembly stage. Crucial problems identified during tests are mostly related to communication with the digital interface of the ASIC and the response of the analog front-end [147]. Since only small discrepancies are found among the tested chips, more rigorous selection criteria can be established. The main findings are summarized in Table 6.1.

Table 6.1: *Statistics on testing the STS-XYTERv2 for module assembly.*

Total number of tested ASICs	339
ASICs with problems	20
Synchronization problem	8
No analog response	5
High power consumption	1
Single broken channel	5
Multiple broken channels	1

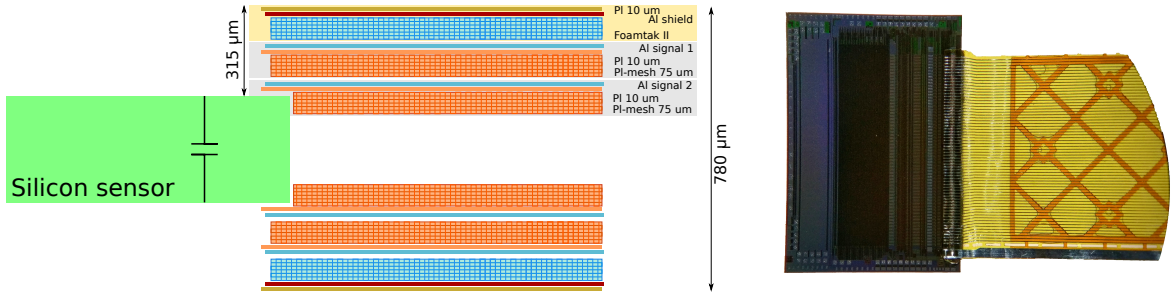
Although 6 chips in total were identified with broken channels, only those with one single broken channel have been used in the assembly of prototype FEBs-B. With a yield larger than 90%, the acceptance criteria for ASICs to be used in the module assembly is set such that only chips without problems are used. This decision is made considering that during the next phases, some channels might be partially or totally damaged. Therefore, as a QA criteria for ASIC testing, only those with no broken channels will be used in the final module assembly.

6.3.3 Measurement of microcables

Ultra-thin microcables are used to interconnect the silicon sensors and the readout electronics, providing minimized material budget. Microcables of different lengths, up to 50 cm, are foreseen to be used in the final STS detector [153]. They are composed of a stack of analog signal cables, meshed spacers and shielding layers. Figure 6.7a illustrates the cross section of microcables attached to a silicon sensor. Each multilayer analog cable consists of two signal layers built from aluminium-polyimide adhesiveless, two meshed spacers based on Kapton (75 μm thick) and a shielding layer with Foamtak II spacer (foamed polystyrene 165 μm thick) [154].

In addition to the total strip capacitance, microcables also contribute to the load capacitance seen by the front-end electronics. Therefore, it is important to characterize their contribution to the overall noise of the system. On the other hand, the cable dependent noise can be exploited to measure the quality of the bonding process. When connecting a microcable to the input of an ASIC channel, the amplifier senses a large capacitance that evidences as an increment in the noise level. Unconnected channels, however, remain silent or noiseless unless a very large cross-talk exists or common-mode noise is introduced on the chip via the ground [147, 155].

To distinguish among connected and unconnected channels using the pogo-pin station, two approaches are studied. The first and also the simplest one, consists of opening the ASIC global gate for a few seconds and to allow noise hits to be counted. Figure 6.8a shows an example taken with a set of 50 cm microcables bonded onto the STS-XYTERv2 ASIC. The number of noise hits across the chip is approximately the same, except for unconnected channels where there is a clear reduction in the number of counts.

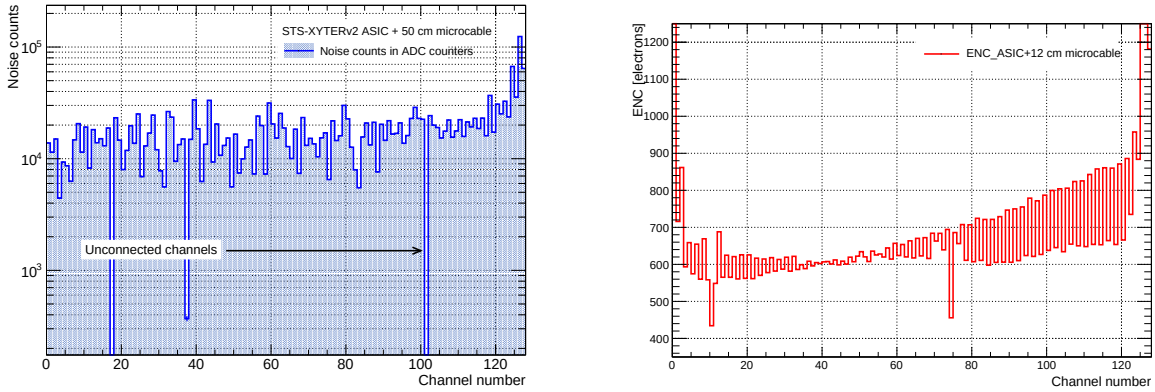


(a) *Cross section of two layers of microcables connected to a silicon sensor.*

(b) *Image of STS-XYTERv2 ASIC connected to a microcable layer.*

Figure 6.7: *a) Schematics of the cross section of two layers of microcables connected to a silicon sensor. b) Image of the first layer of microcables bonded onto the front row of channels in the STS-XYTERv2 ASIC.*

The second approach performs a *s-curves* scan for at least one discriminator per channel and measures the absolute noise level. By comparing all channels, it is easy to find if the channel has been correctly bonded. This method does not only require more time and computational resources, but also, in extreme cases, like 50 cm long microcables, it might require to shield the microcables in order to not saturate the discriminator counters with noise hits [155]. This method is illustrated for a set of 12 cm microcables in Fig. 6.8b. Two channels with noise level below 500 ENC(e^-) can be distinguished and marked as broken or unconnected.



(a) *Noise counts in all channels of the ASIC bonded onto 50 cm microcables.*

(b) *Noise measurement (using s-curves) across all channels for 12 cm microcables.*

Figure 6.8: *Identification of unconnected channels during the TAB-bonding process of the microcables to the ASIC. Two methods based on counting noise hits or measuring the overall system noise can be used to determine whether a channel is connected or not.*

In Chapter 3, subsection 3.9.4 the ASIC noise as a function of the detector capacitance has been investigated. In that study, low leakage capacitors were used to represent the module, resulting in a linear dependency with average slopes of ∼27.3 ENC(e^-)/pF and ∼43.9 ENC(e^-)/pF for the ADC and FAST discriminator, respectively. During the assembly procedure, it is also possible to cross-check if this result is consistent for real module components. Under such premise, three ASICs have been selected among those that passed the QA procedure. The noise on the bare chips was measured using the pogo-pin station, showing that there is no significant differences among

them 494 ± 46 ENC(e^-). In the next stage, microcables of different lengths (12, 25 and 50 cm) are bonded onto the chips, and the overall noise is determined. To achieve a correct estimation of the noise level, microcables are shielded using two layers of conductive copper tape connected to the ASIC ground potential.

Figure 6.9 shows the dependence of the overall noise on the cable length. The load capacitance at the input of the amplifier can be accurately estimated considering the total capacitance per unit length of the microcable as 0.38 ± 0.02 pF/cm [106]. These values are plotted in an alternative axis to guide the eye. Each point represents the average value among all channels while error bars show the standard deviation. The linear correspondence is observed for the ADC and the FAST discriminator, resulting in 28 ENC(e^-)/pF and 51 ENC(e^-)/pF, respectively. These values confirm the previous measurements and also show that proper shielding can reduce considerably the electromagnetic interference, even for larger structures like the 50 cm microcables. In addition, results set a reference baseline for the noise level on the modules. Once the silicon sensors are connected, an increment on the noise level is expected mainly due to the very large sensor capacitance and its leakage current.

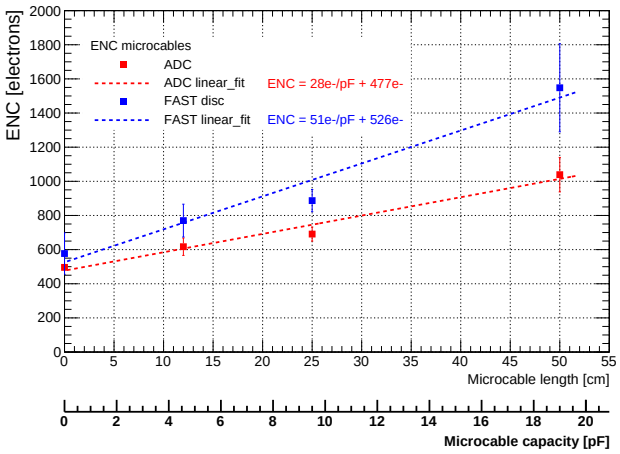


Figure 6.9: *Linear dependence of the noise in STS-XYTERv2 ASIC with the microcable capacitance.*

6.4 The front-end board FEB-8

The development of the FEB-8 aims at realizing a very highly integrated board carrying 8 STS-XYTERv2 ASICs to read out 1024 channels, corresponding to one sensor side [156]. Many are the challenges to consider in the design of the FEB-8, such as:

- the mechanical integration of a large number of electronic components in a reduced space;
- the high density of wire bonds and bond-pads necessary for connecting every chip;
- the routing of LVDS signals and clock lines across the board;
- the integration of a last stage of power regulation;
- a proper cooling interface for removing the heat dissipated by every ASIC.

The FEBs-8 are fabricated in two flavors that mirror each other. This feature, allow to read every sensor while keeping data cables and powering on the different sides. The already existing versions of the FEBs-8 use commercially available LDOs for supplying the required voltages (1.2 V and 1.8 V). However, the final version will use the custom-designed, radiation hard SCL LDO. This also represents a challenge, because of the difficulties on bonding these chips due to their very small bond pads [147, 156].

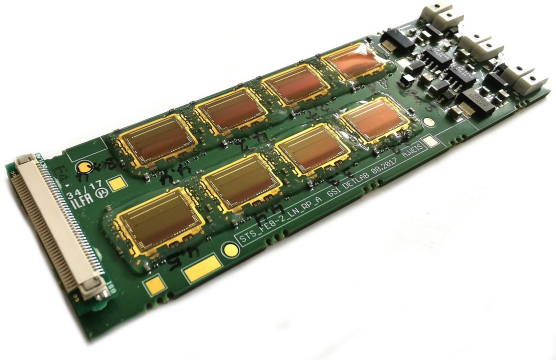


Figure 6.10: *Image of a prototype FEB-8 assembled with 8 STS-XYTERv2 ASICs.*

Figure 6.10 shows an image of one of the existing FEB-8 populated with 8 STS-XYTERv2 ASICs. These boards are designed to have up to 2 up-links per ASIC. In the final system, a small fraction of boards will have up to 5 up-links per ASIC. They will be used for reading out sensors located in the central part of the first stations. In order to compensate the lack of space on the board, the HV capacitor array is placed below the ZIF-connector. The 36 vertically arranged HV ceramic SMD capacitors (3.3 nF / 500 V / type 0603) are responsible for the galvanic isolation of the data signals. This is one of the most sensitive parts in the design and can be easily damaged from lateral forces or improper handling [156].

An important step before using the FEB-8 in the module assembly is to check if the design requirements are fulfilled. Important features, such as the communication with each individual chip, the digital signal integrity, the overall power consumption and thermal behavior are thoroughly tested.

After wirebonding each row of ASICs to the FEB-8 (i.e. with 4 or 8 ASICs mounted on the FEB-8), a basic communication and functionality test is done. Power consumption with and without clock signal is measured and compared to the expected values. The synchronization procedure is executed for each ASIC and a set of configuration registers are written and read back. For a fully assembled FEB-8 or module, other important functionalities, directly related to the ASICs performance, are checked. ADC and FAST discriminator are properly configured using calibration values obtained beforehand, otherwise, each ASIC is undergoes a calibration process. This procedure yields satisfactory results as the ones obtained with the prototype FEB-B and the pogo-pin station. The absolute thresholds for time and energy measurements are shown in Fig. 6.11. It can be observed that the spread across the 1024 channels is in the order of 1.3% and 0.5% for the ADC and FAST discriminator, respectively. The ADC gain is uniform among the different chips, with a mean value of 0.336 fC/LSB and a narrow spread smaller than 0.5%, see Fig. 6.12.

Next phase in the testing process is the evaluation of the noise level of bare ASICs in the FEB-8. Figure 6.13 demonstrates that the performance for all the chips is similar. The average noise level is approximately 422 ENC(e^-) with a standard deviation of 73 ENC(e^-). The expected difference between odd and even channels is highlighted in the right histograms, see Fig. 6.13 *right*. Even channels show a narrower distribution around 383 ENC(e^-) with no significant difference

across the entire FEB-8. For odd channels, the average noise level has a wide range that extends from 350 ENC(e^-) until 650 ENC(e^-). Within every ASIC, there is a visible trend to increase the noise level towards larger channel number as expected in the v2.0 and explained in Chapter 3, subsection 3.9.2.

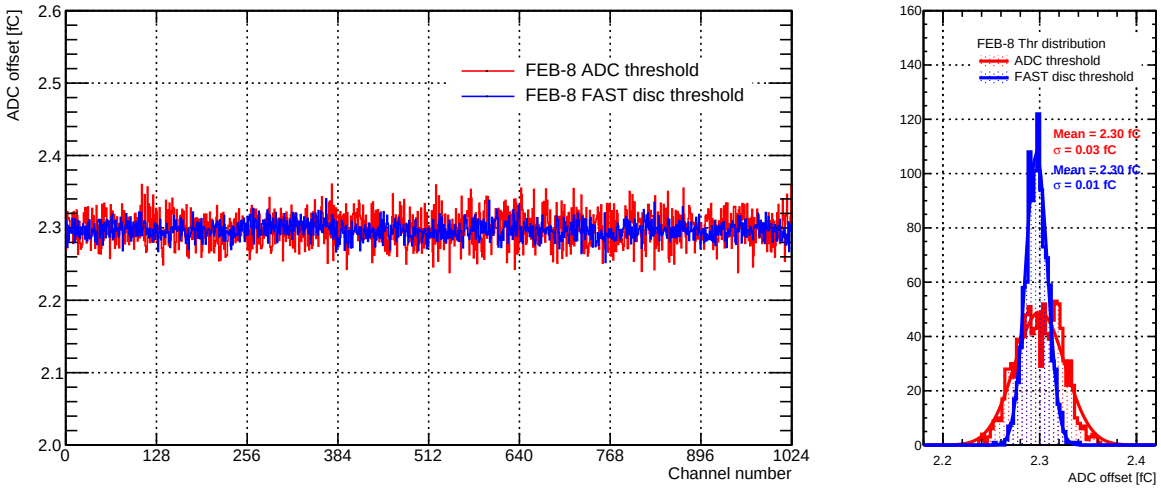


Figure 6.11: *Distribution of the absolute threshold in the FEB-8 after calibration.*

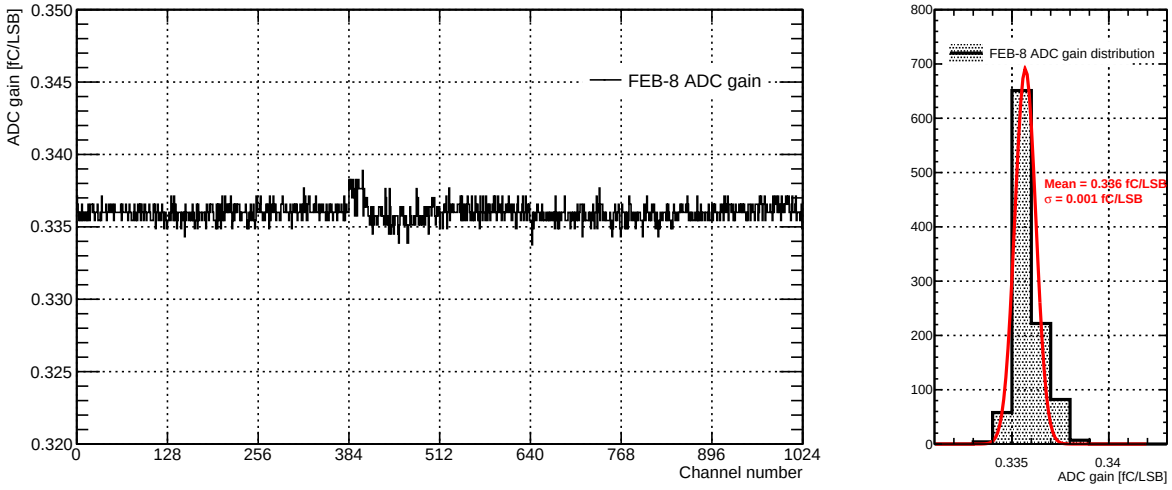


Figure 6.12: *ADC gain distribution accross 1024 channels on a FEB-8.*

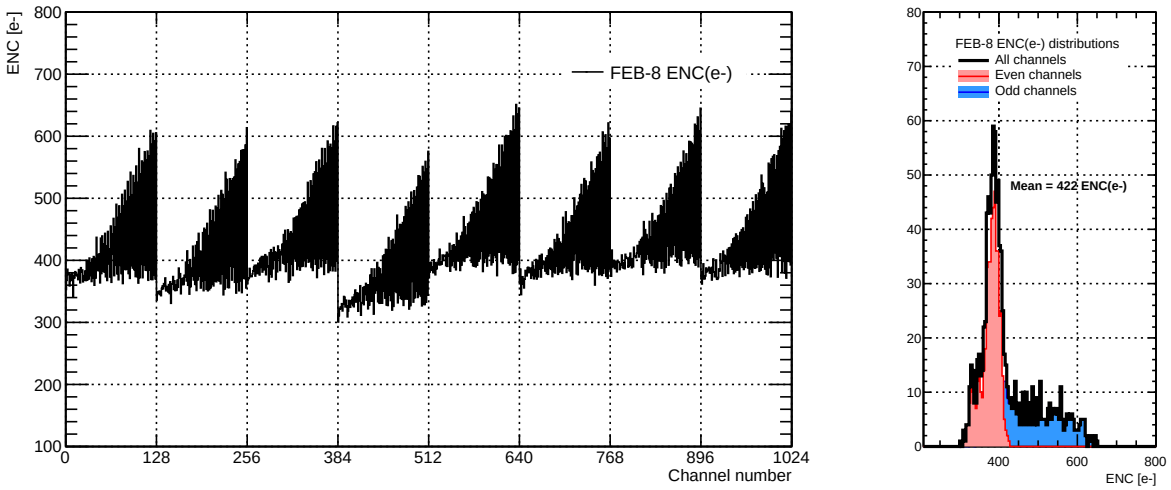


Figure 6.13: *Distribution of the overall noise measured in each STS-XYTERv2 of the FEB-8. On the right panel, the histograms of the noise distribution split according to the channel number (even and odd).*

6.5 Test of STS fully assembled modules

6.5.1 Test setup and readout chain

After the assembly of the module is completed, a set of tests is regularly performed to evaluate the operation and stability of the modules. A dedicated setup and a simplified version of the readout chain allow to carry out the tests with a fully biased sensor. The testing setup consists of a light-tight aluminum box, which also provides shielding against electromagnetic interference. It is equipped with a water cooling system for the FEB-8, and also integrates a holder for accurately positioning a radioactive source and performing position sensitive signal studies. Pictures of the test box with a module under test is shown in Fig. 6.14.

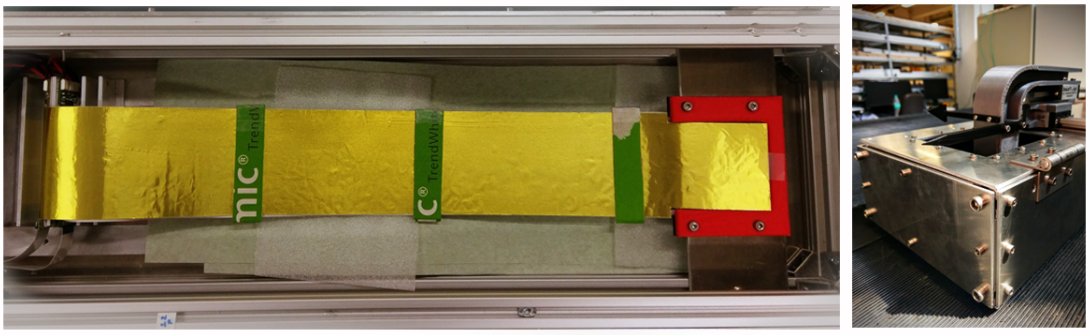


Figure 6.14: *Pictures of the module test box showing a module under test. The 3D printed sensor holder can be seen in red.*

In order to test the functionalities of the FEB-8 and the fully assembled modules, further developments of the DAQ and readout chain were fundamental. The completion of the chain included mainly the use of the C-ROB, as a layer for data aggregation after the front-end electronics and electrical to optical interface.

The C-ROB implements the full GBTx, slow-control and Versatile Link functionalities required by the STS and other systems [70]. The interface to the FEB-8 with all E-link and SCA functionality is realized on 2 FMC connectors with custom designed ZIF to FMC mezzanine cards. The DPB as a common hardware platform, is currently based on the AFCK board. The DPB implements the back-end of the optical interfaces to multiple C-ROB and also serves as interface to the detector control system (DCS).

6.5.2 Test results

For every module, operating parameters such as writing/reading configuration values, current consumption and the overall system noise are investigated. Results from module tests, before their installation in mSTS detector, are summarized in Table 6.2. Beyond the regular features check, the number of unresponsive ASICs as well as the number of broken channels are controlled. Since these are the first STS fully assembled modules, the acceptance criteria are not rigorously applied as this is still considered a learning phase.

In total three ASICs do not respond to synchronization commands. A careful analysis has revealed no signal on the ASICs up-links. In three other chips, marked with (†), communication is possible; however, their analog response is erratic and not well understood. Therefore chips are not operated and also considered as broken.

Table 6.2: *Test results for STS fully assembled modules.*

		Module			
Parameter	**Pol**	**01Tr**	**02Tr**	**01Tl_2**	**02Tl**
Broken ASICs	n	2†	1†	0	1
	p	1	1	0	0
Broken channels	n	9	5	4	19
	p	69	28	49	33
ENC [e^-]	n	2994 ± 343	1688 ± 241	1445 ± 198	1932 ± 270
	p	2022 ± 499	1600 ± 430	1633 ± 202	2057 ± 389
ADC gain [fC/LSB]	n	0.331 ± 0.004	0.335 ± 0.003	0.334 ± 0.002	0.342 ± 0.030
	p	0.335 ± 0.005	0.337 ± 0.003	0.334 ± 0.003	0.337 ± 0.002
ADC thr spread [%]	n	8.3	4.5	1.6	5.2
	p	6.1	4.1	2.5	2.6

†*ASIC can be synchronized but shows erratic analog response.*

The TAB and wire bonding of the silicon sensor, microcables and the ASICs are very sensitive points of the module. Even if bonds are protected with glue, they are under a constant mechanical stress during the assembly. When the TAB bonds are broken, either at the ASIC or sensor side, noise levels appear relatively low compared to well connected channels. By using this method, every unconnected channel can be identified. In general the total number of broken channels exceeds the acceptable value. The *p-side* statistics shows a larger number of broken channels compared to the *n-side*. Even if these parameters have been monitored during the full assembly procedure, inappropriate handling, thermal or electrical shocks could damage the object. Therefore, these tests can be also considered as indicators to built an acceptance criteria of the modules.

From the assembly point of view and in order to evaluate the bonding quality, it is worth

studying every channel individually. In the STS-XYTER ASIC, input pads are distributed over two rows. The front one, for even channels, is the first in the bonding process using aluminum polyimide cables. Afterwards, a protective layer of glue is applied and the microcable connecting odd channels is then bonded. During the tests, it was found that the number of broken channels is bigger for even than odd channels. The relative ratios 63% and 37% indicate that channels in the front row are more affected than the odd channels during the assembly. Results are summarized for every module in Fig. 6.15. The number of broken channels does not include those belonging to unresponsive ASICs.

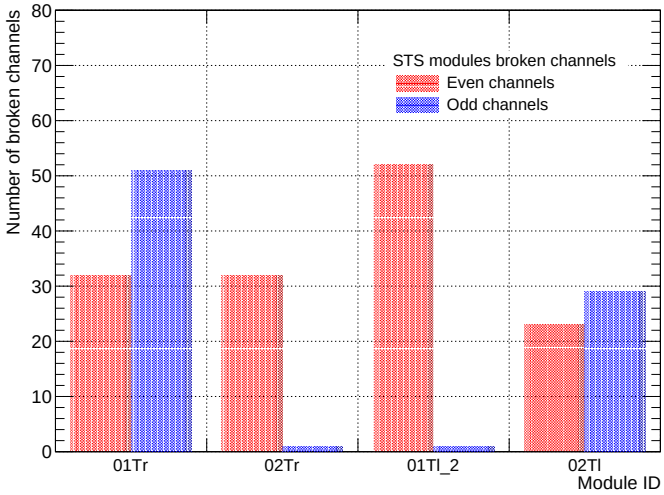


Figure 6.15: *Broken channels in each module separated in two groups according to their number: odd and even differences might help identifying some issues during the assembly.*

Regarding the overall ASIC performance, the noise behavior across the full module 01Tl_2 is shown in Fig. 6.16. ASICs have been arranged according to their position to read the silicon sensors. In addition, the noise performance of the FEB-8 is plotted to illustrate not only the absolute noise difference, but also a comparative measure for identifying broken channels. Besides the well discussed odd-even effect, the first readout ASIC of the *n-side* shows a relatively large noise in half of its channels. This effect can be related with a defective capacitor in the biasing line of the channels CSA.

In the module performance, not only low noise levels are required but also uniformity in the channels response with respect to ADC gain and threshold. Their distribution across all channels of module 01Tl_2 are illustrated in Fig. 6.17. In both cases, the relative spread among channels is below 5%, which can be considered as a satisfactory result. The average values for every module are listed in Table 6.2. Errors are defined as the standard deviation across all channels.

Module assembly and testing provided invaluable practice in handling and operating the STS modules. Among those were the development of iterative QA procedures during the assembly, e.g. using the pogo-pin station, finding a suitable balance between finding problems in the assembly and potential damage to the ASIC during testing. In addition, crucial experience in cooling the FEB-8 during operation was gained in order to avoid damaging the bonds due to thermal shocks [157].

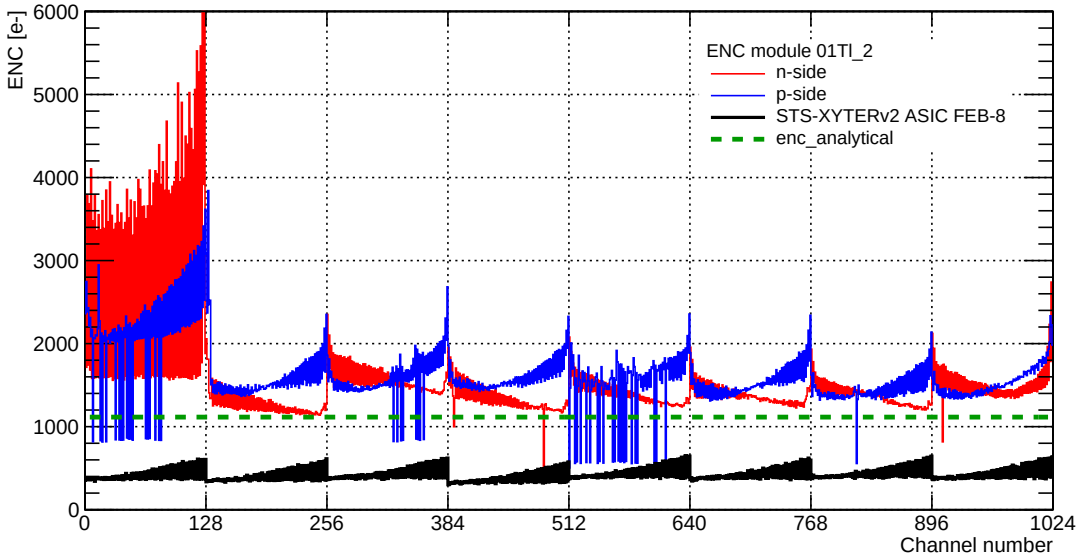


Figure 6.16: *Overall noise level in all channels of module 01Tl_2.*

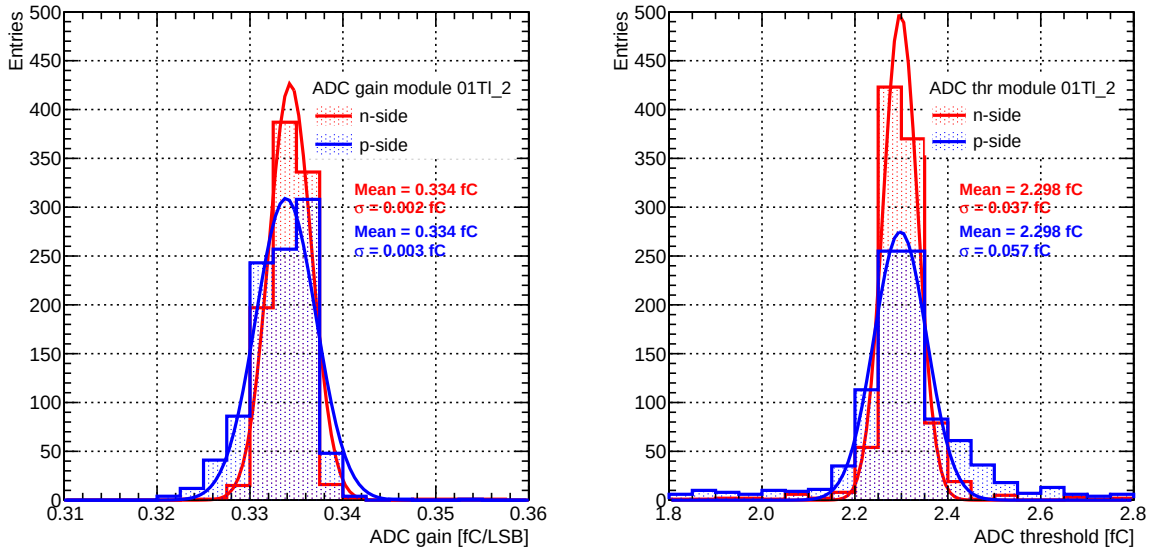


Figure 6.17: *Distributions of the ADC gain and threshold on module 01Tl_2 evaluated for both readout sides. Relative spread are lower than 5%, which can be assumed as a satisfactory result.*

6.6 Installation of mSTS

Two fully assembled modules were integrated into the first half-ladder for the STS demonstrator. The modules with right orientation, i.e. 01Tr and 02Tr, were used in the construction of the ladder. Afterwards, the ladder and other components such as the C-ROB and POBs were mounted onto a C-frame [145]. The full system was housed in a light-tight aluminum box that provides shielding

against electromagnetic interference. The first half ladder installed in the service box is shown in Fig. 6.18 *left* [145]. The box was designed with proper interfaces for the data, power connections and cooling pipes. The integration of the mSTS detector in the service box brought valuable insights about combining services such as:

- assembling and placing detector ladders;
- integrating different power domains into a common high voltage and low voltage power and ground scheme;
- cooling and cabling front-end electronics and power boards.

The full system was installed into the mCBM experiment at the end of November 2018, yielding one half of the first mSTS tracking station for mCBM start-up in December 2018. Figure 6.18 *right* shows the mSTS service box placed in the mCBM beam line.

Figure 6.18: ***Left:*** *Open detector box after full assembly of the main components.* ***Right:*** *Installation of mSTS in the beam line.*

6.6.1 mSTS power and grounding scheme

Noise problems are often not encountered during the design phase of a detector system. However, they tend to show up when the full system is installed and operated in its intended environment [158, 159]. In the case of silicon microstrip sensors, the very low signal levels and a considerable number of channels make them very sensitive to all kind of noise sources. External electromagnetic fields introducing pickup currents into the systems can be listed as one of the main causes. In addition, ground currents from large scale power supply networks may appear into the signal path and create additional noise. Careful design of grounding, shielding and power distribution is thus essential.

mSTS implements a symmetric and floating ground scheme for the sensor bias and the front-end electronics. Operating floating front-end electronics requires significant engineering effort. First of all, each module side would require a separate power domain [142]. Moreover, a DC-decoupling interface between the floating FEB and the data transport hardware (C-ROB) is necessary. Figure 6.19 shows the powering scheme implemented in mSTS, including the POB and the sensors. In the LV power line, radiation hard and magnetic field tolerant DC-DC converters are used before the linear regulators on the board [103, 160]. They are used to provide the required potentials for operating the front-end electronics on each side. Microcable shields are connected to the respective FEB grounds and the HV common return is connected to the mSTS enclosure. The mSTS box is grounded and electrically insulated from the mounting table. On the signal return path a cross-capacitor is placed as close as possible to the FEBs ground.

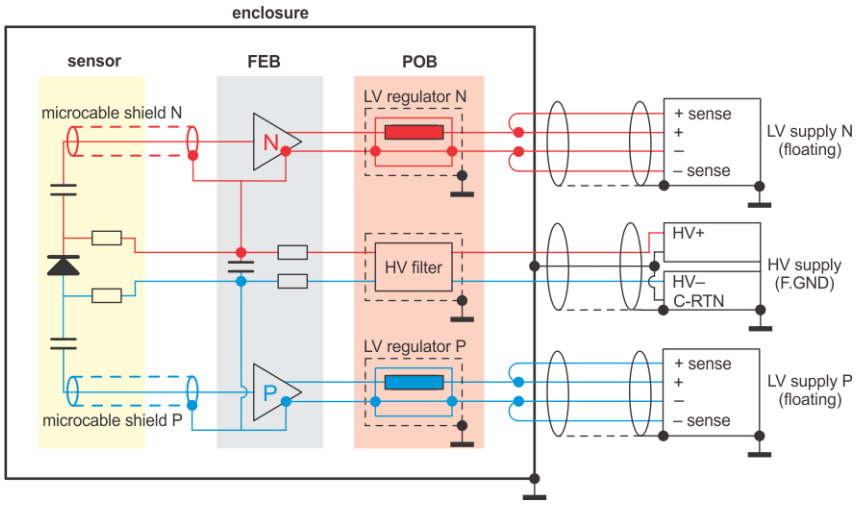


Figure 6.19: *Power distribution scheme for the mSTS detector.*

6.6.2 Preliminary results and main findings

During the commissioning run of December 2018, only one of the two detector modules proved functional. Since the replacement of a second module resulted a very risky and complex task, it was decided to rebuild the entire half-ladder with new modules. They were produced using the STS-XYTERv2.1 ASIC and labeled 01Tr_2 and 02Tr_2, due to their right orientation. The full Station 0 was then completed with the existing left orientation modules, e.g. 01Tl_2 and 02Tl built from the v2.0.

Along the mounting, testing and re-installation of mSTS in cave HTD, multiple chips start failing in the modules. It is considered that failures are probably consequence of thermal damage. When the chips are under operation, the glob-top protective glue dilates as a consequence of the dissipated heat on the ASIC. This can cause that wirebonds partially or totally break apart. A large effort currently focuses on determining whether this can be the main cause or other effects are also involved. Alternative glues are also under test.

In addition mSTS provided a good test scenario for checking the recently developed ASIC. The STS-XYTERv2.1 implements several improvements with respect to its predecessor. In terms of noise performance, the difference between odd and even channels is significantly smaller and the noise increment towards higher channel numbers is largely suppressed. These results are shown in Appendix C. Another solved issue in the new ASIC version is related to duplicated and missing hits.

Using realistic post-layout simulations, it was demonstrated that these errors rose as a consequence of improper matching between commands and data FIFO and the channels and data FIFO.

In the mCBM beam campaign of March 2019, valid data were acquired with the newly produced modules. Data taking from multiple running scenarios, e.g. different targets and beam intensities, verified their performance. The mSTS detector was exposed to the products of Ag+Au collisions at energies above 1.58 AGeV and overall interaction rates up to 40 MHz, which resembles the real conditions of the CBM experiment.

Figure 6.20 shows the mean time difference of mSTS signals with respect to a reference time measured by start T0 detector as a function of the signal amplitude. Data correspond to the measured time-walk of ASIC 4 in one of the FEBs. An expected delay of approximately 20 ns can be seen for low amplitude signals (below 5 ADC units) compared to larger ones. These values show a good agreement with the measured time-walk of the ASIC, see Fig. 3.30b. For large amplitude signals, the measured RMS ($\sim 5\ ns$) indicates a good time resolution achieved by the detectors. Since T0 time resolution is in the order of tens of ps, the overall RMS is mostly dominated by the mSTS contribution. The achieved resolution is consistent with the measured data in a relativistic proton beam at the COSY facility, see Chapter 5, section 5.3.

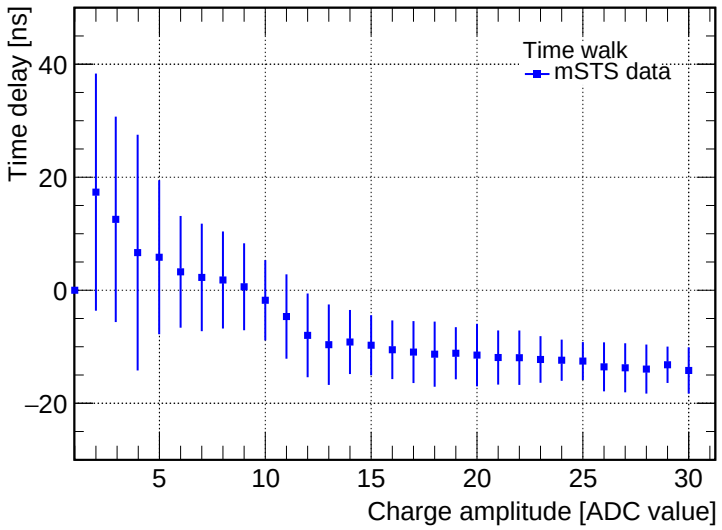


Figure 6.20: *Time-walk for ASIC 4 in FEB_2 calculated after selecting the true signal.*

Figure 6.21 shows the distribution of 1 strip-cluster signals measured in the ASIC 4 of different FEBs. Charge spectra are built based on two main requirements: a time coincidence with T0 detector and a single hit across all channels in the ASIC. In addition, the effective ADC threshold is different among the FEBs, decreasing from FEB_1 towards FEB_4. According to the calibration values, the most probable value extracted from the distributions on FEB_2 and FEB_3 corresponds to approximately 26 ke$^-$.

Another important achievement during the beam campaign was the successful implementation and operation of a close-to-final version of the readout chain. mSTS was integrated with other CBM subsystems into a common free-streaming DAQ that proved functional for different running scenarios and up to 40 MHz interaction rate.

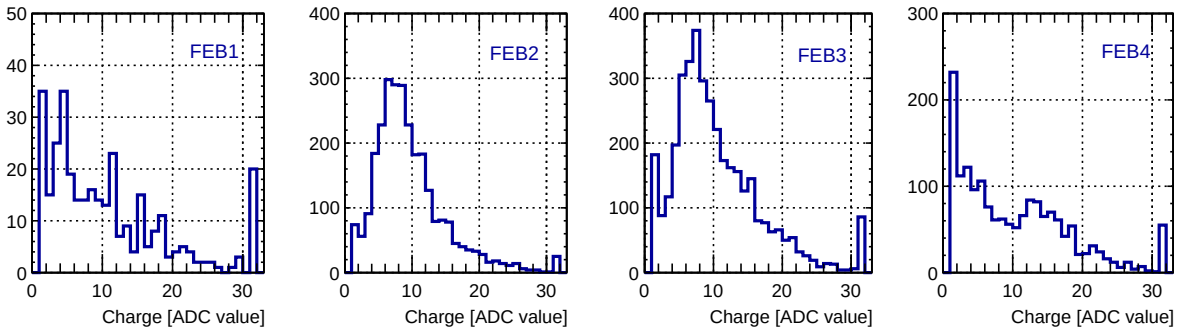


Figure 6.21: *Charge distribution for 1 strip-cluster signals measured in ASIC 4 of different FEBs. The effective ADC threshold is different among the FEBs, decreasing from FEB_1 towards FEB_4.*

6.7 Summary

This chapter has presented multiple results related among each other and guided by a common goal: the construction and operation of the STS demonstrator. In this context, an important milestone was achieved by the assembly of the first STS modules. For the module assembly, it was required to develop and test a rigorous QA procedure to ensure the proper operation of the STS-XYTERv2 ASIC. A dedicated setup was built based on a custom designed pogo-pin station and a total of 339 chips were tested. Results are considered satisfactory, yielding more than 90% of good-quality and operational ASICs.

Two flavors of the FEB-8 were developed and integrated with the module components. They were successfully operated in a C-ROB based readout chain. Four detector modules, based on the STS-XYTERv2 ASIC, were built and tested for the assembly of Station 0 of mSTS. As the first produced modules, invaluable lessons in the assembly, QA testing and final operation were learned. From the typical performance tests, broken channels, overall noise levels, threshold spread and gain uniformity were determined for each individual module.

The installation and operation of mSTS during the first data taking beam campaign allowed to look into the system performance. During operation multiple ASICs failed, probably as a consequence of thermal expansion of the protective glue, causing the breaking of ASIC bonds. The exact reason for the failures are being carefully investigated. The completion of Station 0 was achieved after replacing the right-orientation half-ladder with a new one. New modules were built using the recently produced STS-XYTERv2.1 ASIC. mSTS resulted in a good environment for checking the corrections implemented in the new version of the ASIC. Preliminary results such as time-walk spectra and charge distributions for 1 strip-clusters were presented and discussed. In addition, another important achievement was the operation of mSTS in a common, high-speed, free-streaming readout chain using products of Ag+Au collisions at interaction rates up to 40 MHz.

In the upcoming months, mSTS will be entirely rebuilt, having in total two operative stations as initially conceived. This poses significant challenges from the integration and operation point of view. A second station, with the powering and cooling services, needs also to be integrated in a limited space. In addition, more than 200 ASICs are expected to be operational, which implies that the full system must be ready to handle 10 GB/s during a stable operation.

Conclusions and Outlook

The challenging design of the CBM experiment, its unprecedented interaction rate and novel free-streaming readout concept, imposes strong constraints in the core tracking detector and its components. The STS custom-designed front-end electronics are based on the STS-XYTER ASIC, a low power, self-triggered chip optimized for amplitude and time measurements in a heavy irradiated environment. This thesis work was devoted to testing and characterization of the STS front-end electronics, its integration with the readout chain and detector components, and its commissioning within dedicated beam experiments.

The operation of the STS-XYTERv2 ASIC within a prototype readout chain was one of the major steps accomplished. A set of procedures and software tools, used in the ASIC characterization, was implemented as part of the standard operation package of the chip. Among the different tested functionalities, the development of procedures for time and amplitude calibration were of major importance. The performance of the calibration algorithms relies on the internal pulse generator, therefore an underlying constraint in the running time is the number of write/read actions. To improve these results towards the series production, the procedure should be implemented using an external generator and a dedicated ADC calibration pad.

The studies on the ASIC noise showed a pronounced discrepancy between even and odd channels. This issue was associated to differences in the biasing scheme of the charge sensitive amplifier and was corrected in the new revision (v2.1) of the chip. An extensive investigation was also carried out to check the dependency of the ASIC's noise on different parameters such as: temperature, slow-shaper peaking time, protective glue, load capacitance and linear regulators used in the final powering stage of the FEBs. From the results, the following conclusions could be highlighted:

- for the small measured range of temperatures (-15°C to 24°C), the noise dependence is linear with a coefficient of approximately 2 ENC(e^-)/°C;
- the ENC(e^-) increases linearly with the input capacitance with a slope of 27.4 ENC(e^-)/pF for both polarities. This value is larger than the one predicted by simulations;
- different filling materials used in the assembly procedure to protect the TAB and wire-bonds in the ASIC were tested regarding their influence on the noise levels. The best results were obtained for Polytec UV2257 and Dymax 9008. Other tests such as radiation tolerance and thermal behavior are mandatory to choose a final candidate;
- the custom-designed power regulators LTChandigarh to be used in the final system, showed good noise performance.

The radiation hard architecture of the STS-XYTERv2 ASIC was tested for SEU in a dedicated high intensity proton beam line. The irradiation was carried out with 1.7 GeV/c protons from the COSY accelerator facility in Research Center Jülich, Germany. The study verified the improvement on the DICE cell architecture with respect to the previous ASIC design. The SEU cross section for DICE cells was measured, resulting in $9.26 \pm 0.98 \cdot 10^{-16}$ cm^2/bit; this value is consistent with

literature. The SEU rate in the STS detector under SIS100 conditions was estimated based on FLUKA calculations of the radiation environment, and the measured cross section. The predicted value of less than 1 SEU/ASIC/day, represents a good result for the STS performance.

Other ASIC irradiation campaigns at the VECC Kolkata (India) and the Nuclear Physics Institute in Krakow (Poland), shed lights on the degradation of the chip functionalities with the dose. Results indicated an increment of 40%–60% in the ASIC's noise at cumulated doses up to the lifetime of the front-end electronics in most critical STS station. Small annealing periods at room temperatures could also help restoring the chip performance.

The integration of the STS-XYTERv2 ASIC with the silicon sensors led to the production of the first STS prototype modules with a single FEB-B and 128 readout channels per side. The performance was studied with 1.7 GeV/c protons at COSY. The campaign brought valuable insights to the development of an effective ground and powering scheme for reading out the detectors. Two detector modules were used to measure the system time resolution and to characterize the signal amplitude distribution for different thresholds and beam incident angles. The overall system noise was determined as a function of the sensor reverse bias voltage, resulting in levels of approximately 1200 ENC(e^-). Signal-to-noise ratios, evaluated for 1 strip-cluster signals, are above 15 for both polarities. A deeper analysis into the collected data, allowed to identify a logic error in the ASIC that affects the readout rate and quality of the data. This issue was eradicated in the revision 2.1 of the chip.

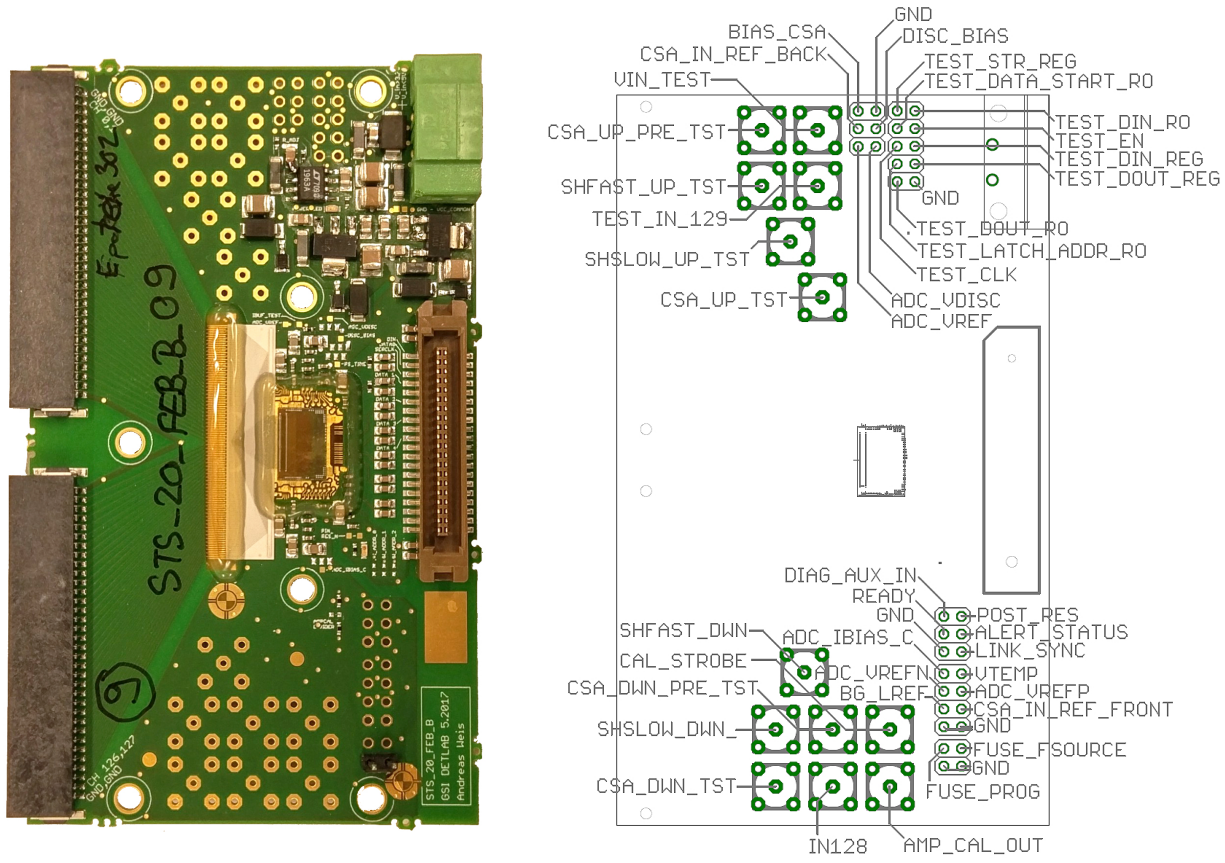
Guided by a common effort, the development of the STS demonstrator (mSTS) for the activities of the CBM Phase 0 was an important achievement. For testing the STS-XYTERv2 ASICs, to be used in the assembly of the detector modules, a test setup based on a custom-designed pogo-pin socket was built. The test setup was successfully integrated into the prototype readout chain and a QA protocol for ASIC testing was developed. The procedure was extended for the measurements of ASIC bonded to microcables in order to identify broken or unconnected channels.

The operation of a close-to-final readout chain supported the measurements of the first STS modules. Typical performance tests made possible to evaluate the overall noise level, number of broken channels and other operating parameters. mSTS detector was operated during the first beam campaign of the mCBM experiment. Valuable data from Ag+Au collisions at 1.58 AGeV and different interaction rates, up to 10^6, were collected.

The value of this work relies not only in the obtained results but also in the gained experience in constructing and operating the modules with the STS-XYTER ASIC based readout chain. Important progress was achieved by developing techniques and tools for characterization of the front-end electronics and the complete detector system. They will be applied for quality assurance of the components during the series production.

Appendix A

The prototype FEB-B



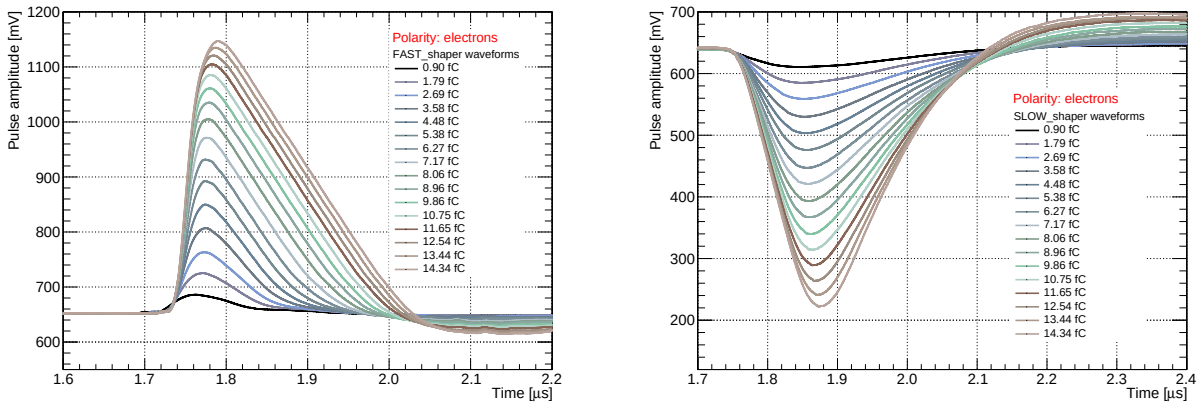
(a) *Prototype FEB-B fully equipped.* (b) *Schematics of main signals in the FEB-B.*

Figure A.1: *Photo and schematics of the prototype FEB-B used for testing the STS-XYTERv2. Two ERNI connectors are used for interfacing up to 128 channels in the detectors with the chip. Clock, down-link and 5 up-links LVDS signals are transmitted via the KEL40 that connects the ASIC to the other components of the readout chain. The FEB-B is fabricated with comercial components including the linear regulators.*

Appendix B

Waveforms of the STS-XYTERv2 shapers in electron polarity

Part of the initial characterization procedure of the STS-XYTERv2 is the acquisition of the shapers waveforms and estimation of the gain for holes and electrons polarities. Complementary to the results shown in Chapter 3 subsection 3.6.1, Fig. B.1 illustrates exemplary waveforms acquired from a test channel in the STS-XYTERv2. Charge pulses are injected at the input of the CSA using the internal calibration pulse and the shaper's response are monitored using a Tektronik oscilloscope.



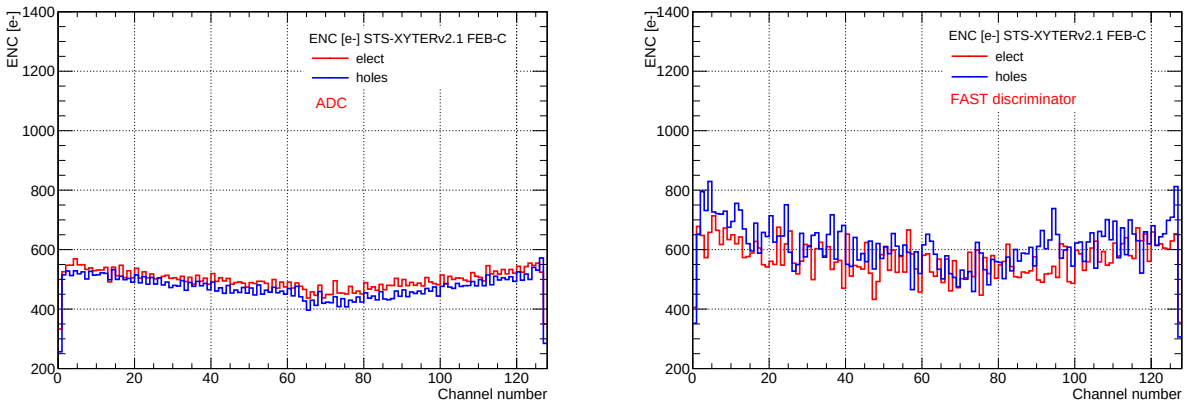
(a) *Fast shaper waveforms.* (b) *Slow shaper waveforms.*

Figure B.1: *Waveforms of the STS-XYTERv2 ASIC shapers measured for electrons polarity.*

Appendix C

Measurements of noise levels for the STS-XYTERv2.1

The revision v2.1 of the STS-XYTER implements several changes with respect to its predecessor. Some of the most important modifications are meant to correct the problem uncovered during the testing phase of the STS-XTERv2; while others extend the monitoring functionalities of the chip. The difference among odd and even channels was one of the main problems identified. Figure C.1 illustrates the noise levels measured in the new revision of the ASIC, where no significant discrepancies are observed.



(a) *ADC noise levels.* (b) *Fast discriminator noise levels.*

Figure C.1: *STS-XYTERv2.1 noise levels measured for the ADC and fast discriminator in both polarities.*

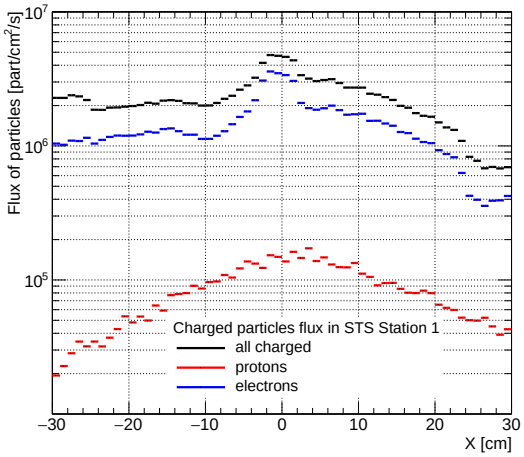
Appendix D

Charged particles flux at STS Station 1

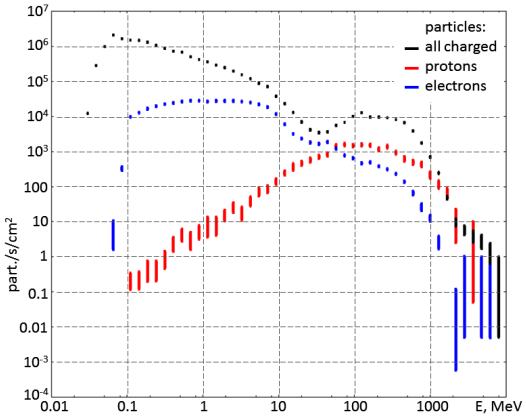
Although out of the physics acceptance, the STS front-end electronics will exposed to high irradiation doses. To estimate the flux of charged particles and TID at which the electronics components will be exposed during the operation lifetime (10 months), realistic FLUKA simulations are used [137]. The parameters considered in the simulation are listed below:

- CBM-MUCH configuration (largest backscattering effect due to the first muon absorber);
- Beam with intensity 10^9 Au ions/s interacting in 1% Au target;
- 10 months of continuous operation;

The flux of charged particles with E $\geqslant$ 20 MeV crossing the front-electronics area of the STS Station 1 is shown in Fig. D.1a. The total flux is mostly dominated by the electron's contribution. Figure D.1b illustrates the energy spectra of charged particles passing through the highest irradiated place on the location of the front-end electronics.



(a) *Flux of charged particles per species crossing the electronics place.*



(b) *Energy spectra at the front-end electronics placed on coordinates X:[-10,0] cm and Y:[15,25] cm.*

Figure D.1: *Flux and energy distributions of charged particles on the electronics place of STS Station 1.*

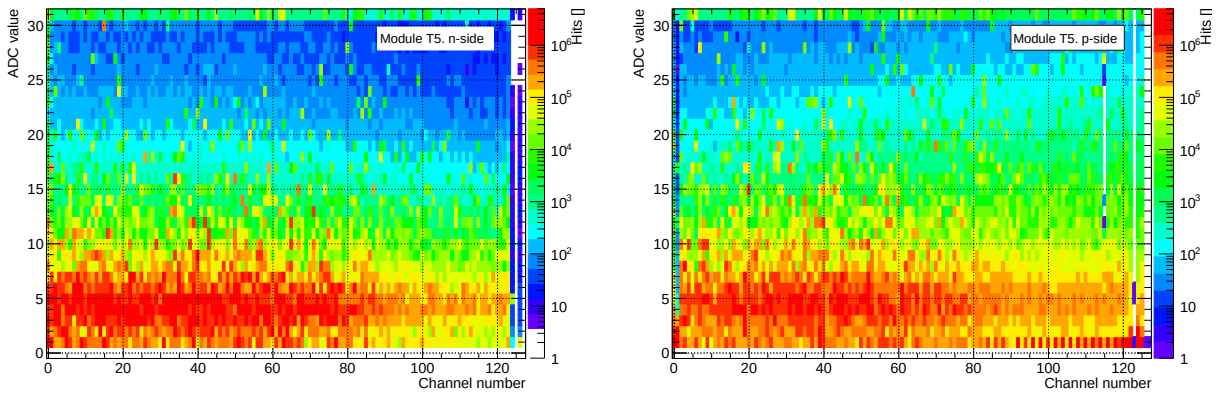
Appendix E

Performance of prototype module T5

The module T5 was one of the first STS prototype module used to study the signal readout with the STS-XYTERv2 ASIC. It was built using the FEBs-B, therefore, it was possible to read only 128 channels per side. Tests were conducted in a relativistic proton line of 1.7 GeV/c momentum from the COSY accelerator facility in Research Center Jülich, Germany.

Complementary to the results discussed in Chapter 5 for module T3, this Appendix aims to illustrate the performance of module T5. Figure E.1 shows the ADC distribution of the signal before being combined into clusters. The data have been filtered to reduce the effect of double pulses created by a logic error in the ASIC.

The cluster amplitude spectra from module T5 are shown in Fig. E.2 after applying the clustering algorithm which include timing and geometrical requirements. The reconstruction yields mostly 1-strip cluster, as shown in the cluster size distribution, see Fig. E.3. Signals from 1-strip cluster for *p* and *n-side* are fitted using a convolution between Landau and Gaussian function.



(a) *Raw ADC distribution for n-side.* (b) *Raw ADC distribution for p-side.*

Figure E.1: *Raw ADC distributions of module T5.*

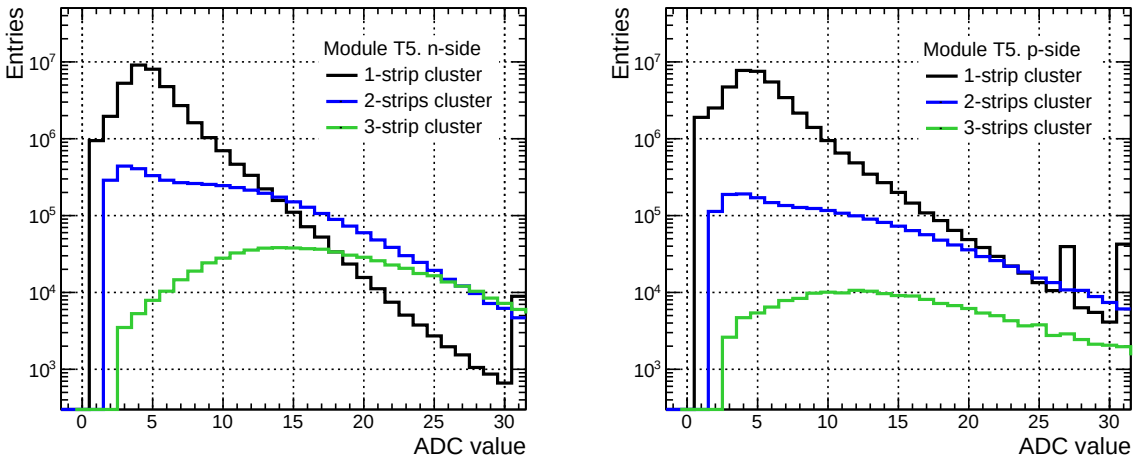


Figure E.2: *Spectra of the total cluster amplitude, taken from module T5 at* $V_{bias} = 160$ *V.*

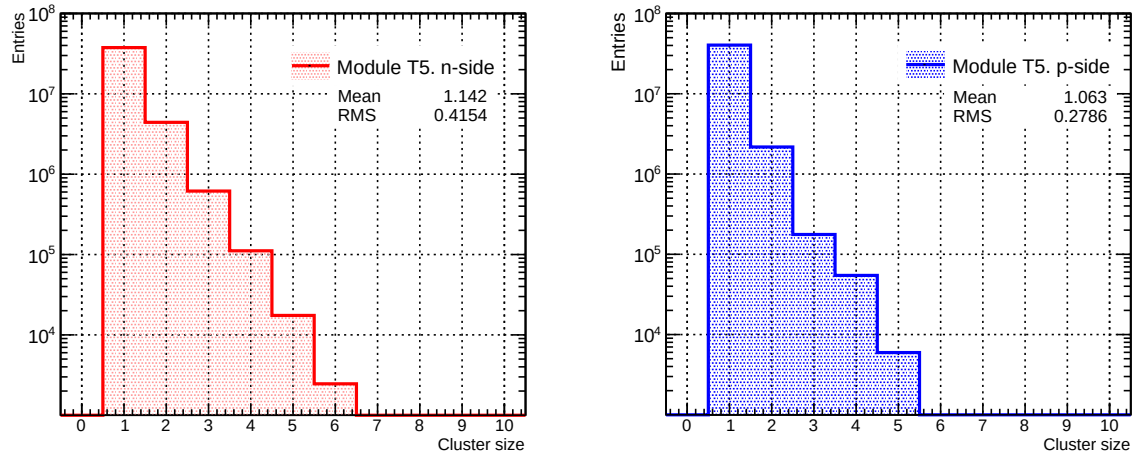


Figure E.3: *Cluster size distribution for protons inciding perpendicular to the sensor area of module T5.*

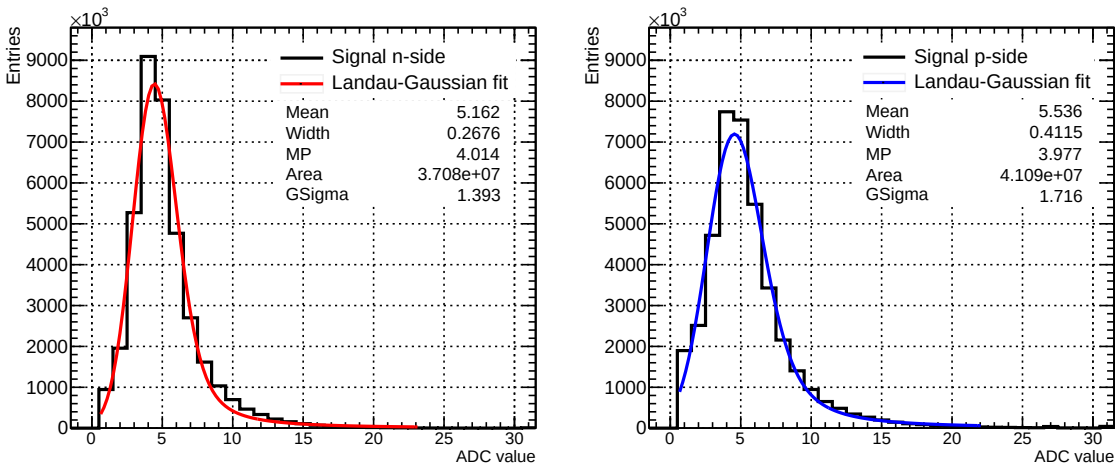


Figure E.4: *Spectra of 1 strip-cluster amplitude from module T5.* ***Left:*** *n-side.* ***Right:*** *p-side.*

List of Acronyms

A	
ADC	Analog-to-Digital COnverter
AFCK	AMC FMC carrier Kintex
AFE	Analog Front-end
ALICE	A Large Ion Collider Experiment
APPA	Atomic Physics, Plasma and Applications
ASIC	Application Specific Integrated Circuit
B	
BELLE II	High energy experiment at the High Energy Accelerator Research Organization (KEKB), Japan
BES	Beam Energy Scan
BM@N	Baryonic Matter at Nuclotron
C	
CBM	Compressed Baryonic Matter
CCE	Charge Collection Efficiency
CFD	Constant Fraction Discriminator
CiS	Forschungsinstitut für Mikrosensorik GmbH
CMOS	Complementary MOS
CRI	Common Readout Interface
D	
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition System
DCS	Detector Control System
DICE	Dual Interlocked Cell
DNL	Differential Non-Linearity
DPB	Data Processing Board
E	
ECAL	Electromagnetic Calorimeter
ELT	Enclosed Layout Transistor
ENC	Equivalent Noise Charge
EoS	Equation of State
ESD	Electrostatic Discharge

F

FAIR	Facility for Antiprotons and Ions Research
FEB	Front-end Board
FEE	Front-end Electronics
FIFO	Electronic circuits for buffering and flow control
FLES	First Level Event Selector
FPGA	Field Programmable Gate Array
FWHM	Full Width Half Maximum

G

GBT	Gigabit Transceiver
GEM	Gas Electron-Multiplier
GSI	Gesellschaft für Schwerionenforschung GmbH

H

HADES	High Acceptance Di-Electron Spectrometer

I

IC	Integrated Circuit
ICh	Ionization Chamber
INL	Integral Non-Linearity
IPBus	IP-based protocol for controlling hardware devices

J

JINR	Joint Institute for Nuclear Research

L

LDO	Low Dropout regulator
LET	Linear Energy Transfer
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LSB	Least Significant Bit
LVDS	Low Voltage Digital Signal

M

MAPMT	Multi Anode Photomultiplier
MAPS	Monolithic Active Pixels
mCBM	mini CBM experiment
MIP	Minimum Ionizing Particles
MOS	Metal Oxide Semiconductor
MPD	Multi-Purpose Detector
MPV	Most Probable Value
MRPC	Multi-gap Resistive Plate Chambers
mSTS	mini STS
MUCH	Muon Chambers
MVD	Micro Vertex Detector
MWPC	Multi-Wire Proportional Chambers

N

NA61/SHINE	North Area 61/The SPS Heavy Ion and Neutrino Experiment
NICA	Nuclotron-based Ion Collider fAcility
NIEL	Non-Ionizing Energy Loss
NuSTAR	Nuclear STructure, Astrophysics and Reactions

P

PADI	Pre-Amplifier DIscriminator
PANDA	anti-Proton ANihilation at DArmstadt
PCB	Printed Circuit Board
POB	Power Board
PSD	Particle Spectator Detector

Q

QCD	Quantum Chromodynamics
QGP	Quark Gluon Plasma
QGSM	Quark Gluon String Model

R

RHIC	Relativistic Heavy Ion Collider
RICH	Ring Imaging Cherenkov Detector
ROB	Readout Board
RPC	Resistive Plate Chambers

S

SCA	Slow Control ASIC
SEE	Single Event Effect
SEU	Single Event Upset
SIS	Schwerionensynchrotron
SNR	Signal-to-Noise Ratio
SPADIC	Self-triggered Pulse Amplification and Digitization asIC
SPS	Super Proton Synchrotron
STS	Silicon Tracking System
STS-XYTER	STS, X,Y coordinate, Time and Energy Resolution ASIC

T

TAB	Tape Automated Bonded
TFC	Timing and Fast Control
Thr2_glb	Absolute Threshold of the FAST discriminator
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
ToF	Time of Flight
TRD	Transition Radiation Detector
TSS	Time Synchronization System

U

UrQMD Ultra-relativistic Quantum Molecular Dynamics

V

VRef_P Positive Reference Voltage of the ADC

VRef_N Negative Reference Voltage of the ADC

VRef_T Absolute Threshold for the ADC

VTemp Reference PAD for monitoring the temperature of the ASIC

Zusammenfassung

Das CBM-Experiment plant eines der führenden und am weitesten gefächerten Forschungsprogramme auf dem Gebiet der Schwerionenphysik. Sein Ziel ist die Untersuchung des Phasendiagram stark wechselwirkender Materie in der Region hoher Baryonendichten und moderater Temperaturen unter Verwendung hochenergetischer Kern-Kern-Kollisionen [11].

CBM wird zur Zeit gebaut als einer der vier wisscenschaftlichen Pfeiler der zukünftigen FAIR - Forschunganlage in Darmstadt [30]. Der experimentelle Aufbau ist ein Fixed - Target Vorwärtsspektrometer, entworfen als ein Vielzweckdetektor mit der Fähigkeit Hadronen, Elektronen und Myonen in p+p, p+A and A+A Kollisionen über den gesamten Strahlenergiebereich von FAIR zu messen. Um hinreichend Statistik zu sammeln, ist das gesamte Experiment auf den Betrieb bei sehr hohen Wechselwirkungsraten (bis zu 10 MHz) ausgelegt und übersteigt damit die Ratenfähigkeit existierender Schwerionenexperimente um mehrere Grössenordnungen [31, 64]. Da die meisten Observablen komplexe Triggertopologien aufweisen, wird das Experiment eine neuartige frei strömende ("free-streaming") Auslese verwenden. Datenworte mit individueller Zeitinformation werden von allen CBM-Detektoren zu einer Computing-Farm gesendet, wo in Echtzeit Spurrekonstruktion, Ereigniszusammenstellung und die Analyse im Hinblick auf Triggersignaturen durchgeführt werden.

Die erwartete Datenrate für das gesamte Experiment liegt bei ca. 2 TB/s in Au+Au-Kollisionen. Da solche Datenmengen nicht mit vertretbarem Aufwand für eine spätere Analyse gespeichert werden können, werden schnelle Algorithmen zur Echtzeit-Rekonstruktion und Ereignisselektion die Anzahl zu speichernder Ereignisse um 2 Grössenordnungen reduzieren.

Das Silicon Tracking System

Das Silicon Tracking System (STS) ist der zentrale Detektor zur Spurrekonstruktion und Impulsbestimmung geladener Teilchen im CBM-Experiment. STS ist in der Lage, die Spuren von bis zu 700 Teilchen in Au+Au Kollisionen bei Ereignisraten bis zu 10 MHz zu messen, kann in einem 1 Tm Dipol-Magnetfeld eine Impulsauflösung besser als 2% erzielen, sowie komplexe Zerfallstopologien, z.B. mit seltsamen Teilchen, identifizieren.

Der STS erstreckt sich von 30 cm bis zu 100 cm hinter dem Target, und wird in der Apertur eines supraleitenden Dipolmagneten installiert. Er besteht aus 8 Ebenen (sog. Stationen) zur Spurerkennung, bestehend aus doppelseitigen Silizium-Streifen-Sensoren. Zwei Millionen Kanäle werden mit selbstgetriggerter Elektronik ausgelesen, kompatibel mit dem Datenauslese und Echtzeit-Ereignisanalyse-Konzept, das im gesamten Experiment angewandt wird. Die funktionelle Einheit des STS-Detektors ist das sogenannte "Modul", bestehend aus einem Silizium-Sensor, Auslesekabeln und zwei Frontend-Elektronik-Boards.

Module werden auf Kohlefaserleitern montiert, die ihrerseits auf den mechanischen Montagerahmen installiert werden.Die Mikrostreifen-Sensoren erlauben eine zweiseitige Segmentierung mit einem Streifenabstand von 58 μm und einem Stereowinkel von 7.5 Grad, haben eine integrierte AC-Signalkopplung und die unter 7.5 Grad verlaufenden Streifen zusätzliche Verbindungslinien auf einer zweiten Metall-Lage. Um das Materialbudget im aktiven Detektorvolumen zu minimieren,

wird die gesamte Elektronik in der Peripherie der Stationen installiert. Detektorsignale werden mit Hilfe von Mikrokabeln zur Frontend-Elektronik geleitet. Die STS-Frontend-Elektronik verwendet den STS-XYTER ("STS X and Y coordinate, Time and Energy Read-out chip") ASIC. Dieser dediziert für CBM-STS entwickelte ASIC implementiert die analoge Elektronik (Verstärker, Shaper), die Digitalisierung sowie die Erzeugung individueller Datenworte für jedes Signal.

Strahlungstoleranz ist ein wichtiges Qualitätsmerkmal der Silizium-Streifen-Sensoren, wenn man die harschen Strahlungsbedingungen in der STS-Umgebung betrachtet. Die zentralen Sensoren des STS müssen über den kompletten Lebenszyklus des Experiments voraussichtlich ein NIEL von bis zu 10^{13} 1 MeV $n_{eq}cm^{-2}$ und eine ionisierende Dosis von ca. 1.1 Mrad aushalten.

Motivation dieser Arbeit

Das neuartige frei strömende Auslesekonzept für das CBM-Experiment erfordert schnelle, selbsttriggernde Elektronik sowie schnelle Daten-Vorverarbeitung und Datenaufnahme.Der STS-XYTER ist ein kompakter analog-digitaler ASIC (Application Specific Integrated Circuit), der diverse Funktionalität für die Auslese von Silizium-Sensoren implementiert und optimiert. Vor der Integration des ASIC mit den Komponenten des Streifen-Sensors war die Charakterisierung des Chips von essentieller Bedeutung.Diese erforderte die Entwicklung von Software-Werkzeugen und Methoden zur Evaluierung der analogen Frontend-Funktionalität, der gesamten Signalverarbeitungskette sowie zur Kalibrierung der Schaltkreise für die Messungen von Zeit and Amplitude. Abschätzungen des ASIC-Rauschens und dessen Abhängigkeit von Systemparametern wie z.B. Temperatur oder Eingangskapazität sind von grosser Bedeutung, da das Rauschen eines der wichtigsten Designkriterien gerade für ein selbsttriggerndes System sind(aufgrund die resultierenden Rausch-Hits). Zur Vorbereitung der Vorserien- und Serienfertigung von Modulen waren auch die Entwicklung und das Testen von Techniken und Werkzeugen zur Qualitätssicherung der ASICs nötig.

Die hohe Strahlungsbelastung im CBM-Experiment beeinflusst nicht nur Sensoreigenschaften, sondern auch den Betrieb der Frontend- und Ausleseelektronik. Daher wurde eine detaillierte Evaluierung der strahlenharten Architektur des STS-XYTERv2 im Hinblick auf Toleranz gegenüber Upset-Fehlern (Single Event Upsets - SEU) sowie der ASIC-Eigenschaften nach Bestrahlung mit einer Lebensdosis durchgeführt.

Wichtige Meilensteine für den STS sind auch der Zusammenbau der kompletten Detektormodule sowie deren Betrieb mit der vollständigen Auslesekette in verschiedenen Datennahme-Szenarien. Die Ergebnisse der ASIC-Charakterisierung sowie die Verfügbarkeit des Frontend-Boards mit 8 ASICS (FEB-8) und der Auslesekette erlaubten die Integration weitgehend finaler Komponenten in die STS-Module. Die während der ASIC-Charakterisierung etablierten Methoden und Werkzeuge wurden in den Systemtests nicht nur genutzt, sondern erforderten auch Erweiterungen und Optimierungen für die Verwendung in den grösseren Systemen mit jeweils 16 ASICs pro Modul. Diese Modul-Studien erbrachten wertvolle Erfahrungen für diverse Aspekte der STS-Systemintegration wie Techniken zur Rausch-Minderung oder die Entwicklung eines Systems für Spannungsversorgung und Erdung.

Charakterisierung des STS-XYTERv2 ASIC und Entwicklung von Kalibrierungs - Prozeduren

Die Charakterisierung der STS Frontend-Elektronik ist eine komplexe Prozedur und einer der wichtigsten Schritte der ASIC-Inbetriebnahme vor der Integration mit Detektor und Auslese. Für Betrieb und Test des STSXYTERv2 ASIC wurde eine Prototyp-Auslesekette eingerichtet. Die Hardware-Plattform, die das Backend der ASIC-Auslese implementiert, basiert auf dem AFCK-Board [75], der in ganz CBM genutzten Entwicklungs- und Prototyp-Plattform für das CBM Datenverbeitungsboard (data processing board - DPB). Dieses System erlaubt neben dem Testen

der Chip-Funktionalität auch Entwicklung und Test des speziell für den STS_XYTER entwickelten Kommunikationsprotokolls. [92]. Ein Satz von Prozeduren und Software-Werkzeugen wurde als Teil des Standard-Software-Pakets des ASICs entwickelt und implementiert.

Im Fokus der getesteten Funktionalitäten stand die Entwicklung der Prozeduren zur Zeit- und Amplitudenkalibration, siehe Kapitel 3 Sektion 3.7. Diese Prozeduren beinhalten die korrekte Konfiguration diverser ASIC-Register und -Funktionalitäten. Ziel ist die Ermittlung individueller Korrekturwerte für die Diskriminatoren von ADC und Zeitbestimmung in jedem einzelnen Kanal. Da der Chip separate Verarbeitungspfade für Energie- und Zeitmessung implementiert, muss die Kalibration nicht nur die Linearität des ADC sicherstellen, sondern unabhängig davon auch die gleichförmige Zeitantwort in allen Kanälen. Die wichtigsten Aspekte der Kalibration können wie folgt zusammengefasst werden:

- Die Kalibration wurde mit dem internen Pulsgenerator durchgeführt, was das Testen des kompletten ASIC-internen Signalverarbeitungs-Pfades ermöglicht. Der interne Pulsgenerator zeigt gute Linearität im erwarteten Signalbereich bis ca. 14.5 fC;
- Die Kalibration basiert auf der Messung der Antwortfunktion aller Diskriminatoren in jedem Kanal. Diese Prozedur wird als *S-Kurven* Scan bezeichnet. Ergebnis der Kalibrationsprozedur ist eine Matrix mit 128×32 Korrekturwerten;
- Die Genauigkeit der Kalibration wurde evaluiert als Funktion der Zahl injizierter Testpulse. Verlässliche Kalibrationsresultate wurden erzielt bei Verwendung von mindestens 50 Pulsen für die ADC-Kalibration und 100 Pulsen in der Kalibration des schnellen Zeit-Zweiges. Dies entspricht mit der gegenwärtigen Firmware und Kontrollsoftware einer Kalibrationsdauer von 360 s pro ASIC;
- mehr als 98% dieser Zeit werden durch Schreib- und Leseoperationen verbraucht, die durch die Geschwindigkeit des Kontroll-Protokolls limitiert sind, das momentan auf dem IPBus-Kommunikations-Protokoll basiert;
- Genauigkeit und Wiederholbarkeit der internen Kalibrationen wurden sowohl mit Hilfe eines externen Pulsgenerators wie auch mit einer radioaktiven Gamma-Quelle verifiziert. Daneben wurde die Stabilität der Kalibrationsparameter in einem Langzeit-Test verifiziert.

Da die Kalibration den über Software-Kommandos kontrollierten internen Pulsgenerator verwendet, ist die Geschwindigkeit der Kaibrationsprozedur durch die Anzahl der Schreib-/Lese-Operationen limitiert. Dies kann in den Testprozeduren der zukünftigen Serienfertigung durch Verwendung eines externen Pulsgenerators und des dedizierten ADC-Kalibrations-Pads des ASICs optimiert werden.

Evaluierung des STS-XYTERv2 ASIC-Rauschens

Untersuchungen des ASIC-Rauschens zeigten eine ausgeprägte Diskrepanz zwischen geraden und ungeraden Kanalnummern. Dieser Effekt konnte auf Unterschiede im Biasing-Schema des ladungsempfindlichen Verstärker für die geraden bzw. ungeraden Kanäle zurückgeführt werden. Diese Diskrepanz konnte in der neuen Version (v2.1) des Chips korrigiert werden.

Die Abhängigkeit des ASIC-Rauschens von verschiedenen Parametern wie Temperatur, Peaking-Zeit des langsamen Shapers, ASIC-Schutzmaterialien, Eingangskapazität der Kanäle sowie Typ des zur Spannungsversorgung auf dem FEB verwendeten Linearreglers, wurde untersucht, siehe Kapitel 3 Sektion 3.9. Als Ergebnis dieser Untersuchungen können die folgenden Schlussfolgerungen hervorgehoben werden:

- für den untersuchten Temperaturbereich von (-15°C bis 24°C) erhöht sich das Rauschen linear mit einer Steigung von ca. 2 ENC(e^-)/°C;
- Der ENC(e^-) erhöht sich linear mit der Eingangskapazität mit einer Steigung von 27.4 ENC(e^-)/pF für beide Signalpolaritäten. Diese Steigung ist grösser als in Simulationen vorhergesagt;
- Verschiedene Füllmaterialien, die während des Modulbaus als Schutz für die TAB- und Draht-Bonds des ASIC verwendet werden, wurden hinsichtlich ihres Einflusses auf das Rauschen untersucht. Die besten Resutate wurden erzielt für die Materialien Polytec UV2257 und Dymax 9008. Andere Tests wie Strahlungstoleranz und thermisches Verhalten sind erforderlich, um letztlich einen geeigneten Material-Kandidaten auszuwählen;
- der speziell für CBM entwickelte Spannungsregler (LTChandigarh) zeigte ein gutes Rausch-Verhalten.

Evaluierung des strahlenharten Design des STS-XYTERv2

Die strahlenharte Architektur des STS-XYTERv2 ASIC wurde im Hinblick auf SEU in einer dedizierten Strahlzeit mit einem hochenergetischen Protonenstrahl getestet. Die Bestrahlung wurde mit 1.7 GeV/c Protonen des COSY-Beschleunigers am Forschungszentrum Jülich, Deutschland, durchgeführt. Diese Studie konnte die Verbesserung der DICE-Zellen-Architektur verglichen mit der vorherigen ASIC-Version verifizieren. Die Verteilung der SEU innerhalb der 8-Bit eines Konfigurations - Registers zeigte ein spezifisches Muster, in dem die ersten 4 Bits eine höhere Rate an SEU-Fehlern aufweisen. Dieser Effekt ist korreliert mit einer Asymmetrie in den Potentialverbindungen zu den Guard-Ringen im ASIC-Layout, siehe Kapitel 4 Sektion 4.4.

Der SEU-Wirkungsquerschnitt für DICE-Zellen wurde mit $9.26 \pm 0.98 \cdot 10^{-16}$ cm^2/bit gemessen; dieser Wert ist zwei Grössenordnungen kleiner als für reguläre*flip-flops* und konsistent mit Literaturwerten, siehe Kapitel 4 Sektion 4.4.1. Die erwartete SEU-Rate im kompletten STS-Detektor, betrieben am SIS100, wurde auf Grundlage von FLUKA-Berechnungen der Strahlungsumgebung sowie mit Hilfe der gemessenen Wirkungsquerschnitte abgeschätzt. Die Simulationen wurden für ein experimentelles Szenario mit höchsten Strahlintensitäten und Wechselwirkungsraten durchgeführt. Die vohergesagten Werte zeigen eine starke Abhängigkeit von der Chip-Position relativ zur Strahlachse sowie dem Abstand zum Target. Die resultierenden Raten von weniger als 1 SEU/ASIC/Tag zeigen die Eignung des gewählten DICE-Ansatzes zur Reduktion von SEUs, siehe Kapitel 4 Sektion 4.4.2.

Weitere ASIC-Bestrahlungen wurden am VECC Kolkata, Indien sowie am Nuclear Physics Institute in Krakau, Polen, durchgeführt, siehe Kapitel 4 Sektion 4.5. Zwei unterschiedliche Fragestellungen wurden in diesen Studien untersucht. Zuerst wurden der Anstieg des ASIC-Rauschens und die Veränderung des ADC-Gain als Funktion der Gesamtdosis systematisch untersucht. Die Ergebnisse zeigen einen Anstieg des ASIC-Rauschens um 40%–60% bei Dosen, die der Bestrahlung von ASICs an den exponiertesten Stellen der 1. STS-Station über die volle CBM-Lebensdauer hinweg entsprechen. Dareuberhinaus wurde der STS-XYTERv2 ASIC über nur 2 Stunden hinweg einer totalen ionisierenden Dosis von 400 krad ausgesetzt, was zu einem Anstieg des Rauschens um 40% führte. Der positive Effekt einer kurzen Ausheilungs-(Annealing)-Periode bei Zimmertemperatur wurde beobachtet, der Rausch-Anstieg verglichen mit der Situation vor Bestrahlung reduzierte sich auf 20%. Die Ergebnisse der Bestrahlungen zeigen insgesamt, dass das strahlenharte Design des Chips hinreichend robust and SEU-tolerant bei den in CBM erwarteten Dosen ist. Dies ist ein wichtiges Kriterium für den Betrieb im STS-Detektor.

Test von Prototyp-STS-Modulen mit einem relativistischen Protonenstrahl

Ein wesentlicher Schritt auf dem Weg zum finalen STS ist der Test der ersten Prototyp-Module zusammen mit der dedizierten Ausleseelektonik und Datenaufnahme. Diese Prototyp-Module lesen nur einen Teil eines Sensor aus. Pro Sensorseite werden 128 von 1024 Streifen mit einem einzelnen STS-XYTERv2 ASIC auf einem Prototyp-FEB-B ausgelesen. Das Verhalten dieses Systems wurde mit einem relativistischen Protonenstrahl (1.7 GeV/c) am COSY-Beschleuniger untersucht. Diese Tests ermöglichten die Untersuchung des Sensorverhaltens und seiner Eigenschaften wie Signal-Amplitude und Rauschen, aber auch die Evaluierung der ASIC-Performance bei der Auslese des Silizium-Sensors. Darüberhinaus war dieses System auch eine fundamentale Plattform für die Weiterentwicklungen des Datenaufnahmesystem.

Die Strahlkampagne brachte daneben wertvolle Erkenntnisse für die Entwicklung eines praktikablen Systems für Spannungsversorgung und Erdung. Um die gleichzeitige Auslese beider Detektorseiten zu ermöglichen, war es nötig, die Potentiale der beiden FEBs mittels eines Kondensators (Kapazität grösser 100 nF) zu verbinden, um den Signalpfad zu schliessen; siehe Kapitel 5 Sektion 5.1.1. Die Zeitkorrelation zwischen Hits in den STS-Modulen und den Signalen eines Referenz-Hodoskops wurde gemessen. Dies erlaubt die Abschätzung einer Obergrenze für die Zeitauflösung des ASIC, die gut mit den erwarteten Werten übereinstimmt (unter 5 ns für Signale mit grosser Amplitude). Die Module wurden auch genutzt, um die räumliche Korrelation zwischen Hits auf der *n-* und *p-Seite* des Detektors zu untersuchen und um das Ladungsspektrum für verschiedene Siganlschwellen und Einfallswinkel des Strahls zu charakterisieren.

Das Gesamt-Rauschen des System wurde bestimmt als Funktion des Sperrspannung, mit Werten von ca. 1200 ENC(e^-). Das Verhältnis von Signal zu Untergrund, gemessen mit Hilfe von 1-Streifen-Clustern, war grösser als 15 für beide Polaritäten, siehe Kapitel 5 Sektion 5.6.

Zusammenbau von STS-Modulen für CBM Phase 0

Als Teil der Aktivitäten von CBM in FAIR Phase 0 wurde ein Prototyp des STS-Detektor namens mini-STS (mSTS) gebaut. Die Konstruktion des mSTS wurde möglich durch zwei wesentliche Fortschritte im STS-Projekt: die Entwicklung des FEB-8 Frontend-Boards zur Auslese einer vollständigen Sensor-Seite, sowie der Betrieb einer C-ROB basierten Auslesekette. Der vollständige mSTS besteht aus zwei kleinen Stationen zur Spurerkennung, gebaut aus Prototyp-Elementen (Modulen, Leitern) des STS-Detektors. Im mSTS-Design wurden diverse Vereinfachungen vorgenommen, um den Fokus auf essentielle Komponenten und Aspekte des System-Designs zu legen.

In einem ersten Schritt wurde die erste mSTS-Station mit 4 Modulen auf 2 Leitern aufgebaut. Die Produktion der 4 Module erforderte das Testen und die Charakterisierung einer grösseren Menge an ASICs. Für diesen Zweck wurde ein Testaufbau basierend auf einem speziell entworfenene Pogo-Pin-Sockel gebaut. Dieser Testaufbau wurde erfolgreich mit einer Prototyp-Auslesekette verbunden, und ein Protokoll zur Qualitätssicherung für das Testen der ASIC wurde entwickelt, siehe Kapitel 6 Sektion 6.3. Diese Prozedur wurde ausgeweitet auf die Messungen an den mit Mikrokabeln versehenenen ASICs, um defekte oder unverbundene Kanäle zu identifizieren.

Der Betrieb dieser ersten vollständigen Module ermöglichte die Durchführung von Messungen u.a. des Gesamt-Rausch-Verhaltens, ADC-Gain, Gleichförmigkeit der Schwellen über alle Kanäle, Anzahl defekter Kanäle und anderer Betriebsparameter, siehe Kapitel 6 Sektion 6.5.

Installation und Betrieb des mSTS wahrend der ersten Strahlzeit des mCBM-Experiments ermöglichten erste Eindrücke und Tests der Eigenschaften des Gesamtsystems. Die erste Station konnte vervollständigt werden, nachdem die Module einer der Leitern mit neu produzierten Modulen ersetzt wurden. Letztere wurden unter Verwendung der neu verfügbaren ASIC-Version STS-XYTERv2.1 gebaut. Hiermit ergab sich die Gelegenheit, die in der neuen ASiC-Version gemachten Änderungen zu überprüfen.

In Ag+Au-Kollisionen bei 1.58 AGeV und verschiedenen Wechselwirkungsraten bis zu 10^6 wurden mit mSTS Daten genommen. Erste Ergebnisse wie z.B. Time-Walk-Spektren und Ladungsverteilungen für 1-Streifen-Cluster wurden gezeigt und diskutiert, siehe Kapitel 6 Sektion 6.6. Ein weiterer wichtiger Erfolg in mCBM war der Betrieb des mSTS in einer gemeinsamen, schnellen Auslesekette bei Wechselwirkungsraten nahe den im CBM-Experiment erwarteten.

Der Wert dieser Arbeit liegt nicht nur in den erzielten Ergebnissen, sondern darüber hinaus in den Erfahrungen, die beim Bau und Betrieb der STS-Module mit der STS-XYTER-basierten Auslese gemacht wurden. Wichtige Fortschritte wurden erzielt durch die Entwicklung von Verfahren und Werkzeugen zur Charakterisierung der Frontend-Elektronik sowie des Detektor-Gesamtsystems. Diese werden für die Qualitaetssicherung von Komponenten waehrend der STS-Serienfertigung genutzt werden.

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