

# Organic Field-Effect Transistors with high- $\kappa$ Dielectric

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# Zusammenfassung

Diese Arbeit beschäftigt sich mit dem Einsatz von Dielektrika mit hoher Permeabilität, sogenannten high- $\kappa$ -Dielektrika, in organischen Dünnschichtfelddefekttransistoren. Dabei werden zwei interessante und aktive Forschungsfelder vereint, zum einen organische Halbleiter, und zum anderen high- $\kappa$ -Dielektrika. Organische Halbleiter, also Halbleiter, die aus Kohlenstoffverbindungen bestehen, gewinnen zunehmend an Bedeutung, insbesondere im Hinblick auf ihre technische Verwendung. Sie haben gegenüber klassischen Halbleitern verschiedenen Vorteile. Sie bieten das Potential die Herstellungskosten aufgrund des Einsatzes von Druck- und Spritztechniken zu reduzieren, und erlauben den Einsatz von flexiblen Trägermaterialien. Ihr Nachteil liegt vor allem in niedrigeren Ladungsträgerbeweglichkeiten im Vergleich zu klassischen Halbleitern. Der Forschungsschwerpunkt liegt daher oft in der Suche nach Materialien, die hohe Beweglichkeiten aufweisen oder einfachere und günstigere Produktionsverfahren ermöglichen. Obwohl organische Halbleiter bereits heute kommerziell eingesetzt werden, beispielsweise in Displays, besteht noch großer Bedarf an Grundlagenforschung. Organische Materialien werden durch van-der-Waals-Bindungen zusammengehalten. Daher wirken sich die Eigenschaften der einzelnen Moleküle stark auf die Eigenschaften des organischen Festkörpers aus. Dies erklärt auch die große Vielfalt an Eigenschaften - elektronisch ist die Bandbreite von Isolatoren bis zu Supraleitern vertreten. Durch gezielte Synthese bietet sich der Chemie somit die Möglichkeit neue Materialien maßgeschneidert zu entwickeln, sofern die Mechanismen des Ladungstransports verstanden sind. High- $\kappa$ -Dielektrika, Materialien die eine höhere Permeabilität als Siliziumdioxid aufweisen, gewinnen in der klassischen Halbleiterindustrie zunehmend an Bedeutung. Mit der fortschreitenden Miniaturisierung der hochintegrierten Schaltkreise geht auch eine Reduzierung der Dicke der Isolatorschicht einher. Dies führt unterhalb von 2 nm zu einem starken Anwachsen von Tunnelströme und somit zu Verlusten. High- $\kappa$ -Dielektrika bieten die Möglichkeit die nötige Kapazität mit dickeren Schichten zu erreichen und somit Leckströme zu reduzieren. Mithilfe von high- $\kappa$ -Dielektrika lassen sich aber auch hohe Flächenladungsdichten erreichen, da sie ebenfalls hohe Durchbruchspannungen besitzen.

Das Mittel um diese Materialklassen in dieser Arbeit zu kombinieren war der Feldeffekttransistor. Zentraler Bestandteil war die Präparation und Optimierung des high- $\kappa$ -Dielektrikums. Dieses wurde in einer Feldeffekttransistorstruktur verwendet, in der organische Halbleiter als aktive Schicht zum Einsatz kamen. Zunächst wurden bekannte organische Halbleiter verwendet. Die Methode eröffnet die Möglichkeit anschließend auch komplexere Verbindungen, wie z.B. organische Donor-Acceptor-Systeme oder Ladungstransfersalze, zu untersuchen.

Der Feldeffekttransistor ist das wichtigste Bauelement in der modernen Elektronik. Er eignet sich durch seine Aufbau aber auch zum Einsatz in der Grundlagenforschung wie zum Beispiel zur Messung von Ladungsträgerbeweglichkeiten. Insbesondere in der Verbindung mit high- $\kappa$ -Dielektrika ermöglicht er eine starke Erhöhung der Ladungsträgerkonzentration des Halbleitermaterials an der Grenzfläche. Auf diese Weise können hohe Ladungsträgerkonzentrationen in organischen Schichten ohne chemische Dotierung erreicht werden. Der Transistor verfügt normalerweise über drei Anschlüsse, die Source, Drain und Gate genannt werden und entspricht in seiner Funktion einem steuerbaren elektrischen Widerstand zwischen Source und Drain. Bei einem Feldeffekttransistor erfolgt die Regelung des Widerstandes über ein elektrisches Feld, das durch Anlegen einer Spannung an die Gate-Elektrode erzeugt wird. Bei einem Dünnschichtfeldeffekttransistor sind die Source- und Drain-Elektroden mit einer aktiven halbleitenden Schicht verbunden, diese ist wiederum von der Gate-Elektrode durch ein Dielektrikum getrennt. Der Ladungsträgertransport findet an der Grenzfläche von Dielektrikum und aktiver Schicht statt. Ein hoher Widerstand im ausgeschalteten Zustand wird durch eine niedrige intrinsische Leitfähigkeit der aktiven Schicht erreicht. Folglich muss diese möglichst frei von Verunreinigungen, wie zum Beispiel Dopanden sein. Besonders kontrollierte Grenzschichten erlaubt die Präparation in einem Vakuumkammersystem mittels Molekularstrahlepitaxie. Darüber hinaus besteht bei dieser Form der Präparation organischer Schichten die Perspektive, Materialien in dünnen Schichten zu präparieren, die nicht löslich sind.

Als aktive organische Materialien kommen in erster Linie kleine Moleküle, die sublimierbar sind, in Frage. Das in dieser Hinsicht am besten untersuchte Molekül ist Pentacen. Es wurde hier vor allem zum Testen der Apparatur benutzt. Eine weitere interessante Materialklasse bilden die Phthalocyanine. Diese Klasse makrocyclischer Verbindungen besitzt eine planare Struktur und bildet Komplex-Verbindungen, bei der unterschiedliche Metalle das zentrale Atom bilden können (Metall-Phthalocyanine). Es besteht darüber hinaus die Möglichkeit alle oder einen Teil der äußeren Wasserstoffatome durch Halogenide zu substituieren. Dadurch wird das Ionisationspotential der Moleküle

geändert, andere elektronische Eigenschaften bleiben dabei aber größtenteils unverändert. Daher können Phthalocyanine als Modellsystem dienen um den Einfluss von Veränderungen der elektronischen Struktur auf den Ladungstransport zu untersuchen. In dieser Arbeit wurde hauptsächlich Kupferphthalocyanin (CuPc) als aktive Schicht eingesetzt.

Als high- $\kappa$ -Dielektrika bieten sich vor allem Oxide mit Pervoskit-Struktur an; in dieser Arbeit wurde Strontiumtitanat ( $\text{SrTiO}_3$ ) ausgewählt. Kristallines Strontiumtitanat besitzt eine Dielektrizitätskonstante von 300 (bei Raumtemperatur) und kann auf verschiedene Arten als Dünnschicht im Vakuum präpariert werden. Es ist ebenfalls als dotiertes, und somit leitfähiges, Substratmaterial erhältlich. Somit verfügt man über ein ideales Wachstumstemplate bei dem das Substrat als Gate-Elektrode fungiert.

Als elektrische Kontakte kommen Metalle zum Einsatz. Oft, wie auch in dieser Arbeit wird Gold verwendet, da es nicht reaktiv ist und aufgrund seiner Austrittsarbeit eine niedrige Injektionsbarriere für Löcher darstellt.

Ein Hauptteil dieser Arbeit war daher zunächst der Aufbau eines Ultrahochvakuumkammersystems zur in-situ Präparation von Feldeffekttransistoren und die Integration in ein bestehendes System zur Präparation metallischer Dünnschichten. Als verbindendes Element diente dabei das bestehende Modul zum Transfer der Proben innerhalb des Kammersystems. Es wurden separate Kammern für die verschiedenen Prozessschritte, eine Schleusenkammer und der Großteil der zugehörigen Komponenten konstruiert und in Betrieb genommen. Die wichtigsten Kammern waren dabei eine Kammer zur Deposition der organischen Schichten, eine Kammer zur Präparation des Dielektrikums und eine Kammer zur Kontaktpräparation.

Die Kammer zur Deposition der organischen Dünnschichten wurde als Molekularstrahlepitaxiekammer konstruiert. Sie ist zylinderförmig mit einem Durchmesser von 400 mm und bietet somit genug Raum für den Einbau von sechs Verdampferquellen. Die Verdampferquellen und der Manipulator zur Probenaufnahme wurden den Anforderungen entsprechend konstruiert. Der Manipulator ist in der Lage die Proben sowohl zu heizen als auch zu kühlen ( $-60\text{ °C}$  bis  $580\text{ °C}$ ) und besitzt eine hohe Temperaturstabilität. Als Verdampferquellen wurden selbstkonstruierte Effusionszellen verwendet. Dabei wurde mit verschiedenen Ausführungen experimentiert um sowohl Aufdampfcharakteristik, Temperaturstabilität zu optimieren, die Relaxationszeit zu verkürzen als auch um Kondensation im oberen Bereich der Zelle zu verhindern. In der Nähe der Aufdampfposition des Manipulators befindet sich ein Schwingquarz zur Kontrolle der Aufdampfrate.

Die Kammer zur Präparation des Dielektrikums wurde als Sputterkammer konstruiert. Sie basiert auf einem Doppelkreuz und wurde mit zwei Sputter-

Kathoden bestückt. Als Sputtergase können Argon und Sauerstoff in variablem Mischverhältnis gesteuert über Masseflussregler eingesetzt werden. Der selbstgebaute Manipulator ermöglicht Temperaturen bis zu 900 °C, sowohl im Vakuum als auch unter Sauerstoffatmosphäre.

Die Kontaktpräparationskammer basiert ebenfalls auf einem Doppelkreuz. Sie wurde mit einer kommerziellen Effusionszelle bestückt. In dieser Kammer wurde ausschließlich Gold verdampft. Um die unterschiedlichen Schichten in-situ in den benötigten Strukturen zu deponieren wurde ein Schattenmaskensystem entwickelt. Die Masken befinden sich in einer Halterung in der Kontaktpräparationskammer und können in dieser mit Hilfe eines Greifers auf den Probenträgern positioniert werden. Durch den kleinen Abstand zwischen Substratoberfläche und Maske ließen sich scharfe Strukturen erzeugen. Das System erlaubt auf diese Weise den Gebrauch der Masken in allen Kammern. Die kleinste realisierte Strukturgröße war dabei eine Kanallänge (Distanz zwischen Source und Gate) von 20 µm. Die Strukturen zur Transistorpräparation waren dabei auf den benötigten Masken vierfach vorhanden.

Die Schleusenkammer ermöglichte die Aufnahme von bis zu drei Probenträgern und wurde mit einem automatisierten Ausheizsystem ausgestattet.

Die benötigten Dünnschichten zur Herstellung der Transistorstrukturen wurden zunächst einzeln präpariert und charakterisiert. Dazu wurden in erster Linie Röntgenbeugung und optische Mikroskopie eingesetzt. Mittels Röntgenbeugung war es möglich sowohl die Dicke der Schichten und somit die Depositionsraten zu bestimmen, als auch über das Auftreten von Bragg-Reflexen die Orientierung der Schichtebenen und Netzebenenabstände zu ermitteln. Das Mikroskop lieferte vor allem bei der Beurteilung der gesputterten Strontiumtitanatschichten Informationen über die Homogenität und Oberflächenbeschaffenheit.

Pentacen wurde bei einer Temperatur von 200 °C auf  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> als Substrate verdampft. Das Filmwachstum wurde für Substrattemperaturen zwischen 305 K und 350 K untersucht. Mit Röntgenbeugung konnten die (001)-Reflexe der Dünnschichtphase bis zur fünften Ordnung nachgewiesen werden. Dabei trat keine Verschiebung der Reflexpositionen durch eine konkurrierende Bulkphase mit der Temperatur auf, die in der Literatur auf Siliziumsubstraten normalerweise beobachtet wurde. Die höchste kristalline Ordnung wurde bei einer Substrattemperatur von 330 K beobachtet, mit einer auflösungslimitierten Rockingkurvenbreite des (001)-Reflexes von 0.019°.

Bei den Wachstumsstudien an Kupferphthalocyanin wurden sowohl  $\alpha$ -Al<sub>2</sub>O<sub>3</sub>- als auch SrTiO<sub>3</sub>-Substrate verwendet. Dabei konnten keine Unterschiede im Filmwachstum aufgrund der Substratwahl nachgewiesen werden. Mit Röntgenbeugung wurde ausschließlich die  $\alpha$ -Phase beobachtet. Es zeigte sich jedoch ein

Einfluss der Substrattemperatur. Bei niedrigen Temperaturen ( $<50\text{ }^\circ\text{C}$ ) wurden nur kleine Bragg-Reflexe gemessen, dafür wiesen die Filme aber niedrige Rauigkeiten auf, was durch das Auftreten von Kiessig Oszillationen beobachtet wurde. Mit zunehmender Substrattemperatur zeigte sich eine Erhöhung der Bragg-Reflexe und damit der Kristallinität aber auch eine zunehmende Rauigkeit. Zur Präparation der Transistoren wurde ein mittlerer Temperaturbereich mit einer Substrattemperatur von  $85\text{ }^\circ\text{C}$  ausgewählt. Die Zelltemperatur betrug dabei jeweils etwa  $360\text{ }^\circ\text{C}$ .

Für einen funktionierenden Transistor ist ein leckfreies Dielektrikum Voraussetzung. Das Sputtern von Strontiumtitanat als high- $\kappa$ -Dielektrikum wurde daher untersucht und optimiert. Dazu mussten gleichzeitig eine hohe Depositionsrate, eine glatte Filmoberfläche und eine gute Kristallinität der Schicht erzielt werden. Der Sputterprozess verfügt über eine Fülle von Parametern, als wichtigste wurden dabei Substrattemperatur, Druck und Sputterleistung identifiziert. Eine große Herausforderung stellte dabei die benötigte hohe Substrattemperatur dar, sodass der Manipulator mehrfach überarbeitet werden musste. Während der Optimierung wurden als Substrate  $\alpha\text{-Al}_2\text{O}_3$  und vor allem MgO verwendet. MgO besitzt eine zu  $\text{SrTiO}_3$  ähnliche Kristallstruktur mit einer etwas größeren Gitterkonstante. Während auf  $\alpha\text{-Al}_2\text{O}_3$  neben der gewünschten (100) auch (110) und (111) Orientierung bei fast identischen Sputterparametern beobachtet wurden, wuchsen die Filme auf MgO (100) vorzugsweise in (100) Orientierung. Diese wiesen im Vergleich zu kristallinem  $\text{SrTiO}_3$  eine Verzerrung zu größeren Gitterkonstanten auf. Der Grad der Verzerrung war dabei abhängig vom Kammerdruck - je niedriger der Druck desto größer die Gitterkonstante. Andererseits war die Depositionsrate ebenfalls druckabhängig und nahm mit zunehmendem Kammerdruck ab. Durch Tempern in Atmosphäre konnte eine Zunahme der kristallinen Ordnung sowie eine Verschiebung der Gitterkonstanten in Richtung des kristallinen  $\text{SrTiO}_3$  erreicht werden. Folglich wurde ein in-situ Temperprozess im Anschluss an die Deposition eingesetzt um die Schichtqualität zu verbessern.

Gold wurde in der Kontaktpräparationskammer mittels einer kommerziellen Effusionszelle aufgedampft. Typische Schichtdicken für die Präparation von Drain und Source lagen im Bereich von 50 nm.

Durch die Kombination der einzelnen Depositionsprozesse wurden Fелеffekttransistoren in Bottom-Gate-Geometrie präpariert. Dabei wurde immer im ersten Schritt  $\text{SrTiO}_3$  auf Niob-dotierte  $\text{SrTiO}_3$ -Substrate gesputtert. Typische Schichtdicken waren dabei etwa 400 nm. Anschließend wurden wahlweise zuerst die Elektroden der Transistoren oder die organische Schicht deponiert, so dass sich Transistoren in „bottom-“ oder „top-“ Kontakt-Geometrie realisieren ließen. Zum Vergleich wurden auch Transistoren auf Siliziumsubstraten mit

einer 300 nm-starken Siliziumdioxidschicht als Dielektrikum präpariert. Zur Untersuchung der Transistoren wurde ein Messaufbau erstellt. Es wurden verschiedene Programme entwickelt, um sowohl das Dielektrikum als auch die Ausgangs- und Transferkennlinien der Transistoren zu vermessen. Die Transistoren wurden dazu zunächst ex-situ kontaktiert und die Funktionalität des Dielektrikums überprüft. Die Ausbeute an funktionsfähigen dielektrischen Schichten war zunächst niedrig, konnte aber im Verlauf dieser Arbeit erhöht werden. Aus den gemessenen Kapazitäten der Elektrodenflächen und der Schichtdicke des Dielektrikums wurden Dielektrizitätskonstanten von etwa 190 für die besten high- $\kappa$ -Transistoren ermittelt. Die Transistoren mit CuPc als aktive Schicht zeigten Löcherleitung. Dabei wiesen die Transistoren mit SrTiO<sub>3</sub> als Dielektrikum ein wesentlich stärkeres Ansprechverhalten als diejenigen mit SiO<sub>2</sub> als Dielektrikum auf. Sie erreichten Beweglichkeiten von  $\mu = 2 \cdot 10^{-4} \text{ cm}^2/\text{Vs}$  und ein „on/off-ratio“ von  $10^3$  bei sehr kleinen angelegten Spannungen von  $-3 \text{ V}$ . Die erzielten Beweglichkeiten waren zwar niedriger als die besten Literaturwerte für CuPc-FETs, jedoch wurde das Wachstum der aktiven Schicht im Hinblick auf hohe Beweglichkeiten noch nicht optimiert.

Zusammenfassend wurde ein Mehrkammersystem zur Präparation von Dünnschichtfeldeffekttransistoren konstruiert und in Betrieb genommen. Alle benötigten Einzelprozesse wurden untersucht, wobei der Schwerpunkt auf der Optimierung des high- $\kappa$ -Dielektrikums SrTiO<sub>3</sub> lag. Durch Kombination der Einzelschritte wurden mittels eines Schattenmaskensystems Dünnschichtfeldeffekttransistoren in-situ präpariert. Diese Transistoren wurden in einem externen Messaufbau charakterisiert. Es konnte somit nachgewiesen werden, dass SrTiO<sub>3</sub> sich als Dielektrikum für organische Feldeffekttransistoren eignet und sich durch die Verwendung von high- $\kappa$ -Dielektrika hohe Ladungsträgerdichten erzielen lassen.

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# Chapter 1

## Introduction

This work is positioned at the intersection of two very active areas of research, organic electronics and high- $\kappa$  dielectrics. The tool for the combination of these two areas of research is the field-effect transistor (FET) structure.

The term *transistor* is derived from *transfer resistor*, a device, where the resistance between two terminals can be changed by a third. Accordingly, a field-effect transistor is a device where the modulation of the resistance is achieved by the regulation of an electric field. The principle of operation was first proposed in the 1930s by Lilienfeld [1]. In the 1940s it was studied by Shockley and Pearson [2] and the first working germanium point-contact transistor was announced by Bardeen and Brattain in 1947 [3]. In 1956 John Bardeen, Walter H. Brattain, and William Shockley were awarded with the the Nobel Prize in physics "for their researches on semiconductors and their discovery of the transistor effect". Finally, in 1960 the first metal-oxide-semiconductor field-effect transistors (MOSFET) based on the Si-SiO<sub>2</sub> system was reported by Kahng and Atalla [4]. FETs are now the key component of modern day electronics, they are the fundamental building blocks of electronic devices and computers. But the transistor structure is also useful for the study of fundamental material properties. It is used to study the charge transport in solids and determine the charge carrier mobility, which can be derived from the device characteristics. The exploration of material properties, such as the transport behavior of charge carriers, is today one of the most prominent research fields. It is on the one hand interesting for technical applications, on the other hand, the physical laws which govern the charge transport especially in organic semiconductors are still not fully understood.

The term "organic electronics" is used for the area of electronics where carbon based small molecules or polymers are used as "functional materials". Depending on the application, the functional materials are the semiconductor material itself, but also conductors, dielectrics and e.g. light emitters [5]. In

the following the focus lies on organic semiconductors, which shall serve as the active material in organic field-effect transistors (OFETs) [6]. Compared to inorganic semiconductors organic semiconductors have lower mobilities which hamper the performance for applications where high switching speeds are required. To increase the mobility is one of the main interests in the research field of organic electronics. Although organic semiconductors can not yet reach the performance of inorganic semiconductors in classical semiconductor applications they are very promising for commercial applications in various areas. Apart from lower manufacturing costs they promise advantages over inorganic semiconductors which can include lighter and more flexible materials and enable applications which are impossible using silicon, like for instance flexible displays [7].

Although organic materials are already used in modern day electronics such as the functional material in organic light emitting diodes or solar cells [8], there is still need for fundamental research to understand their intrinsic properties. Since the weak van der Waals interactions are responsible for the cohesion in organic solids they preserve the molecular properties in a stronger way than the covalently bound semiconductors. This leads to interesting properties like anisotropic conduction [9], the possibility to modify the characteristics on the molecular level and explains the wide variation in the organic materials from insulators to superconductors. A further understanding of the mechanisms involved in charge transport in organic materials would also enable the organic chemistry to design new materials according to the desired properties.

The second field of interest are high- $\kappa$  dielectrics which are gaining importance to allow for a further miniaturization of silicon based electronic circuits. With a further miniaturization of integrated circuits in microprocessors the thickness of the gate dielectrics also has to shrink. Eventually, this leads to increasing leakage currents due to tunneling through the thin dielectric layer [10, 11]. One way to overcome this problem is the utilization of high- $\kappa$  dielectrics. These materials have a high relative permittivity and therefore achieve larger polarization than conventional dielectrics. They are also necessary to reach high charge carrier concentrations in active organic materials without chemical doping [12].

In this work no low cost organic devices or a further miniaturization of silicon electronics are the objectives. The focus lies on the preparation of high- $\kappa$  dielectric thin film field-effect transistor structures in which organic semiconductors are utilized as active material. This opens the possibility to study organic semiconductors under influence of high charge carrier concentrations. This is also done with a perspective to application for more advanced organic semiconductors, such as strong donor-acceptor systems or charge transfer com-

pounds.

The charge transport in a thin film FET takes place at the interface between the dielectric and the semiconducting layer. The experimental conditions at this interface must be well controlled to prevent contaminations or oxidations of the organic materials. The cleanest interfaces can be realized in a vacuum environment. Thus a vacuum chamber system consisting of inter-connected vacuum chambers for the different steps in the device preparation was constructed. Organic molecular beam deposition (OMBD) under ultrahigh vacuum was chosen as the preparation method for the organic layers. SrTiO<sub>3</sub> was chosen as high- $\kappa$  dielectric and radio frequency (RF) sputtering was selected as deposition method. A shadow mask system to define the structures was realized to allow for the entire device preparation in-situ. The different thin films were characterized and an ex-situ setup for electronic measurements of the transistors was assembled.

In the following chapters the most important properties of field-effect transistors, organic semiconductors and high- $\kappa$  dielectrics are summarized. Then the experimental setup for the preparation of the different layers is described. The characterization methods are briefly outlined and the deposition conditions are reported. Finally, measurements on successfully prepared transistors are presented.



# Chapter 2

## Organic electronics and materials

Organic electronics deals with molecules or polymers used in electronic circuits. Despite the advantages organic electronics offer they are expected to complement the inorganic electronic and not to replace it, since the mobilities in inorganic materials are much higher. The reason for the lower mobility of organic semiconductors can be found in the different material structure and interactions of the individual atom. These differences lead also to differences in the charge transport mechanisms.

In the group of organic conductors one distinguishes between polymers and small molecules. Polymers are typically amorphous and highly disordered which makes the modeling of the transport very difficult. An important part of the transport in polymers is intramolecular transport mediated by  $\pi$ -orbitals along the chains. In contrast, small molecules can form ordered crystal structures and intermolecular transport determines the conductivity. The transport properties can therefore be highly anisotropic both in single crystals grown by physical vapor [13] or solution growth and in ordered thin films. This offers the possibility to study fundamental transport properties when samples of high purity and order are available. In the following only the properties of small molecules will be considered.

In the second part of this chapter the small molecules, *copper phthalocyanine* and *pentacene*, which were used during this work will be introduced.

### 2.1 Electronic structure of organic solids

In a single polyatomic organic molecule the Coulomb potentials of the atomic nuclei and electrons interact to form molecular orbitals (Fig. 2.1). In contrast to atomic orbitals the designated molecular  $\pi$ -orbitals in these systems are delocalized over the molecule. The  $\pi$ -bonds are usually weaker than  $\sigma$ -bonds and

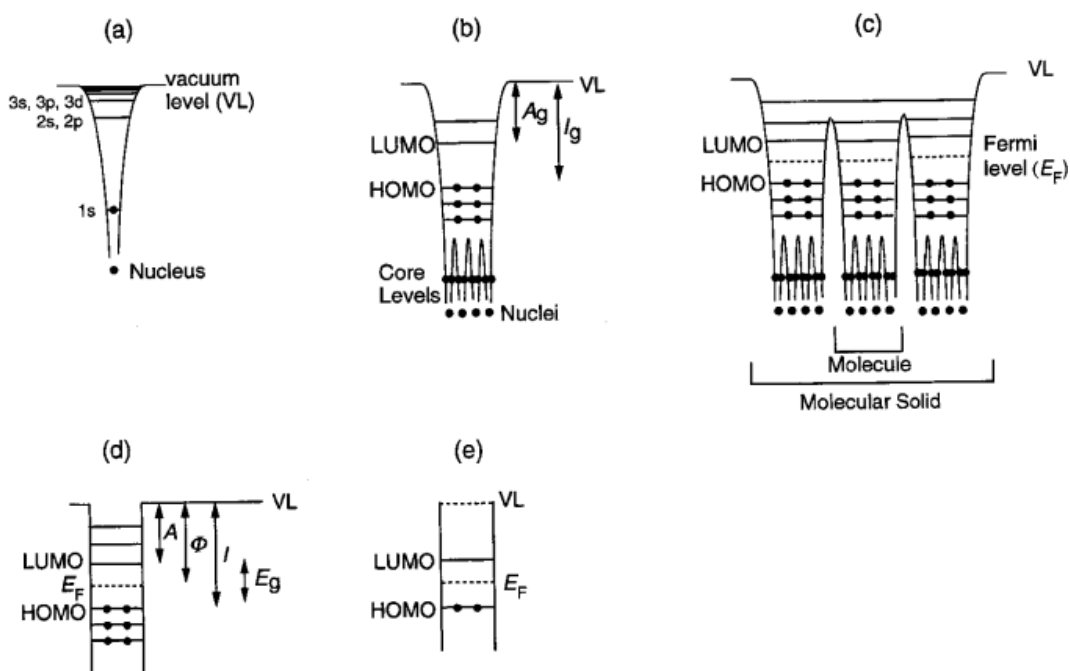


Figure 2.1: Electronic structures

These sketches illustrate electronic structures with potential wells. a) pictures a Hydrogen atom, b) a polyatomic molecule. In c) the molecules form a organic solid with weak interaction between the molecules. In d) and e) simplifications of c) are drawn. The abbreviations stand for  $I_g$ : gas phase ionization energy,  $A_g$ : gas phase electron affinity,  $I$ : solid state ionization energy,  $A$ : solid state electron affinity,  $\Phi$ : work function, and  $E_g$ : HOMO-LUMO band gap. Taken from [14].

the electronic excitations in molecular crystals are rather low (a few eV) [15]. The highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) are usually  $\pi$ -orbitals and are among the most important characteristics of organic molecules. The energy separation from the HOMO to the vacuum level is called ionization energy  $I$ , the distance from the LUMO to the vacuum level is the electron affinity  $A$ . These terms are used not only for single molecules but also for organic solids. The energy gap between HOMO and LUMO is termed the band gap  $E_g$ . It can serve as a measure for the excitability and in case of an optical transition determines the color of the solid. The van der Waals interaction between the individual molecules is responsible for the intermolecular structure. Since the interaction is weak, the molecular orbitals are localized on each molecule. The formation of wide intermolecular bands is hindered and the single molecule electronic structure

is largely preserved [14]. This is also the reason for the two different models which describe the charge transport in organic molecular crystals. Molecules which form conjugated  $\pi$ -electron systems, such as aromatic systems, are of special interest (comp. Fig. 2.2). In these systems an overlap of stacked  $\pi$  orbitals leads to improved transport properties.

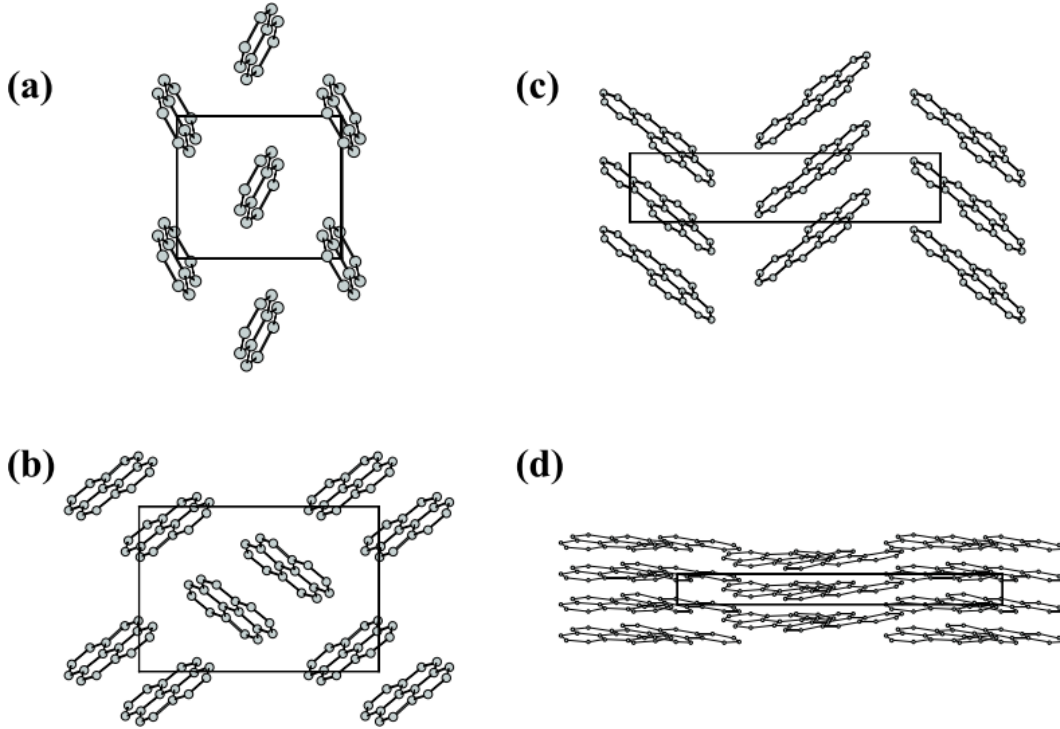


Figure 2.2: Crystal packings

The four different crystal packings observed for aromatic hydrocarbon crystals. (a) Naphthalene as an example of a herringbone structure (b) Pyrene in a sandwiched herringbone structure (c) Benzopyrene as an example of a  $\gamma$  structure (d) Violanthrene an example of a  $\beta$  structure. Taken from [16].

## 2.2 Charge transport and mobility

In organic semiconductors there are two theoretical models to describe the transport mechanisms, namely band transport and hopping transport. One important parameter which characterizes the transport properties in a material is called the mobility. One distinguishes between the electron and the hole mobility. They are proportionality factors between the applied electric field and

the average drift velocity of the electrons and holes ( $v_d = \mu E$ ). The mobility is an important factor for the switching speed of devices. The charge transport in metals and conventional semiconductors occurs in delocalized states which extend over the whole material. In these materials the strong interatomic interactions lead to the formation of wide bands and relatively high mobilities [17].

The mobility is affected by various mechanisms such as carrier scattering processes. In conventional semiconductors this leads to a decrease of the mobility with increasing temperature with

$$\mu \propto T^{-n}, \quad (2.1)$$

where  $n > 1$ . The main scattering processes, which influence the mobility are the so-called *ionized impurity scattering* from donor or acceptors in the semiconductor and the *(lattice) phonon scattering*. The phonon concentration increases with increasing temperature. This in turn causes an increased scattering of the carriers and thus a decrease of the mobility from interactions with acoustic phonons of the lattice,  $\mu_l$ , with

$$\mu_l \propto \frac{1}{m_c^{*\frac{5}{2}} T^{\frac{3}{2}}}, \quad (2.2)$$

where  $m_c^*$  is the effective mass for conductivity calculations [18]. Scattering from ionized impurities decreases with increasing temperature because carriers with higher thermal velocity are less deflected by Coulomb scattering. The mobility  $\mu_i$  is described by

$$\mu_i \propto \frac{T^{\frac{3}{2}}}{N_I m^{*\frac{1}{2}}}, \quad (2.3)$$

where  $N_I$  is the ionized impurity density [19]. The combined mobility is given by the Matthiessen rule to

$$\frac{1}{\mu} = \frac{1}{\mu_l} + \frac{1}{\mu_i}. \quad (2.4)$$

Measured values for pure samples near room temperature yield a temperature dependence of the mobility of  $T^{-2.42}$  for  $n$ -type and  $T^{-2.20}$  for  $p$ -type Si [20]. Organic semiconductors reach mobilities of up to 10 cm<sup>2</sup>/Vs at room temperature, low compared to conventional semiconductors, e.g. silicon up to 450 cm<sup>2</sup>/Vs for holes and 1400 cm<sup>2</sup>/Vs for electrons (comp. Fig. 2.3) [21]. Band transport occurs in ultra pure organic crystals where the charge carriers are almost solely scattered at phonons and the conductivity is increasing with decreasing temperature. In contrast, most organic semiconductors show an increasing mobility with increasing temperature. The charge transport



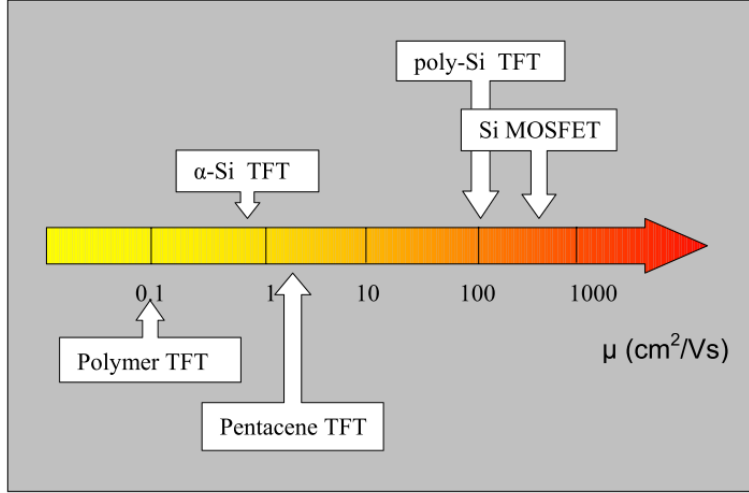


Figure 2.3: Scale of field-effect mobilities

The scale of the field-effect mobilities in different types of field effect transistors. Taken from [22].

mechanism in organic semiconductors is than attributed to phonon assisted hopping between localized states. When the charges are localized like in disordered crystals or layers, the transport is thermally activated and therefore the mobility is increasing with increasing temperature. The mechanism is called hopping transport because the charges move by hopping from site to site. The temperature dependence follows an Arrhenius behaviour

$$\mu \propto \exp^{\frac{-E_a}{k_B T}}, \quad (2.5)$$

with an activation energy  $E_a$ . The cross-over region between hopping and band transport is often defined by a mobility in between 0.1 and 1  $\text{cm}^2/\text{Vs}$ . The organic semiconductors with the highest mobilities like pentacene or rubrene reach or surpass this limit. Furthermore, there are examples for temperature independent mobility in organic thin film transistors, for example for pentacene. This excludes thermally activated hopping as the fundamental transport mechanism [23].

The mobility of organic crystals is often measured with the time-of-flight method [24]. A crystal of the material is placed between two electrodes, one of these must be transparent for a laser of a given wavelength, and an electrical field is applied. The charge carriers are excited in a thin sheet at the transparent electrode by a laser pulse. From the propagation of the charges under the influence of the bias and the thickness of the crystal the mobility can be

calculated.

The second method to measure the mobility of organic materials is the preparation of field-effect transistors, where the mobility can be derived from the device characteristics. This will be explained in more detail in chapter 8, in conjunction with the measured devices. With this method it is possible to measure the mobility not only of single crystals but also of thin films. This is much more interesting for technical applications and devices. In an OFET the charges are induced at the interface between the organic semiconductor and the dielectric. They move only in a thin sheet at the interface. Therefore the measured mobilities very often differ from the bulk value. The density of charge carriers can be much higher and interactions between them may become important.

In practice the charge transport is often dominated by chemical impurities and defects. Chemical impurities often act as dopant and defects as charge traps. A careful preparation of the devices is therefore of importance.

## 2.3 Copper Phthalocyanines

Copper phthalocyanine (CuPc) ( $\text{CuN}_8\text{C}_{32}\text{H}_{16}$ ) is a crystalline synthetic blue pigment from the group of phthalocyanine dyes. The chemical structure is depicted in Fig. 2.4. These dyes are commonly used in the industry, e.g. for optical disks, printing inks or textiles. CuPc is generally regarded as *p*-type semiconductor [25], but ambipolar transport has also been reported on CuPc single crystal field-effect transistors recently, with hole mobilities reaching  $3 \text{ cm}^2/\text{Vs}$  [26]. Studies of the electronic structure indicate that the Fermi energy of CuPc lies in the middle of the HOMO-LUMO gap. This implies that CuPc without impurities is an intrinsic semiconductor and the *p*-type-like behavior most likely arises from oxygen impurities [27]. CuPc has a high thermal and chemical stability and can be sublimed in vacuum. CuPc crystallizes in different structures, the most important ones are the  $\beta$ -phase and the  $\alpha$ -phase, but also  $\gamma$ -,  $\delta$ -,  $\epsilon$ -,  $\pi$ -,  $\tau$ -,  $\chi$ -, and *M*-modifications are reported [28]. In single crystals often the stable  $\beta$ -phase is found where the molecules arrange in layers with a herringbone structure [29]. The monoclinic cell parameters are  $a = 19.047 \text{ \AA}$ ,  $b = 4.790 \text{ \AA}$ ,  $c = 14.628 \text{ \AA}$  and  $\beta = 120^\circ$  [30].

The metastable  $\alpha$ -phase is frequently reported for vacuum sublimation of CuPc. The crystal structure was re-determined by Hoshino *et al.* [28] to the lattice parameters  $a = 12.886 \text{ \AA}$ ,  $b = 3.769 \text{ \AA}$ ,  $c = 12.061 \text{ \AA}$  and  $\alpha = 96.22^\circ$ ,  $\beta = 90.62^\circ$  and  $\gamma = 90.32^\circ$ . The molecules are stacked in columns with a distance between neighboring planes of  $3.42 \text{ \AA}$  and an angle of  $24.9^\circ$  between the direction normal of the molecule planes and the column direction [28].

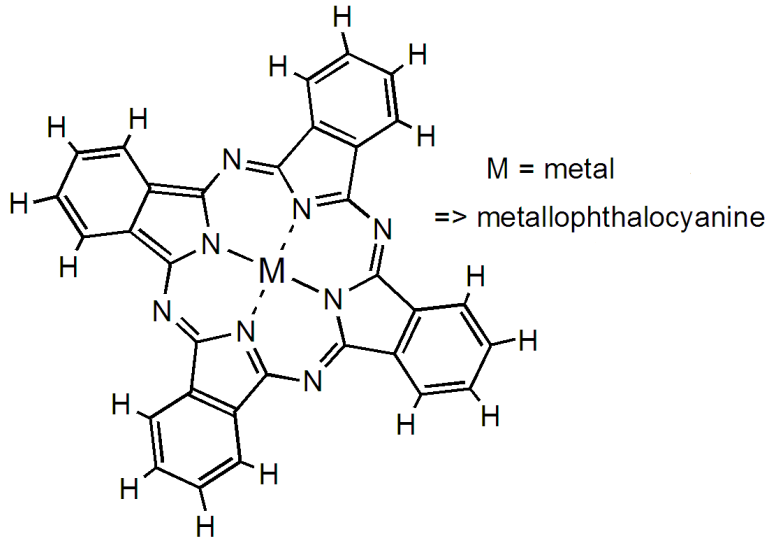


Figure 2.4: Metal Phthalocyanines

Chemical structure of phthalocyanines. Different metal atoms can be substituted in the center of the structure and the hydrogen atoms can be completely or partly replaced by halogen atoms.

There exists a wide variety of phthalocyanines with different metal center atoms. Furthermore, the hydrogen atoms can be partially or fully replaced with electro-negative atoms, such chlorine or fluorine. This changes the ionization potential of the molecules (e.g. 5.05 eV for CuPc, 5.7 eV for CuPcF<sub>4</sub>, 6.1 eV for CuPcF<sub>16</sub>) but further electronic properties, like the optical gap, remain largely unchanged [31, 32]. Since the electron affinity is a function of ionization potential and gap, this explains why fluorinated CuPc, e.g. CuPcF<sub>16</sub> [33], shows *n*-type behaviour [34]. Thus the class of phthalocyanines can serve as a model system for the study of the influence of modifications of the electronic structure on the transport properties [34]. CuPc has been used by various groups in field-effect experiments, usually with SiO<sub>2</sub> as the dielectric [35] when deposited as thin films, but also already with high-permittivity insulators [36] and as single crystals [25]. It is as well used in organic solar cells and light emitting diodes [37].

## 2.4 Pentacene

Pentacene ( $C_{22}H_{14}$ ) is a small molecule of 5 linearly-fused benzene rings, a polycyclic aromatic hydrocarbon. The chemical structure is depicted in Fig. 2.5. It is a flat molecule where the  $\pi$ -electrons form a delocalized cloud above and below the molecular plane. For bulk samples the triclinic crystal structure

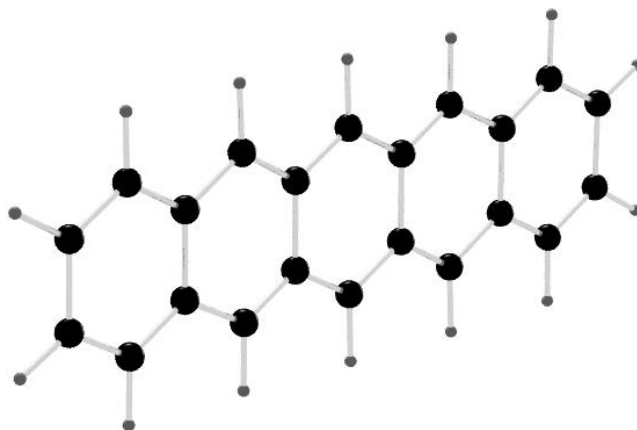


Figure 2.5: Structure of pentacene

This is a POV-ray<sup>1</sup> drawing of the chemical structure of pentacene. Pentacene consists of 5 linearly-fused benzene rings. The larger black orbs represent the carbon atoms, the smaller grey orbs the hydrogen atoms.

with two molecules in a unit cell in a herringbone configuration of dimensions  $a = 7.93 \text{ \AA}$ ,  $b = 6.14 \text{ \AA}$ ,  $c = 16.03 \text{ \AA}$ ,  $\alpha=101.9^\circ$ ,  $\beta=112.6^\circ$   $\gamma=85.8^\circ$  and space group  $P\bar{1}$  was reported by Campbell [38, 39].

Pentacene has a density of  $1.32 \text{ g/cm}^3$  and can be easily evaporated in vacuum at moderate temperatures of about  $200^\circ\text{C}$ . When thin films are prepared, the so called "thin film phase" with  $d(001)$  values of  $14.1 \text{ \AA}$  and  $15.4 \text{ \AA}$  is reported in literature [40, 41, 42]. There is evidence for at least four different polymorphs of pentacene [16]. The differences are related to growth conditions such as substrate material and orientation, temperature, deposition rate and thickness of the films.

Pentacene is probably the most thoroughly studied organic semiconductor ( $p$ -type) with one of the highest reported mobilities for organic materials with more than  $1 \text{ cm}^2/\text{Vs}$  obtained from thin film FET measurements [23, 43]. The

efficient charge transport depends on an efficient  $\pi$ -orbital overlap between the molecules, and hence on the crystallinity of the thin film. This was shown by depositing on substrates with different temperatures; on cooled substrates amorphous films are obtained with extremely low conductivity, at room temperature well ordered films with high mobility are obtained. When the temperature is further increased a double phase, a mixture of two phases observed as two distinct peaks in X-ray diffraction, was reported with lower mobility, possibly related to a high defect concentration from the competing phases [44]. It has also been shown that the electronic structure of the surface can control the orientation of pentacene molecules during growth [45].

## 2.5 Organic superconductors

Another very interesting material class are the organic superconductors. Among those are the charge transfer salts based on the bis(ethylenedithio)-tetrathiafulvalene (BEDT-TTF) molecule [46, 47]. These charge transfer complexes are formed by small, planar organic molecule as electron donors in combination with electron acceptors. They show structural similarity and analogies in phase diagrams to the high temperature superconductors [48]. BEDT-TTF is a strong electron donor and it forms charge transfer compounds with a variety of acceptors. The superconductors of this material class can reach a transition temperature of more than 10 K at ambient pressure [49] and are strongly correlated materials [50, 51]. To use BEDT-TTF based charge transfer complexes in thin film field-effect device was one of the objectives of this work. Therefore it was attempted to prepare thin films of BEDT-TTF and the charge transfer complex (BEDT-TTF)(TCNQ) by evaporation in ultra high vacuum. It proved to be very difficult to obtain layers of sufficient quality, as detailed in [52, 53]. Consequently, in this thesis the focus is on FETs with CuPc as the semiconducting layer.

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<sup>1</sup>Created with the program KPovModeler (<http://www.kpovmodeler.org/>) which is based on the POV-ray rendering engine (<http://www.povray.org/>).



# Chapter 3

## The Field-Effect Transistor

In the first section of this chapter the field-effect transistor structure is introduced. The operation of conventional MOSFETs<sup>1</sup> is briefly reviewed. In the second section the differences of organic and inorganic semiconductor-based transistors are emphasized.

### 3.1 Conventional FETs

Conventional field-effect transistors based on silicon have now been studied for several decades. Their behavior and the physics of semiconductor devices is a well-developed field of research with more than 250,000 papers published since 1981 [20]. The general principles of organic devices are similar to those of conventional ones and their properties are often compared and benchmarked to silicon based transistors. It is therefore useful to review the fundamental operation principles of conventional transistors.

#### 3.1.1 The MIS structure

The metal-insulator-semiconductor (MIS) capacitor structure is the foundation of the field-effect transistor. In this structure the interplay of the gate and the channel of the FET can be explained. The MIS junction consists of a stack of metal, insulator and doped semiconductor.

The energy-band diagram of the ideal MIS structures for a *p*-type (hole conducting) and a *n*-type (electron conducting) semiconductor is shown in Fig. 3.1.

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<sup>1</sup>Other terminologies used for the same structure are MISFET (metal-insulator-semiconductor FET) or IGFET (insulated gate FET).

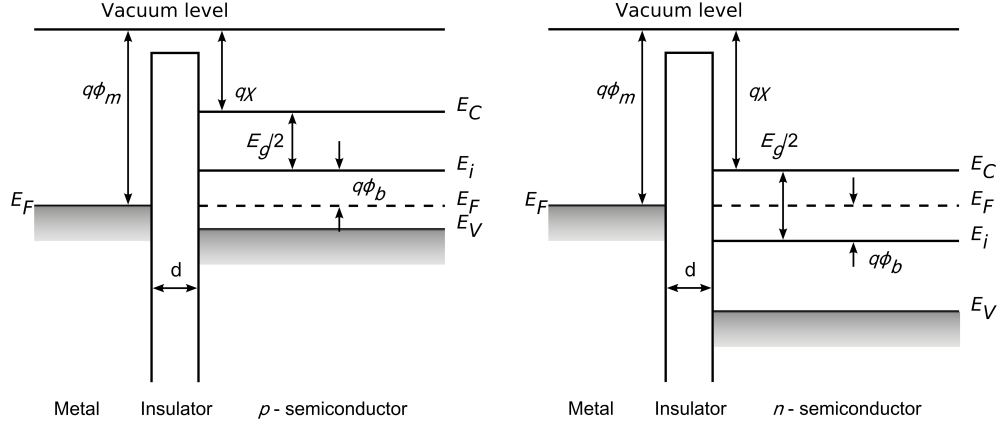


Figure 3.1:  $p$ - and  $n$ -type MIS structures

The figure shows an ideal MIS structure with a  $p$ -type semiconductor on the left and the corresponding structure with an  $n$ -type semiconductor on the right. In both cases the Fermi energies  $E_F$  of semiconductor and metal are aligned. The conduction bands  $E_C$  and the valence bands  $E_V$  are flat. The position of the intrinsic Fermi level  $E_i$  with respect to  $E_F$  depends on the type of dopant.

In an idealized case at zero applied voltage the bands are flat, there is no carrier transport through the insulator and the device is free of defects. For a  $p$ -type semiconductor this is equivalent to the equation

$$\phi_m - \left( \chi + \frac{E_g}{2q} + \phi_b \right) = 0 \quad (3.1)$$

where  $\phi_m$  is the metal's work function,  $\chi$  is the electron affinity of the semiconductor,  $E_g$  is the semiconductor bandgap,  $q$  is the elementary charge and  $\phi_b$  is the potential difference between the Fermi level  $E_F$  and the intrinsic Fermi level  $E_i$  [20, 54]. In the following discussion  $p$ -type semiconductors will be considered. For  $n$ -type semiconductors analogous results are obtained with opposite polarity of the voltages.

When a voltage is applied to the device the Fermi level in the metal is shifted and the bands at the semiconductor-insulator interface are bent. The Fermi level in the semiconductor remains flat since no current is flowing through the insulator. With respect to the voltage three different situations can be distinguished (Fig. 3.2, 3.3).

When a negative voltage is applied to the metal the valence-band edge in the semiconductor bends upwards to the Fermi level. The hole carrier density depends on the energy difference ( $E_F - E_V$ ) and increases at the interface.



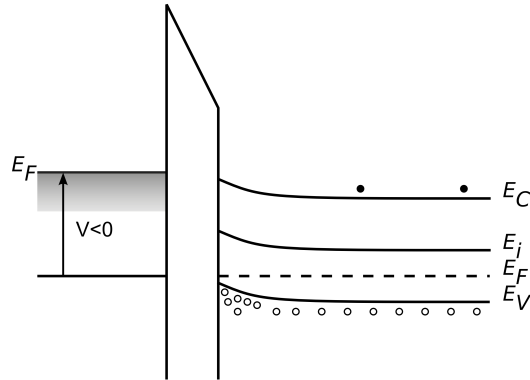


Figure 3.2: Accumulation regime of a  $p$ -type MIS

A negative voltage on the metal side of the MIS junction shifts the Fermi level upwards. The bands in the semiconductor are bent upwards and the majority carrier concentration (holes) at the interface increases. This is called the accumulation mode.

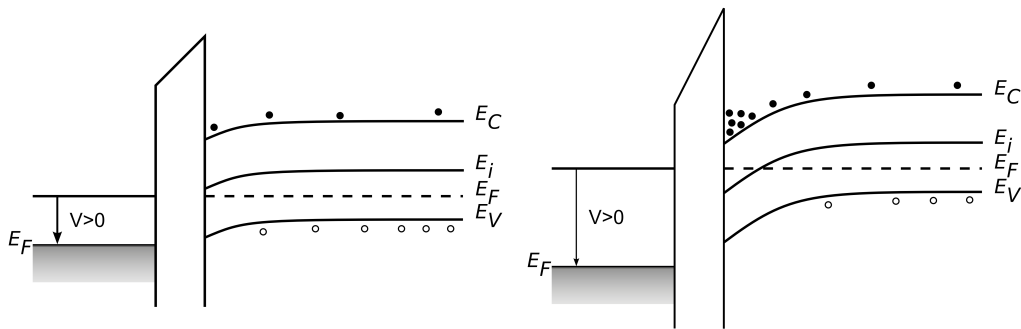


Figure 3.3: Depletion and inversion mode of a  $p$ -type MIS structure

Depletion (left) and inversion (right) are obtained with positive voltage to the metal in a  $p$ -type MIS structure. A positive voltage reduces the Fermi energy  $E_F$  in the metal and bends the bands in the semiconductor downwards. A small voltage reduces the majority carriers at the interface and causes a *depletion*. A large voltage leads to a crossing of Fermi  $E_F$  and intrinsic level  $E_i$  and causes an *inversion* when the number of electrons surpasses the number of holes at the interface region.

Since holes are the majority carriers in a  $p$ -type semiconductor this is called the accumulation case.

When a positive voltage is applied the bands bend downwards. Here two cases have to be distinguished. When the positive voltage is small the majority carriers (holes) are depleted, this is consequently called the depletion case. When the positive voltage is further increased the bands bend further downwards till

at one point the Fermi level  $E_F$  crosses the intrinsic Fermi level  $E_i$ . At this point the inversion case is reached where the number of minority carriers (electrons) at the interface is larger than the number of majority carriers (holes).

### 3.1.2 The MOSFET

Referring to the above discussed MIS structure a FET can be pictured as a MIS device with two additional contacts to the semiconductor. Field-effect transistors can be realized in different geometries. They all have a source and a drain terminal, a conducting channel between these terminals and a gate terminal to capacitively modulate the conductivity of the channel with an electric field<sup>2</sup>. The contact separated by the insulator is the gate terminal, the other two contacts are source and drain (Fig. 3.4). The most common

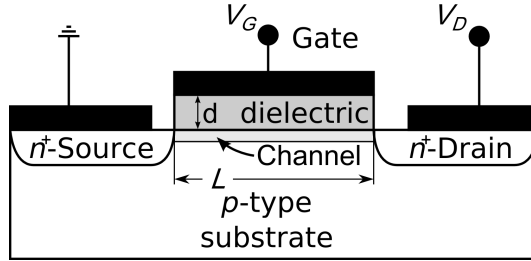


Figure 3.4: Schematic MOSFET diagram

The MOSFET in this figure is fabricated on a  $p$ -type substrate. Source and drain contacts are formed by  $n$ -type doped regions. A dielectric is situated above the channel and metal contacts are used to connect the source, drain and gate terminals.

realization of the field-effect transistor is the MOSFET. The substrate and channel usually consists of a doped semiconducting material e.g.  $p$ -type silicon, and the source and drain terminals are ideally low resistance Ohmic contacts, which is often realized by heavy doping oppositional to the substrate (in this case  $n$ -type). This results in devices which are non-conducting under zero gate bias, since there are two  $pn$ -junctions, one at each side of the channel. Hence, MOSFETs usually operate in the inversion regime. The gate is isolated from the channel by an insulating (usually  $\text{SiO}_2$ ) dielectric layer. In this way the channel and the gate compose a structure equivalent to a parallel plate MIS capacitor where charges are induced at the semiconductor-insulator interface

<sup>2</sup>There are also transistors with more than one gate terminal under development as a strategy to develop smaller device structures.

under the application of a gate voltage and the associated electric field.

When a voltage is applied between the source and the drain the resulting current depends strongly on the gate voltage. This can be pictured in the band model. At the semiconductor-insulator interface the gate voltage causes the conduction and valence band in the semiconductor to bend. Thereby the carrier density in the channel can be enhanced, reduced or inversed, just as discussed in the MIS structure.

In analogy to the MIS, the FET can be classified into different types. The most important distinctions are

- majority carriers of the channel:  $n$ - or  $p$ -channel
- zero bias behaviour:
  - enhancement mode: The device is non-conducting under zero bias, i.e. the device is normally "off" and the conductivity in the channel has to be enhanced by the application of a gate voltage
  - depletion mode: The device is conducting under zero bias, i.e. the device is normally "on" and the channel has to be depleted by applying a gate voltage to change the state of the channel to non-conducting

Accordingly, one categorizes FETs into the type of the charge carriers in the channel and the state of zero bias, e.g.  $n$ -channel, enhancement-mode (normally-off) FET. Each combination results then in different characteristics. Usually, one refers to the *output curve* as the source drain current  $I_D$  over source drain voltage  $V_D$  at fixed gate voltage  $V_G$  and to the *transfer curve*, which is the source drain current  $I_D$  over gate voltage  $V_G$  at fixed source drain voltage  $V_D$  (Fig. 3.5). To calculate the current-voltage characteristics for MOS-FETs Shockley's gradual channel approximation is used. It is assumed that the field perpendicular to the channel exceeds the one parallel to the channel. This condition is fulfilled if the channel length  $L$  is much larger than the insulator thickness. The modulated charge depends then on the gate voltage  $V_G$ , and the local potential in the channel depends on the drain voltage  $V_D$  i.e. the bias between source and drain. Under the assumption of constant mobility  $\mu$  the drain current is given by

$$I_D = \frac{W}{L} C_I \mu \left\{ \left( V_G - V_{FB} - 2\phi_b - \frac{V_D}{2} \right) V_D - \frac{2}{3} \frac{\sqrt{2\epsilon_s q N_A}}{C_I} \left[ (V_D + 2\phi_b)^{3/2} - (2\phi_b)^{3/2} \right] \right\}, \quad (3.2)$$

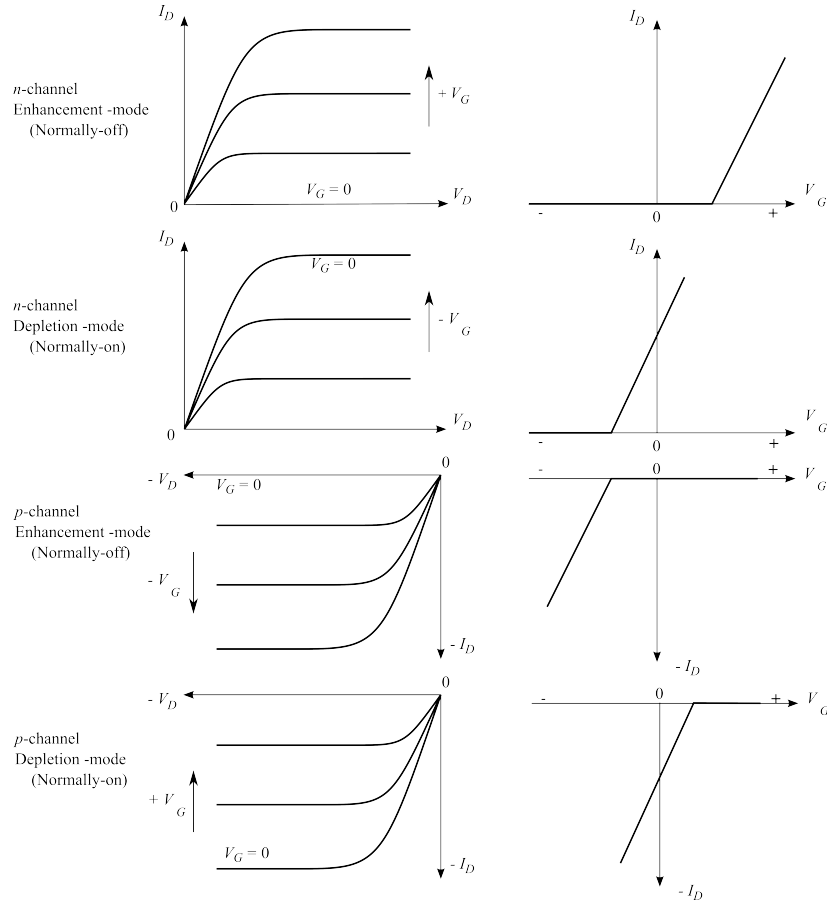


Figure 3.5: Output and transfer characteristics of different MOSFETs

According to the channel type and zero bias behaviour different characteristic curves are obtained. The output curves are depicted on the left and the corresponding transfer curves for a fixed drain voltage  $V_D$  are depicted on the right.

where  $\phi_b$  is the potential difference between the Fermi level and the intrinsic Fermi level,  $\epsilon_s$  is dielectric constant of the semiconductor,  $N_A$  is the acceptor doping concentration,  $C_I$  is the capacitance per unit area of the gate insulator,  $W$  is the width of the channel,  $V_{FB}$  is the flat-band voltage and accounts for work function differences between gate and semiconductor [55, 20].

The drain current characteristic can be separated into three regions. A linear region for small drain voltages, a saturation region for high drain voltages and an nonlinear region between them (Fig. 3.6). Qualitatively, this can be pictured in the following way: Consider a MOSFET with the source terminal at ground and an applied gate voltage  $V_G$  which causes an inversion layer at

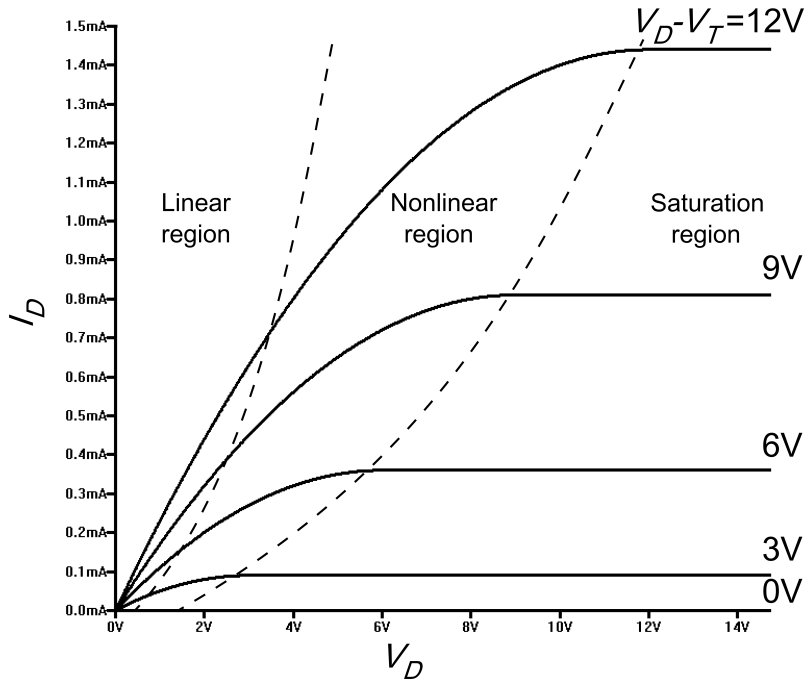


Figure 3.6: Linear, nonlinear and saturation region of a MOSFET

In the output curve of a MOSFET three regions can be distinguished. In the linear region the source drain current  $I_D$  increases linearly with the drain voltage  $V_D$ . In the saturation region a further increase in drain voltage  $V_D$  is pinching off the channel so that the drain current  $I_D$  remains stable. These two regions are separated from each other by the nonlinear region.

the semiconductor-dielectric interface. The carriers which form the inversion originate from the bulk and a depletion region is formed which then separates the inversion layer from the bulk/substrate. For a small drain voltage  $V_D$  the inversion region acts as a conductive channel and behaves as a resistor with source drain current  $I_D$  proportional to the applied voltage ( $V_D$ ). This is called the linear regime.

In the linear regime, for  $V_D \ll (V_G - V_T)$  the quadratic term  $\propto \frac{V_D^2}{2}$  is small as compared to  $(V_G - V_T) V_D$ . The expression for the drain current in the linear region therefore reduces to

$$I_D = \frac{W}{L} C_I \mu \left( V_G - V_T - \frac{V_D}{2} \right) V_D \quad (3.3)$$

where  $V_T$  is the **threshold voltage**, given by

$$V_T = V_{FB} + 2\phi_b + \frac{\sqrt{2\epsilon_s q N_a (2\phi_b)}}{C_I}. \quad (3.4)$$

In MOSFETs which operate in the inversion regime the threshold voltage is the voltage which is necessary to induce the inversion in the channel. It is mainly caused by work-function differences between semiconductor and gate material and fixed oxide charges.

If the drain voltage is further increased, the voltage drop across the oxide at the drain end of the channel ( $V_G - V_D$ ) decreases. Hence the inversion layer thickness at the drain side also decreases as does the conductance of the channel. In this non-linear region the drain current deviates from the linear relationship till the saturation current is reached. At some point the inversion charge is reduced to nearly zero. This is called the pinch-off point and the corresponding drain voltage is called saturation voltage - which of course depends on the gate voltage. Beyond the saturation voltage the pinch-off point moves towards the source, but the voltage at the pinch-off point remains the same, as well as the amount of charge carriers which enter the channel at the source. From the pinch-off point they are swept to the drain in a space charge region by the electric field  $E$ . The channel length is effectively reduced by the length from the drain to the pinch-off point, but usually this reduction is small compared to the total channel length.

In saturation the drain current results in

$$I_{Dsat} = \frac{W}{2LM} C_I \mu (V_G - V_T)^2, \quad (3.5)$$

where  $M$  is a function of doping concentration and oxide thickness

$$M = 1 + \frac{\sqrt{2\epsilon_s q N_a / C_I}}{2\sqrt{\phi_b}}. \quad (3.6)$$

Key figures of merit for a field-effect transistor are the the field-effect mobility and the threshold voltage.

## 3.2 Organic Field-Effect Transistors

Organic FETs can be realized with single crystals or thin films. The structure used with organic thin films is usually the bottom contact or the top contact thin film transistor (TFT) depicted in Fig. 3.7, where top and bottom refers to the position of source and drain with respect to the active layer. Both

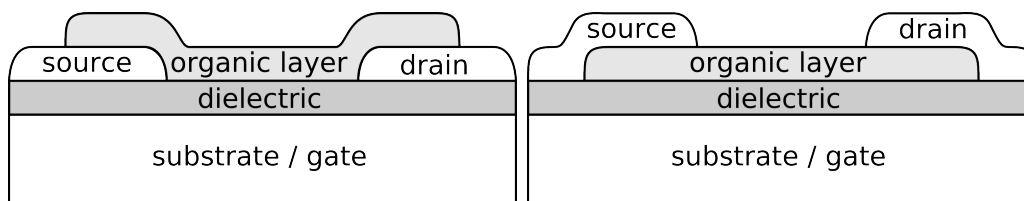


Figure 3.7: TFT in bottom contact (left) and top contact geometry (right)

On a conductive substrate an insulating layer is deposited in the first step. In the usual bottom contact geometry the source and drain contacts are deposited onto the dielectric layer and the active (organic/semiconducting) layer is applied in the last step. For the top contact geometry the deposition order of the active layer and the source and drain contacts is exchanged.

depicted structures are of the bottom-gate type. For single crystals usually a top-gate structure is used, where a dielectric material and gate electrode is fabricated on top of the crystal. These devices work in a similar way as MOSFETs [54]. In both cases an electric field is applied to the organic material via the gate electrode across the insulating dielectric layer. This field attracts or repels charges in a thin sheet at the dielectric-organic interface and modifies the conductivity from source to drain. In contrast to conventional MOSFETs the metallic source and drain electrodes are directly in contact with the channel. The devices operate in the accumulation mode and a low off current is established by using an intrinsic organic semiconductor with low conductivity. In the case of bottom-gate type devices the individual transistors on one substrate share a common gate electrode and can not be switched separately.

### 3.2.1 Device characteristics

The output characteristic of an organic thin film transistor can be derived by transposing the classical silicon MOSFET equations to a TFT structure operating in the accumulation regime [56]. The principle of operation is sketched in Fig. 3.8. The organic semiconductor between the metal electrodes can conduct charges either in the highest occupied molecular orbital (HOMO) or in the lowest unoccupied molecular orbital (LUMO). Usually, only the charges in either HOMO or LUMO contribute to the charge transport due to for example injection barriers at the contacts or a large field-effect threshold, so that the materials can be classified into  $n$ -type or  $p$ -type. However, certain organics also allow for so-called ambipolar transistors [58, 26]. In these devices either  $n$ -type or  $p$ -type transport is possible depending on the gate voltage.

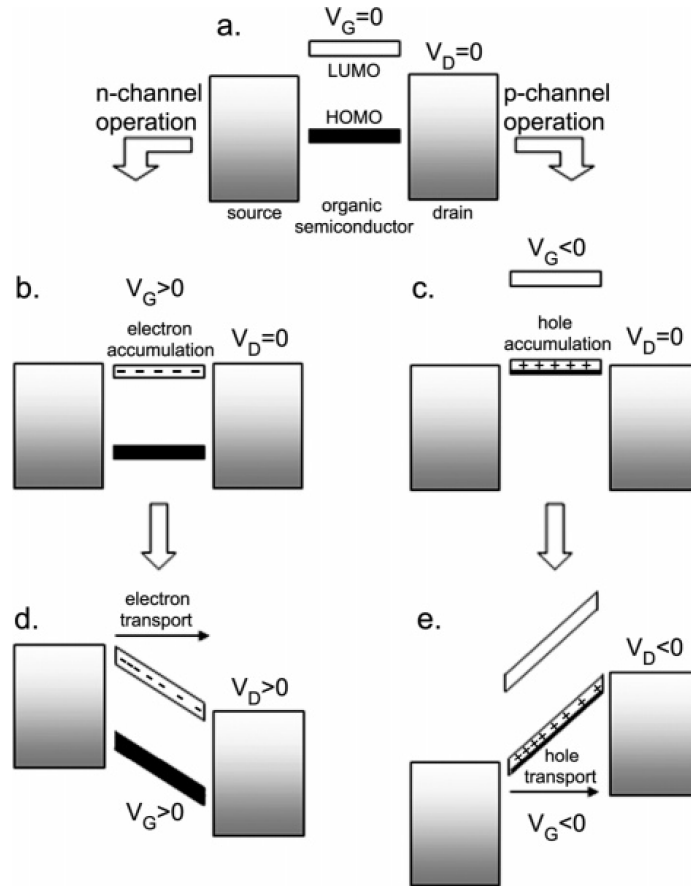


Figure 3.8: Energy diagram of an organic TFT

This sketch shows the idealized energy level diagram of an organic TFT at  $V_G=0$  and  $V_D=0$  (a). The LUMO is above, and the HOMO below the Fermi level of source and gate and the transport is blocked by this energy barrier. The principle of electron (b) and hole (c) accumulation with a positive/negative voltage is shown in the next line. The gate voltage moves the potential in the channel, so that is either HOMO or LUMO become resonant with the electrodes. Electron (d) or hole (e) transport can be achieved when additionally to the gate voltage a drain voltage is applied. Taken from [57].



The gate voltage  $V_G$  induces charges in the HOMO or LUMO which are located in an accumulation layer close to the dielectric-semiconductor interface. The induced charge at a certain position in the channel depends on the distance to the source electrode. Under the assumption of constant mobility within the channel the equations for the linear and the saturation regime can be derived. The solution for the linear regime is [54]

$$I_D = \frac{W}{L} C_I \mu \left[ (V_G - V_T) V_D - \frac{V_D^2}{2} \right]. \quad (3.7)$$

This expression is mathematically the same as for conventional MOSFETs (Eq. 3.3), but there are some subtle differences. First, in contrast to conventional MOSFETs which work in the inversion regime this is an exact solution and not an approximation. Secondly,  $V_T$  is of different origin than in conventional MOSFETs. The threshold voltage of an ideal organic TFT is zero [56], which is a direct consequence of the absence of a depletion layer. Therefore the term *zero voltage* instead of threshold voltage is sometimes used in the literature. Nevertheless, for non-ideal devices the threshold voltage plays the same role as in conventional MOSFETs. The threshold voltage will be further discussed at a later stage.

In the saturation region the channel is pinched off just as in a conventional MOSFET when  $V_D = V_G - V_T$ , and the solution

$$I_{Dsat} = \frac{W}{2L} C_I \mu (V_G - V_T)^2, \quad (3.8)$$

is obtained. This equation is frequently used to determine the mobility by plotting the square root of the saturation current  $I_{Dsat}$  as a function of the gate voltage  $V_G$  (comp. Eq. 8.1). The slope and the intercept of a linear fit yield the mobility and the threshold voltage. The field-effect mobility can also be estimated in the linear region from the transconductance [54]

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D} = \frac{W}{L} C_I \mu_{lin} V_D \quad (3.9)$$

(comp. Eq. 8.2) or the conductance

$$g_d = \left. \frac{\partial I_D}{\partial V_D} \right|_{V_G} = \frac{W}{L} C_I \mu_{lin} (V_G - V_T), \quad (3.10)$$

when  $(V_G - V_T) \gg V_D$  (comp. Eq. 8.3). Often there is a discrepancy between the mobilities in the linear and saturation region [57]. The mobilities in the linear regime are usually lower than the saturation mobilities, which is attributed to the fact that the properties of the contacts effect the linear regime

more strongly [59].

Furthermore, since there is no depletion layer which separates the channel from the bulk of the organic semiconductor, an Ohmic current must be taken into account in parallel to the channel current. Ideally, the Ohmic current

$$I_{Ohmic} = \frac{W}{2L} h n \mu V_D, \quad (3.11)$$

is small compared to the current in the channel, where  $h$  is the thickness of the semiconducting layer and  $n$  is the density of free carriers. This can be achieved by thin devices and a low number of free charge carriers.

### 3.2.2 Threshold voltage

All effects changing the voltage which is necessary to induce mobile charges in the channel are summarized to the threshold voltage [57]. Typical causes are a mismatch between the Fermi level of the metal contacts and the organic semiconductor, analogous to the flat band voltage in conventional transistors. Further contributions to the threshold voltage are deep traps at the semiconductor-insulator interface, which have to be filled before the channel can conduct, or dopands which lead to a conduction at zero gate voltage.

Traps are localized electronic states within the HOMO-LUMO gap, which are caused by e.g. crystal defects due to chemical impurities. In the case of a  $p$ -type semiconductor one can distinguish between shallow traps with a distance of a few  $k_B T$  from the HOMO and deep traps (distance more than a few  $k_B T$  from the HOMO). When the gate voltage is increased, the Fermi level moves towards the HOMO. The deep trap states are the first states which are emptied. Since these states are localized they do not contribute to the transport and therefore the conductance of the channel is still low. A further increase of the gate voltage brings the Fermi level at the organic surface within a few  $k_B T$  of the HOMO and the shallow traps are also emptied. Holes are generated in the HOMO band due to the thermal excitation of electrons from the band into empty localized states and the conductance increases by several orders of magnitude (comp. Fig. 3.9) [60].

### 3.2.3 Subthreshold swing

The subthreshold swing  $S$  is a measure of how quickly (in terms of the steepness of the  $I_D(V_G)$ -curve) a device switches from the off state to the on state and is defined as [57]

$$S = \frac{dV_G}{d(\log I_D)}. \quad (3.12)$$

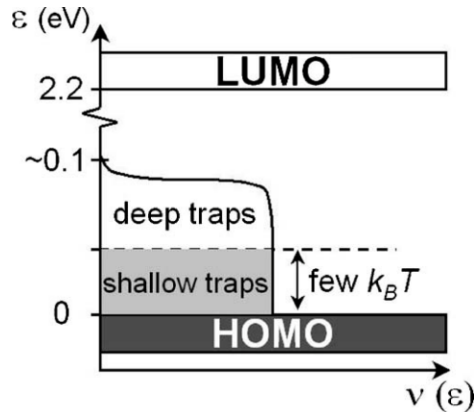


Figure 3.9: Traps

Schematic diagram of the energy distribution of localized electronic states in the energy gap between HOMO and LUMO bands in rubrene single-crystal OFETs. Taken from [60]. One distinguishes between deep and shallow traps with respect to their energy between LUMO and HOMO. For a  $p$ -type organic semiconductor, the traps within a few  $k_B T$  are referred to as shallow, other traps as deep.

The subthreshold swing depends on the quality of the contacts and also on the semiconductor-insulator interface, which influences the number of shallow traps. Since it depends on the dielectric it is more meaningful to use normalized subthreshold swings  $S_n = C_I S$  to compare different devices.

### 3.3 Mott transition field-effect transistors

Another type of field-effect device is the so called Mott transition field-effect transistor (MTFET) [61, 62]. Its geometry is essentially the same as for an ordinary thin film field-effect transistor, but the conduction mechanism in the channel has a different origin. This device works on the basis of the Mott metal-insulator transition [63]. Here the material in the channel consists of a Mott-Hubbard insulator which has an odd number of electrons per unit cell. Although this results in a half filled band the material is non-conductive. The transport is blocked by the repulsive interaction between two electrons on the same site. When a Mott insulator is doped with a certain percentage (typically about 15%) the excess charge carriers can percolate through the material. They form a mobile hole or electron gas and finally a metallic state. At lower carrier concentrations the mobility is low due to a spin exchange process [62]. Materials which show this behavior are for example cuprate superconductors

[64] and charge transfer salts based on organic molecules such as tetrathiofulvalene-tetracyanoquinodimethane (TTF)-(TCNQ) [65] or  $K^+TCNQ^-$  [61]. Even ambipolar injection has been shown in devices based on (BEDT-TTF)-(F<sub>2</sub>TCNQ) [66].

Theoretical studies on MTFETs predict depletion mode devices, when the material in the channel is just a monolayer. Enhancement mode devices are also possible with thicker layers, just as in the TFT structure. However, due to the high required modulations of the charge carrier concentration, gate dielectrics with a high dielectric constant are necessary to build a MTFET. The response curves of a MTFET resemble those of conventional FETs. MTFETs have the advantage that they can be scaled to small dimensions with less limitations, like dopant number fluctuations or tunneling through thin gate oxides, compared to conventional MOSFETs. Dopants, for instance, are either absent or present in high concentration and the dielectric can be thicker due to the required high dielectric constant [61].

### 3.4 Electrical contacts

Source and drain contacts are important parts in field-effect experiments with organic materials. The contact resistivities in organic transistors are typically between 10 k $\Omega$ cm and 10 M $\Omega$ cm, which is large compared to inorganic devices [67]. For the contact preparation several aspects have to be considered. The contact material should be a good conductor and it should ideally form Ohmic contacts to the organic material or at least have only small hole and/or electron injection barriers [68]. It should be non-reactive with the channel material.

Another important point is the source and drain geometry, which defines channel width (source/ drain width) and length (distance between source and drain). The channel length should be short compared to the channel width to minimize edge effects. But it should also be large enough to provide a resistance larger than the contact resistance, otherwise the transistor characteristics are severely influenced [67]. The geometry can be optimized since the contact resistance is independent of the channel size, whereas the channel resistance scales linearly with the channel length.

Ideally, the electrodes are adapted to the HOMO and/or LUMO levels of the organic semiconductor. For *p*-type organic conductors metals with a high work function such as Au are suitable for hole injection. For electron injection in *n*-type devices metals with low work function are preferable. There are many groups which study the influence of the contacts on the electronic structure [14].

Common methods for contact preparation are thin film deposition of metals

combined with structuring techniques (stencil masks, lithography, ...). Since organic materials are sensitive to chemical processing, such as etching and thermal stress during metal deposition, also new methods to prepare the contacts are being developed. One example is a soft contact lamination process, where a kind of stamp is used to fabricate the contact to single crystals [59].

### 3.5 High- $\kappa$ dielectrics

To employ the electrostatic field-effect in a transistor structure a dielectric layer is necessary.  $\text{SiO}_2$  was and still is the most popular dielectric in transistors, since it offers an ideal interface to silicon. With a further miniaturization of electronic circuits also the thickness of the gate dielectric is shrinking to keep the capacitance high enough for a proper switching between the on and off state. A thickness below 2 nm leads to an increase of undesired leakage currents through the  $\text{SiO}_2$  due to the tunneling effect [69].

In modern electronics, materials with a higher permittivity<sup>3</sup> than  $\text{SiO}_2$  are referred to as high- $\kappa$  (or high-k) dielectrics.  $\text{SiO}_2$  with a dielectric constant of  $\epsilon_r=3.9$  serves as the reference value, since it was nearly exclusively used in the semiconductor industry as the gate dielectric of the MOSFET. The gate of a MOSFET bears analogy to a parallel plate capacitor. From the capacitor equation

$$C = \frac{\epsilon_0 \epsilon_r A}{d}, \quad (3.13)$$

it can be seen that a material with a higher dielectric constant  $\epsilon_r$  allows for a larger thickness  $d$  of the gate dielectric to obtain the same capacitance, i.e. polarization. Since the leakage currents depend on the thickness of the dielectric layer, thicker dielectrics reduce the leakage currents. Intel corporation, for example, is very active in the search for high- $\kappa$  dielectrics [70] compatible with silicon technology and favor currently hafnium-oxide based materials as a replacement for  $\text{SiO}_2$ .

In contrast to applications in the semiconductor industry where, e.g., switching speeds and manufacturing processes for the whole devices have to be considered, in fundamental research a larger variety of materials is available. The emphasis is here often on very high polarizations and favorable growth conditions for subsequent layers.

The second important parameter of the dielectric layer in field-effect devices is the breakdown field. The breakdown field is the field strength at which the insulation fails and a breakdown occurs. Usually, a breakdown seriously damages or destroys the insulating capabilities of the dielectric layer. The

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<sup>3</sup>Also called dielectric constant.

breakdown voltage of a device depends on the breakdown field  $E_{BD}$  and the thickness  $d$  of the insulating layer

$$U_{BD} = E_{BD} \cdot d. \quad (3.14)$$

One should note that the dielectric constant  $\epsilon_r$  can also depend on the electric field. The capacitance depends then on the applied voltage as well, according to

$$C(U) = \frac{\epsilon_0 \epsilon_r(U) \cdot A}{d}. \quad (3.15)$$

The maximum charge that can be accumulated is the product of breakdown field and capacitance evaluated at the breakdown field [71]

$$\Delta Q = C(U_{BD}) \cdot U_{BD}. \quad (3.16)$$

With  $\text{SiO}_2$  as dielectric a breakdown field of  $E_{BD} = 10 \text{ MVcm}^{-1}$  and polarizations of  $3 \text{ } \mu\text{Ccm}^{-2}$  are possible at best, while with complex oxide dielectrics polarizations in the range from  $10 - 40 \text{ } \mu\text{Ccm}^{-2}$  can be achieved [12].

### 3.5.1 $\text{SrTiO}_3$

With the aim to achieve a high polarization in the active layer oxides with perovskite structure are a natural choice for the dielectric [72]. A lot of materials of this class have a much larger dielectric constant than common dielectrics, such as for example  $\text{SiO}_2$ , and combined with the maximum breakdown field higher sheet charge densities can be expected. From the perovskite class  $\text{SrTiO}_3$  is one of the best characterized materials. It has a cubic crystal structure with a lattice constant of  $a = 3.905 \text{ \AA}$  and the advantage of a high dielectric constant of  $\epsilon_r=300$  for bulk material at room temperature. A sketch of the perovskite structure is depicted in Fig. 3.10. Thin films of  $\text{SrTiO}_3$  have been grown with various techniques, such as RF sputtering [72, 74], pulsed laser deposition [75] or molecular beam epitaxy [76]. Furthermore, it can be doped with Niobium, which results in a conductive crystalline substrate material [77]. By using a conductive substrate and growing a dielectric layer on top the thin film field-effect transistor structure is realized. In this structure the active layer can be deposited in-situ onto the dielectric layer which ensures clean interfaces. For this reasons  $\text{SrTiO}_3$  was chosen as dielectric for the organic TFTs in this work, with Nb doped  $\text{SrTiO}_3$  as substrate.

The dielectric constant of crystalline samples of  $\text{SrTiO}_3$  increases upon cooling and can reach values of about 20000 below 10 K (comp. Fig. 3.11) [78]. In thin  $\text{SrTiO}_3$  films such strong increases in the dielectric constant have not been observed, yet. The dielectric constant in thin film samples is in general lower

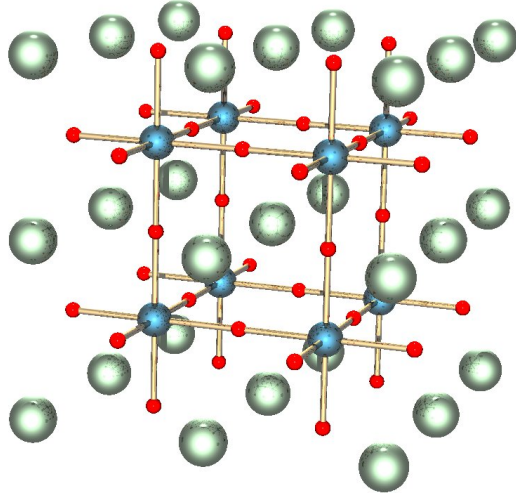


Figure 3.10: POV ray drawing of a perovskite

This is a POV ray drawing of a section of a perovskite lattice, such as of  $\text{SrTiO}_3$ . The red atoms are oxygen and for  $\text{SrTiO}_3$  the blue atoms are Ti and the green atoms are Sr [73].

than in bulk samples most likely due to defects and inhomogeneities of the electric field caused by surface roughness [72]. The relationship of microstructure and electric properties of  $\text{SrTiO}_3$  thin films are also studied but not yet fully understood [79].

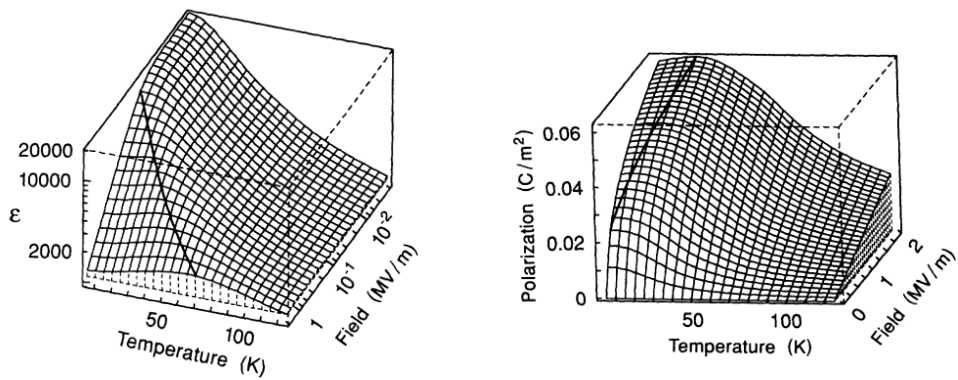


Figure 3.11: Dielectric constant and polarization of  $\text{SrTiO}_3$

On the left the calculated dielectric constant  $\epsilon$  as a function of temperature  $T$  and electric field  $E$  for bulk  $\text{SrTiO}_3$  is shown. The bold solid line indicates the maximum  $\epsilon(T)$  which shifts to higher temperatures for higher fields. The graph on the right shows the calculated resulting polarization. The solid line indicates the maximum polarization with respect to the temperature. Taken from [72].



# Chapter 4

## Preparation setup

The design and construction of the thin film and device preparation equipment represents a major part of this work. The most important features of the different vacuum chambers and the accessory components are described in this chapter.

There are different possibilities to prepare field effect transistors with organic semiconductors as the active layer. The most general differentiation is whether the organic semiconductor is available as a single crystal or as a thin film. In the single crystal case they are often prepared by physical vapor transport or solution growth and the so prepared devices show usually higher mobilities compared to thin film devices. In the thin film case several methods exist with different objectives. There are commercially attractive low cost/high throughput methods like spin coating, dipping techniques, inkjet printing or roll-to-roll processing which are to a large extent still under development. On the other hand the classical methods which were already used for the preparation of inorganic thin films are now used for the deposition of organic thin films as well, like physical vapor deposition which is the most commonly used deposition method in research laboratories. The equivalent of molecular beam epitaxy (MBE) with respect to the deposition of organic layers is called organic molecular beam deposition (OMBD). The OMBD process has several unique features. It enables a precise control over the deposition rate, provides clean interfaces and allows for co-deposition of materials. This also permits the deposition of new charge transfer complexes of, e.g., non soluble reactants. Therefore OMBD was chosen as the preparation method for the organic thin film layers in this work. The OMBD process requires an ultra high vacuum (UHV) chamber. For a full in-situ (i.e. without breaking the vacuum) preparation of an OFET apart from the growth of the organic semiconductor also the additional steps in device preparation, i.e. source, drain and gate electrodes and a (high- $\kappa$ ) dielectric layer, need to be possible in the UHV setup.

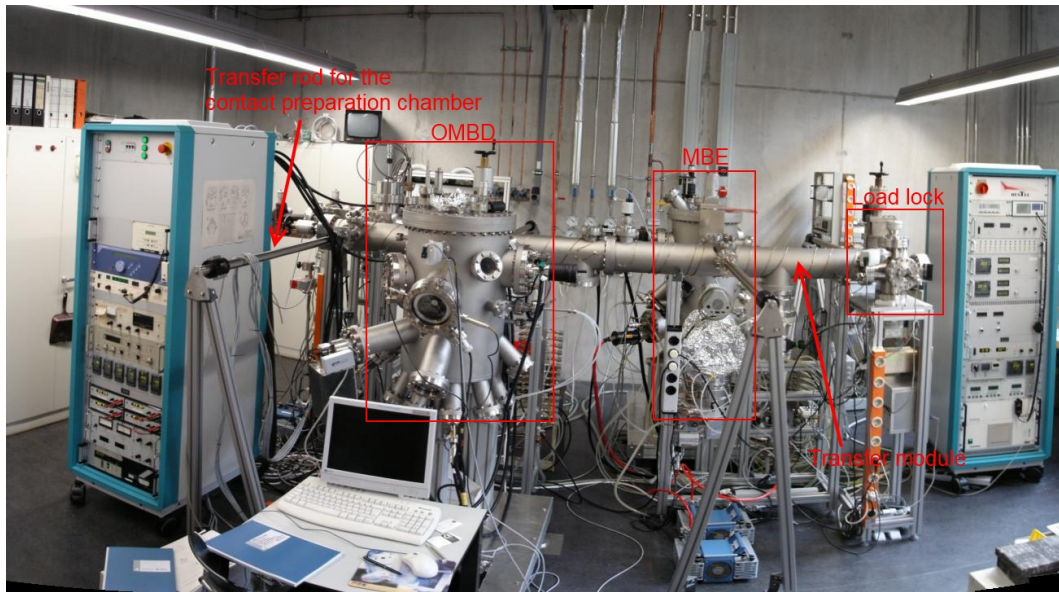


Figure 4.1: UHV-MBE lab

UHV chamber system as used to prepare the thin films and devices. The large chamber in the front is the OMBD chamber where the organic layers were prepared. The long tubular chamber is the transfer module and the small chamber at the right side is the load lock. The MBE chamber is on the other side of the transfer chamber and has about the same size as the OMBD chamber. The contact preparation and sputtering chamber are from this perspective behind the OMBD chamber. The power supplies and controllers for the OMBD and contact preparation chambers are in the left and the controller instrumentation of the MBE, transfer and load lock chamber are in the right rack.

## 4.1 Chamber system

The preparation equipment consists of an UHV chamber system. A picture of the system is shown on Fig. 4.1. The system is connected together by a transfer module with a trolley. The transfer system and one chamber for (metal) molecular beam epitaxy (MBE) was purchased from BESTEC<sup>1</sup>. All other chambers were designed and set-up as a part of this thesis work and will be described in the following. The construction and assembly of the UHV system was performed in cooperation with Kerstin Keller. Further information, especially with respect to the effusion cells can be found in her thesis [52]. The further chambers, which are connected to the preparation system, are an

<sup>1</sup>BESTEC GmbH, Carl-Scheele-Str. 14, D - 12489 Berlin - <http://www.bestec.de>

organic molecular beam deposition (OMBD) chamber, a contact preparation chamber, a sputtering chamber and a load lock chamber. With the exception of the sputtering chamber which is connected to the contact preparation chamber, all chambers are directly connected to the transfer module. They can each be separated by an individual gate valve, and every chamber has a pumping system of its own. The thin films are deposited onto substrates which are attached with conductive silver glue to transferable sample holders.

The transfer mechanism consists of transfer rods with magnetic coupling and a bayonet lock to the sample holder and trolley. The retainer on the trolley is identical to the manipulators in the different chambers. To allow access to both sides of the transfer module the carrier on the trolley can be rotated about a vertical axis by  $180^\circ$  at one end of the transfer module.

Sample access to the sputtering chamber is provided by transfer through the contact preparation chamber.

## 4.2 Sample holders

In a multi-chamber system the sample holder must be transferable to all deposition chambers. Additionally, in situ device preparation using shadow masks was desired. The sample holders had therefore to follow the BESTEC design, with some modification that allowed to mount shadow masks onto them. Furthermore, sample holders were made from different materials according to the different deposition processes. Standard sample holders were made from stainless steel. For low temperature deposition processes, for which a high thermal conductivity is necessary, sample holders were made from copper. For SrTiO<sub>3</sub> sputtering with high temperatures under oxygen atmosphere sample holders made from Inconel were used. The substrate size is limited by the sample holder diameter below 2 inch and with the shadow mask system it is further restricted to a maximum size of 10x10 mm<sup>2</sup>. A sample holder with a mounted shadow mask is reproduced in Fig. 4.2.

### 4.2.1 Shadow mask system

To prepare thin film devices in-situ, it is necessary to sequentially deposit different layers in different patterns. In principle there are two possible approaches. One approach is to provide certain shadow masks in each chamber for the different deposition steps, e.g. by moving the required structure in front of the substrate, or, as realized in this work, mount and unmount exchangeable shadow masks directly onto the sample holder inside the UHV system. Although the latter is arguable more challenging, it provides several advan-

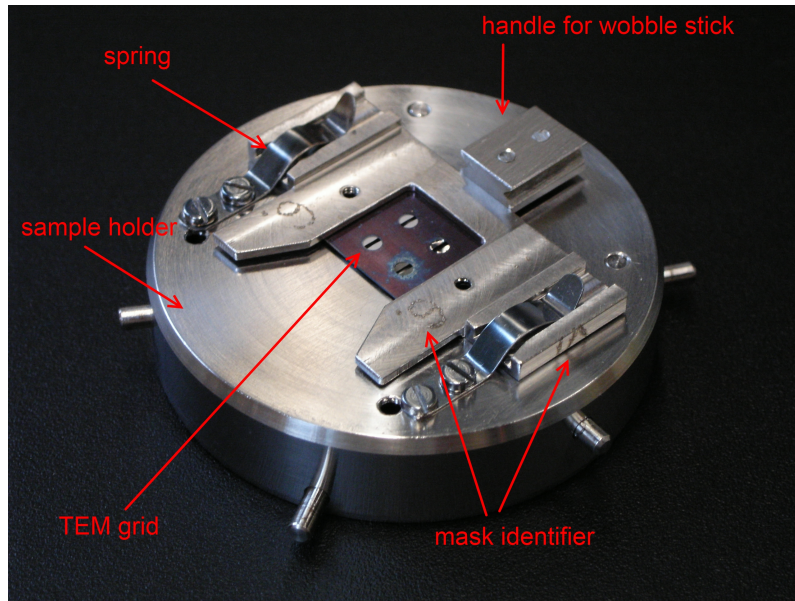


Figure 4.2: Sample holder with mounted shadow mask

Photograph of a sample holder with a mounted shadow mask. The mask can be placed and removed in situ with a wobble stick. The spikes at the front of the mask are used to store the mask in the retainer inside the contact preparation chamber. They also ease the mask transfer process with the wobble stick and help to prevent an accidental removal of the substrate from the sample holder. The pins at the side of the sample holder are used for sample transfer and fixture on the chamber manipulator and on the transfer rods.

tages. It allows for an easy way to exchange and repair masks, because they can be mounted onto a sample holder and moved to the load lock. In that way it is also possible to use a larger variety of different masks without breaking the vacuum in the deposition chambers. It simplifies the design of the other chambers, where no space and flanges have to be considered for shadow masks. Furthermore, it is possible to mount a mask very close to the sample surface which strongly reduces penumbra effects and allows for smaller device structures. One disadvantage of this system is that a larger sample holder is necessary since not only the substrate but also the shadow mask has to be mounted onto it.

To be able to mount masks onto the sample holder two springs were attached to the top and a positioning bore was made below each spring. The positioning bore is required to exactly overlap the structures at the desired spot (comp. Fig. 4.2). All mask are designed identically. The masks have a main

body, made from stainless steel. A thin steel sheet is attached to the body by spot welding. It is important to temper the steel sheets before the spot welding process, otherwise they will bend during the welding process which can cause problems, like scratching, due to the short distance between substrate surface and steel sheet. The sheets for the transistor preparation have four bores of 2 mm diameter. There are TEM (Transmission electron microscope) grids available which, when used as shadow mask, provide a gap of 20  $\mu\text{m}$  between source and drain electrode<sup>2</sup>. A different grid is used to define the area where the active layer is deposited. One of these grids is spot welded to each bore hole. In this way four identical transistors can be realized on a single substrate. Other structures can be realized with different TEM grids or structured steel sheets. Although the sheets are spot welded to the mask body, it is possible to remove them (destructively) with reasonable force, when a different layout is required. The mask body has a block with a v-profile (compare Fig. 4.2) at two sides. This block can be grabbed with a wobble stick equipped with a pincer inside the UHV system to remove/attach the mask from/to the sample holder. The masks can be used in all deposition chambers and processes except for the deposition of  $\text{SrTiO}_3$ <sup>3</sup>.

### 4.3 OMBD chamber

To grow thin films of organic molecules a UHV chamber was designed. First a 3D model was created with POV-ray and was used to e.g. visualize the view through the different ports on the transfer position and verify that enough space was available for the various system components. The chamber was then ordered from VTS Creactec. The chamber is of cylindrical shape with a diameter of 400 mm and a height of 625.5 mm with a total of 30 flanges whereof six flanges were designed for effusion cells. Other flanges are used for the manipulator, a cooling feed through, pressure measurement, a LEED (low-energy electron diffraction) optic, viewports, a port for a quartz crystal micro balance, a mass spectrometer, shutters etc. It is pumped by a Varian *Turbo-V 1001 Navigator* pump in combination with a Varian *TriScroll 300* dry pump and reaches a base pressure of  $10^{-10}$  mbar without bakeout. The flanges for the effusion cells are all directed to the same position, namely the center a sample holder mounted on the manipulator in deposition position. Thus it is possible to employ co-evaporation from different cells. Close to the deposition position a quartz crystal micro balance is installed. A photograph of the OMBD chamber is shown in Fig. 4.3.

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<sup>2</sup>For example from Plano GmbH, <http://www.plano-em.de/>

<sup>3</sup>Sputtering of aluminum is possible, but will result in a diffuse structure.

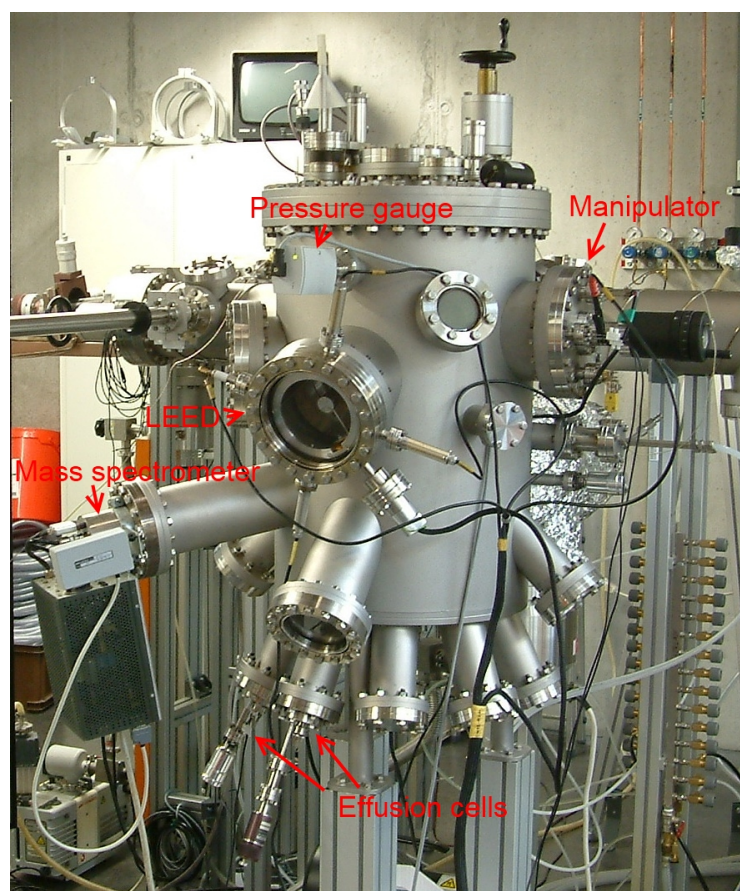


Figure 4.3: OMBD Picture

This is a photograph of the OMBD chamber. The manipulator is mounted on the right. Also the pressure gauge, the LEED optic and the mass spectrometer can be seen. The flanges in the bottom are intended for effusion cells. When this photograph was taken, only two effusion cells were used in the OMBD chamber.

### 4.3.1 OMBD manipulator

To fulfill the requirements of organic thin film deposition a custom made sample manipulator was constructed. In an molecular beam deposition process the substrate temperature influences the film growth. For characterization purposes it is also beneficial to allow for sample rotation. The samples on the manipulator should therefore be:

- heatable
- coolable



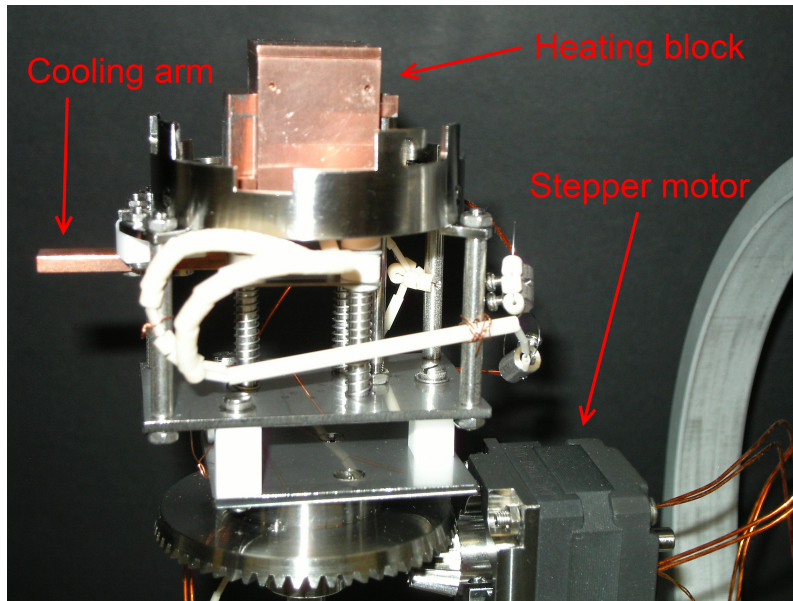


Figure 4.4: OMBD manipulator head

Photograph of the OMBD manipulator. The copper arm at the left side provides contact to the cooling block. The resistive heating wire is coiled up within the copper block electrically isolated from the copper with thin ceramic tubes. The thermocouple is clamped between the heating block and the bottom plate. When a sample is mounted onto the manipulator, three springs are used to press the heating block to the back of the sample holder to provide mechanical stability and good thermal contact.

- at a stable temperature during deposition
- rotatable perpendicular to the surface

The manipulator is mounted on a CF-150 flange with a centric CF-40 port for a rotational feed through and four CF-16 ports. The head of the OMBD manipulator is depicted in Fig. 4.4. It is attached to the rotational feed through. In this way a sample holder mounted on the manipulator can be rotated by up to  $360^\circ$  to all required positions, from the transfer position to the deposition position, in front of a LEED optic or to a view port at the top of the chamber. A UHV stepper motor inside the chamber is attached to the rotational feed through. With a use of a bevel gear it allows to rotate the manipulator head perpendicular to the rotational feed through by more than  $\pm 180^\circ$ , limited by the electrical wiring. This allows for an effective use of the LEED optic and furthermore minimizes shadowing effects during device preparation, since the mask can be aligned with respect to the effusion cell used for deposition.

Since the effusion cells are arranged in a semi circle around the bottom of the chamber tilted under an angle of  $30^\circ$  towards the sample position, the area which is coated through the shadow masks depends on the orientation of the sample holder.

The CF-16 flanges on the manipulator port are used for the electrical wiring of the stepper motor, the sample heater, the thermocouple feed through and a "claw" which can fix the manipulator head against an undesired rotation during transfer.

A cooling mechanism for the manipulator head is attached to a second flange at the top of the chamber. A liquid nitrogen feed through is mounted on a z-travel flange. The liquid nitrogen passes through a cooling block with a Cu arm which can be brought into contact with an analogous Cu arm attached to the manipulator head. This allows for cooling of the sample down to about  $-60^\circ\text{C}$ .

The central element of the manipulator head is a heating block made from Cu with bores for a resistively heated Tungsten wire and a type K thermocouple at the bottom for temperature measurement. This block is brought into contact with the sample holder with springs at the backside. In this manipulator assembly temperatures up to  $580^\circ\text{C}$  were achieved. When not in contact with the cooling mechanism the manipulator head is thermally and electrically isolated from the chamber by Macor<sup>4</sup> cubes.

### 4.3.2 Effusion cells for organic materials

Effusion cells are a standard tool for physical vapor deposition of thin films in UHV systems. They consist of a crucible filled with the material to be evaporated and a heating system - often a heater wire - wound around the crucible. Usually a temperature sensor is also integrated and radiation shields are attached. To deposit organic molecules temperatures in the region from  $80^\circ\text{C}$  to  $500^\circ\text{C}$  are sufficient. Effusion cells of different designs were developed and used in this work depending on the organic material. Important points for organic effusion cells are a very accurate and stable temperature control, short relaxation times and good temperature uniformity along the cell. The last point here is the hardest to verify, but can be very important. If the top of the cell is too cold, condensation of source material can take place which will reduce and eventually block the molecular flow. This was observed with CuPc for different cell designs. Furthermore, some molecular species only evaporate close to the point of decomposition or the deposition rate has a very strong

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<sup>4</sup>MACOR is a machinable glass-ceramic from Corning Incorporated (<http://en.wikipedia.org/wiki/MACOR>).



temperature dependence. Here it is especially important that the temperature is uniform in the lower part of the cell. All cells are mounted to CF-40 flanges and are temperature controlled with a PID controller from Eurotherm.

### **Effusion cell with tungsten wire**

The first prototype effusion cell was build for pentacene deposition with a working temperature of around 200 °C. A tungsten filament was coiled with a lathe and wound up upon an Al<sub>2</sub>O<sub>3</sub> tube. Inside the tube a crucible made from Al<sub>2</sub>O<sub>3</sub> with 8 mm inner diameter and 100 mm length was suspended in a steel cage. Temperature was measured at the bottom of the crucible at the steel cage with a type K thermocouple. The cell was equipped with two radiation shields and a shutter. In test runs temperatures up to 900 °C could be achieved. Temperature stability was good (< 0.1 °C with adjusted PID parameters), but relaxation times during cooling at low temperatures were quite long (e.g., about 1 h to cool from 200 to 150 °C). After heating to high temperatures it was impossible to remove the radiation shields without damaging the cell. Therefore the state of the tungsten filament, e.g. whether the windings are still uniformly distributed along the tube, could not be checked. A second version of this cell is similar to the first one, but the filament is only supported by three thin Al<sub>2</sub>O<sub>3</sub> capillaries instead of the massive tube. This reduced the relaxation time. In this cell type the filament lacks support at the top winding. Due to the weight of the filament the distance between the coils at the top gradually increases over time of usage. Consequently, the top of the crucible remains cooler than the lower part of the cell. This was detected by condensation of CuPc at the top of the cell.

### **Effusion cell from graphite rod**

The second type of effusion cell was build from a graphite rod with a bore in the center. The evaporation material is filled into the bore and a current is applied along the graphite rod from the baseplate to a clamp at the top. A thermocouple is attached to the bottom of the rod and a radiation shield can be mounted to the baseplate. This cell type has a higher temperature uniformity except for the clamp region at the top, but this part can be additionally heated by a short Tungsten filament to avoid condensation of source material at the top of the cell. A small drawback of this cell type is the contamination of the cell with the source material, therefore only one kind of molecular species should be used with such a cell.

## 4.4 Contact preparation chamber

The contact preparation chamber is based on a standard 150CF double cross. It has a view port at the front, an elbow with a port for the manipulator at the back, a custom made flange for the shadow mask handling at the top and a cluster flange with four ports at the bottom. The left and right ports are reserved for sample transfer from the transfer module and to the sputtering chamber. The flange at the bottom is equipped with an effusion cell (gold) and a pressure gauge. If necessary a second effusion cell with a different contact material can be added. The manipulator head in this chamber can be retracted out of the double cross to allow for sample transfer through the contact chamber into the sputtering chamber. It has a special supporting mechanism which allows for linear travel and provides sufficient support for a large lever arm. The flange at the top of the contact preparation chamber has the shape of a pot mounted upside down. It has a 40CF flange in the top, where a wobble stick with a pincer is mounted, and supports a stage, where up to seven shadow masks can be stored. Mask storage is realized by cutouts in the stage, where the masks can be fixed vertically with the help of their spikes. Storage in the contact preparation chamber has the advantage of the lowest possible contamination of the various masks due to the low base pressure and gold as the only material which is evaporated in this chamber.

## 4.5 Sputter chamber

For the preparation of thin films by sputtering a separate chamber is used. This chamber is based on a CF-100 double cross and is connected to the UHV system via the contact preparation chamber. It is designed to host two sputter cathodes and a stage for plasma oxidation. During this work one cathode was used for the sputtering of aluminum and the other for the sputtering of  $\text{SrTiO}_3$ . A manipulator for the sputter process was designed with the aim to provide temperatures up to 900 °C in oxygen atmosphere. The chamber is pumped by a Pfeiffer turbo molecular pump in combination with a membrane pump. Pressure is measured by a Bayard-Alpert ionization gauge, a Pirani gauge and a capacitance gauge. Gas inlet for sputtering is realized by two needle valves, one for argon and one for oxygen, and mass flow controllers. The gas inlet is on the opposite site of the pumping system, so that the gases are forced to flow through the chamber along the manipulator and the sputter cathodes, which guarantees a homogeneous and stable plasma discharge.

### 4.5.1 Sputter manipulator

To successfully grow thin films of SrTiO<sub>3</sub> by sputtering an oxygen atmosphere and high temperatures are necessary. This poses special requirements for the manipulator and the used materials. Furthermore, the limited space in the sputter chamber and the transfer mechanism had to be considered. In Fig. 4.5 the sputter manipulator is depicted in different stages - from design till a test run in air.

Based on a x-y-z stage the manipulator head is mounted onto a rotational feed through. The manipulator head consists of an Inconel baseplate with a copper cooling plate on the back and the sample holder and heater at the front. The heater consists of a ceramic block with a Kanthal<sup>5</sup> wire supported by two Inconel pins. The pins additionally support two Inconel radiation shields separated by ceramic split bushes and are attached to the baseplate. The current to the Kanthal wire is fed through the Inconel pins. Due to the high temperatures a water cooling mechanism had to be designed. Since the sputter chamber is in line with the contact preparation chamber three transfer positions (the trolley in the transfer chamber, contact preparation and sputtering chamber) must be usable. This required an adjustable positioning of the manipulator head including the cooling mechanism. Cooling water is feed through a wound up copper pipe on a copper cylinder. The pipe can be moved linearly on the cylinder which is connected to the copper cooling plate on the back of the manipulator head. In this way the manipulator head can be moved linearly along the copper cylinder to allow for an adjustment of the sample transfer. The manipulator head is supported by a construction which allows for further fine tuning of the transfer in the other directions and supports the water cooling bellows. The temperature is measured with a type K thermocouple at the back of the inner radiation shield inside the manipulator head. The distance from the radiation shield to the heater block is the same as the distance from the heater to the sample holder. Nevertheless, the measured temperature  $T_m$  is not necessarily the same as the sample temperature  $T_s$ . Effects which could lead to a temperature difference are

- cooling from the manipulator backside can lower the measured temperature:  $T_m < T_s$ .
- radiation shielding from the second radiation shield could increase the measured temperature:  $T_m > T_s$ .

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<sup>5</sup>Kanthal is an alloy of mainly iron, chromium and aluminum which is able to withstand high temperatures in oxygen or UHV conditions. However, before its first use in vacuum it must be heated under oxygen atmosphere to allow for the formation of an oxide protection layer. It is manufactured by Sandvik AB (<http://www.kanthal.com/>).

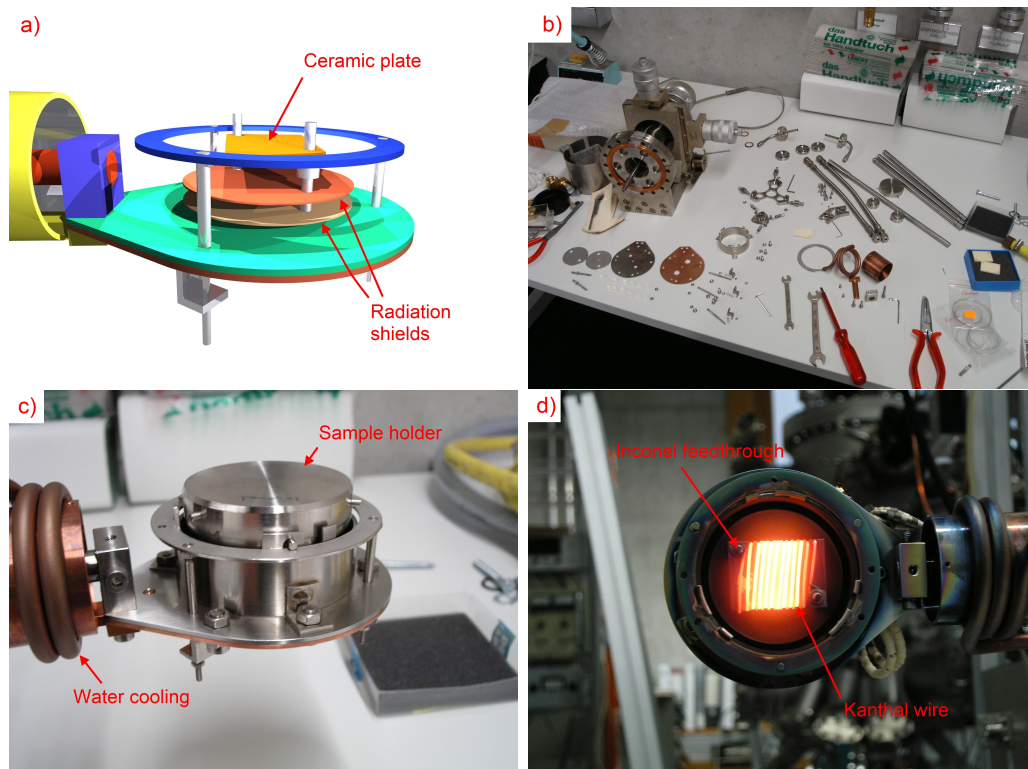


Figure 4.5: Sputter manipulator

Different stages in the design and construction process of the sputter manipulator. First a 3D construction model (a) of the sputter manipulator was developed. The sample mount is not depicted in this model to allow a view of the interior of the manipulator head and the radiation shields. The ceramic plate (orange) serves as the support for the heating wire. The second picture (b) shows the cleaned parts before assembly. On the next photograph (c) the manipulator is semi assembled and equipped with a sample holder. The water cooling pipe is wound up on the cylinder which is connected to the cooling plate. The wiring for the temperature measurement and heating is still missing. The last picture (d) shows a heating test in air after a heating filament change. At this stage the manipulator was already used multiple times, as can be seen from the staining.

- heating from the sputter process can increase the sample temperature stronger than the reference temperature:  $T_m < T_s$ .
- gas flow can decrease the sample temperature stronger than the reference temperature:  $T_m > T_s$ .
- different sample holders can have different absorption/emission coefficients which leads different temperatures since radiation heating is used:  $T_{s1} \neq T_{s2}$ .

The temperature of a sample holder on the sputter manipulator was measured once with an infrared thermometer through a UHV view port and compared to the temperature measured with the thermocouple from 0 – 14 A (at 0 – 22.1 V). The maximum temperature measured with the thermocouple was 946.1 °C in vacuum. The temperatures measured with the infrared thermometer depend on the preset emission coefficient. With an emission coefficient of 0.4 the measured values were in the same temperature range. Since emissivity varies as a function of temperature and surface finish the exact values are very hard to determine, therefore these measurements should be considered a rough estimate.

During the usage the manipulator was slightly modified and repaired multiple times. The Kanthal wire was exchanged and the current leads from the flange to the manipulator head were upgraded to allow for larger currents. Presently the maximum current is limited due to the UHV current feedthrough to 15 A. With this configuration temperatures close to 900 °C (nominal) in oxygen atmosphere can be reached.

## 4.6 Load lock

A load lock chamber is used in the multiple chamber UHV systems to provide sample access. It is based on a 100CF double cross. It is equipped with a rotary feedthrough, a current feed through and a full range pressure gauge. The rotary feedthrough is motorized and supports a stage where up to three sample holders can be mounted. With the current feedthrough a radiative sample heater is realized, using a tungsten filament from a halogen lamp and a reflector, formed from a stainless steel sheet. The heating mechanism is mounted to the flange opposite to the gate valve which provides access to the transfer module. It can heat one sample at a time and is calibrated up to 400 °C. With a computer program the motor on the rotary feed through can be controlled, which allows for bake out of up to three samples over night.

## 4.7 Small MBE and test chamber

Additionally to the chambers described above a small MBE chamber system and a test chamber was set up.

### 4.7.1 Test chamber

The test chamber was used to obtain sublimation points for different source materials and to further study the effusion and temperature characteristics for different effusion cells. It can also be used to purify source material without contaminating the OMBD chamber. It consists of a CF 150 tube with an elbow to the pumping system at the one end and a gate valve for easy access at the other. The main body has three more ports, one at the top, where a window was used to observe the sublimation experiments, one at the bottom where effusion cells can be mounted and one at the left side where a sample holder and the vacuum gauges are mounted. The effusion cells were usually mounted on a telescopic bellow so that different distances can be realized to the substrate. As substrate microscope slides were used. They can be placed on a frame type holder which can be moved horizontally to be able to prepare multiple deposits without intermittent venting of the chamber for substrate change. Due to the short distance between substrate and effusion cell this system is ideally suited to determine sublimation points. The deposition rates are higher and the view on the glass slides is much better compared to a sample in the OMBD. Furthermore, the crucible of the effusion cell can be removed whenever the chamber is opened for a substrate change. This allows to control the (filling) state of source material, which in the case of organic materials is very important because it can decompose under too high temperatures. The test chamber is pumped by a turbo molecular pump in combination with a rotary vane pump, which due to the small volume of the chamber, allows for a short pump time. A detailed description of the experiments performed in the test chamber can be found in Kerstin Keller's thesis [52].

### 4.7.2 Small MBE

In the small MBE chamber the effusion cell designs were tested and pentacene samples were prepared. This setup, realized early on in this thesis work, consisted already of two chambers separated by a gate valve and a transfer system. A CF100 double cross was used as load lock and a CF150 double cross as the evaporation chamber. The system was used in conjunction with a transferable and heatable sample holder of our own design, which was tested till 400 °C. Pumped with a combination of turbo molecular pump and a rotary vane pump

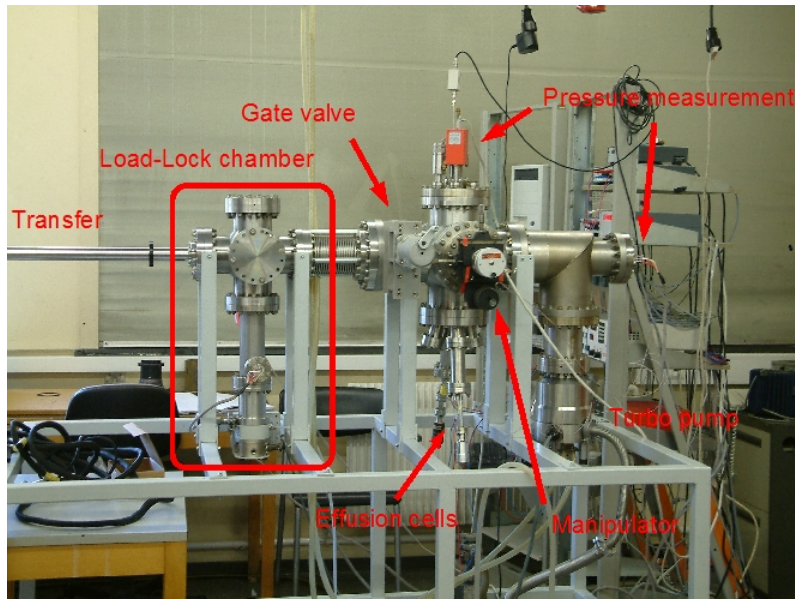


Figure 4.6: Small MBE

Photograph of a the test chamber system used for the growth studies of pentacene. This system was a two chamber system with a load lock and preparation chamber. It was pumped with a turbo molecular pump in conjunction with rotary vane pump via the elbow at the right side.

it reached a base pressure in the range of  $10^{-9}$  mbar in the deposition chamber. The chamber system is shown in Fig. 4.6 and the transfer mechanism is illustrated in the picture series in Fig. 4.7. This sample holder is not compatible with the BESTEC design and is not used anymore. The chamber system was dismantled and the parts were re-used for the contact preparation and sputtering chamber presently in use.

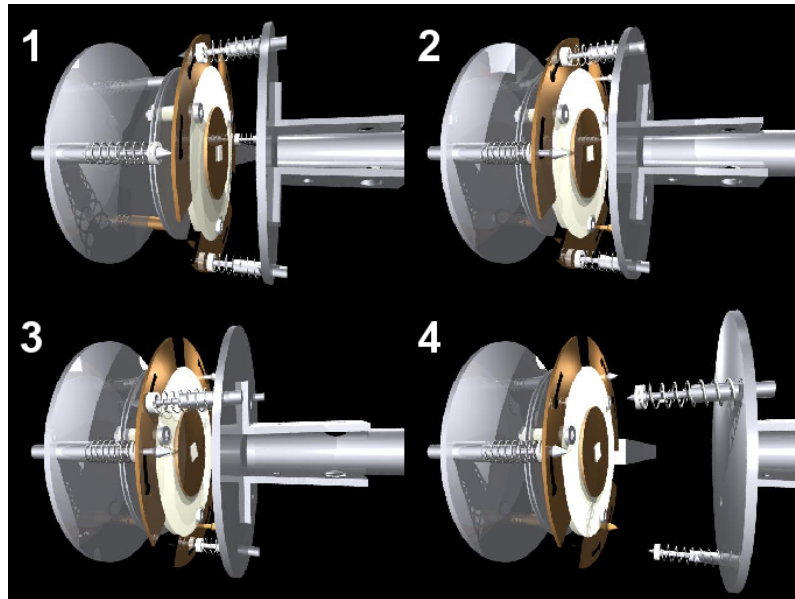


Figure 4.7: Transfer mechanism in the small MBE chamber

This rendered picture series (1 to 4) illustrates the transfer mechanism. The sample holder is secured on a transfer rod. By pushing and turning the holder is unlocked on the rod and locked on the manipulator. Afterwards the transfer rod is removed. Sample transfer to the rod works in the same way in reverse order. The series is based on the sample holder designed for the test chamber, but the principle for the current sample holders is the same.



## Chapter 5

# Organic thin film deposition and characterization

In this chapter the study of the growth processes of the organic layers is described. The deposition experiments were carried out in the OMBD chamber and the small MBE chamber. The temperature of the effusion cells and the substrate was controlled with Eurotherm PID-controllers. The effusion cells were kept at a constant standby temperature 50 – 250 °C below deposition temperature, depending on the material. Before deposition the desired substrate temperature was adjusted with the heating system of the manipulator. During deposition the temperature of the effusion cell was then ramped up and after a certain waiting time the shutters were opened. The temperatures of the manipulator and the effusion cells, the pressure in the chamber and the deposition rate on the quartz micro balance were routinely recorded with a computer program. Changes in the deposition rate or, e.g., an unusual chamber pressure could then be detected easily. The small molecules which were studied are pentacene, chlorinated copper phthalocyanine and copper phthalocyanine. Substrates used for deposition were mainly  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> a-plane, r-plane and random cut, where random cut was routinely used for thickness calibration experiments. The batch of randomly cut  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> substrates was in our case quite close to the r-plane cut.  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> was chosen since it is stable, of high crystalline order, non-reactive and cheap. Since the field-effect transistor structures were deposited on SrTiO<sub>3</sub>, also SrTiO<sub>3</sub> (001) substrates were used. Prior to deposition the substrates were ultrasonically cleaned with acetone and isopropanol and glued onto a sample holder with conductive silver paint. They were heated in the load lock chamber for a minimum of 2 h<sup>1</sup> at 400 °C to remove residual water and volatile contaminations.

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<sup>1</sup>Often the samples were heated during the night.

After deposition the samples were analyzed with X-ray diffraction (XRD) and an optical microscope.

In the following sections the experiments and results of pentacene, chlorinated copper phthalocyanine and copper phthalocyanine are reported.

## 5.1 X-ray diffraction

The thin films prepared during the growth studies were measured on different X-ray diffractometers. Since this work started in an early phase of establishing the group and the equipment was in the build-up phase there was initially no diffractometer available. For the first studies the machines in the group of Prof. Dr. Aßmus (University of Frankfurt), a diffractometer mainly used for powder measurements, and Prof. Dr. Adrian (University of Mainz) were used, mainly for pentacene samples.

Later a new D8 diffractometer from Bruker AXS (Fig. 5.1) was acquired and since then all films were measured on this system. It is specially designed for thin film measurements. It is equipped with a Göbel mirror which provides a parallel beam, a motorized sample stage for precise adjustment of the samples. The samples are mounted on three circles including an Eulerian cradle and the diffractometer can be setup for in-plane measurements, when the X-ray tube is rotated  $90^\circ$  with respect to the beam axis. On the detector side a single-bounce germanium monochromator or a variable slit can be used.

The X-ray diffractometer was used to measure the thickness with high accuracy and to determine information about the crystal structure and orientation of the thin films on the substrates. Routinely, a reflectivity scan (XRR), a Bragg scan and - if a Bragg peak was detected - a rocking curve measurement were performed. For all measurements a precise alignment of the diffractometer and the sample were necessary. The sample holder of the diffractometer is equipped with two small cradles. Utilizing a laser the cradles were used to adjust the surface normal of the sample along the axis of the  $\phi$ -circle.

Bragg peaks are detected when Bragg's law [80]

$$2d \sin \Theta = n\lambda \quad (5.1)$$

is fulfilled. From the wavelength of the X-ray radiation, Cu  $K_\alpha$  with a wavelength of  $1.54 \text{ \AA}$  and the detected  $2\theta$  angle the distance between the lattice planes can be determined.

There are two possibilities to determine the thickness of thin films with X-rays. The first are the Kiessig interference fringes, the second are Laue oscillations. Kiessig fringes appear under small angles as interference of the beams reflected on the film and the substrate surface. This can be described with the Fresnel

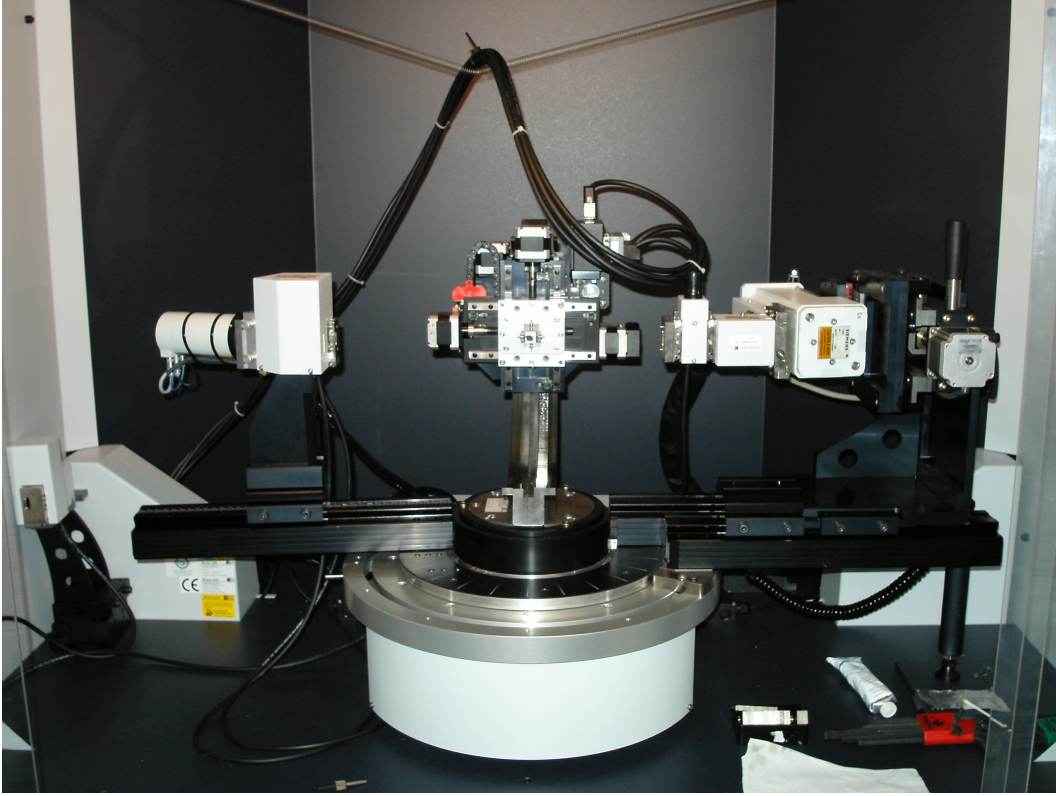


Figure 5.1: X-Ray diffractometer

The X-ray diffractometer D8 from Bruker AXS. The sample is in the center of the sample stage mounted on a small holder. The X-ray tube is on the right side, the detector on the left.

equations [81]. Kiessig fringes was the preferred method to determine the film thickness.

The associated reflectivity scan was performed in a  $2\theta$  range of  $0.1$  to  $5^\circ$  with the incident angle equal to the reflected angle. When Kiessig fringes were detected the commercial Leptos software from Bruker AXS was used to fit the curves and obtain thickness and roughness values. When the films were too rough no Kiessig fringes appeared, but sometimes Laue oscillations around the Bragg peak could be detected. In this case the distance between two peaks could be used to fit the film thickness  $d = N \cdot a$  via

$$d = \frac{\lambda}{2(\sin \Theta_i - \sin \Theta_{i-1})}, \quad (5.2)$$

where  $\Theta_i$  and  $\Theta_{i-1}$  are the positions of the maxima,  $N$  is the number of lattice planes and  $a$  is the lattice plane distance. With the measured thickness the

deposition rate during preparation could be determined and the thickness of further films could be adjusted by adapting the deposition time.

When Bragg peaks were detected, a rocking curve was used to further study the thin film quality. In this type of scan the detector was positioned at the angle of the Bragg peak and the  $\omega$  circle was scanned. From the intensity and width (FWHM) of this scan information about the mosaicity of the thin film was obtained. A small rocking curve width showed that the lattice planes were oriented in the same direction, whereas a large widths showed a tilt of the lattice planes with respect to each other.

When the lattice planes of the film were tilted with respect to the substrate, the maximum of the rocking curve was shifted to an angle different from  $2\theta/2$ . The position of the detector was then adjusted accordingly to refer to the film's lattice planes normal rather than to the substrate's normal and a second Bragg scan was performed.

## 5.2 Optical microscopy

A microscope from Leica working in reflection mode was used for optical characterization of the films. It allows for a magnification up to a factor of 1000 and is equipped with a camera and interference contrast setup (prism and filters). The microscope proved very useful, especially for the judgment of the sputtered SrTiO<sub>3</sub> films. Here it was often hard to come to a conclusion from the X-ray data alone. For the organic layers the magnification was sufficient to reveal details in case of micro crystalline film growth.

## 5.3 Pentacene

Commercial pentacene without further purification was the first material used in the small MBE-chamber system and could be easily evaporated at 200 °C. Comparing the filling level of the effusion cell before and after a series of depositions, the source material consumption was determined to about 1.25 cm<sup>3</sup> of pentacene for 15 films. The thin films of pentacene grown on  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> a-plane showed very sharp Bragg peaks (comp. Fig. 5.2) when measured with X-ray diffraction. Exclusively the thin film phase in (00*l*) orientation with a *d* value of 15.4 Å was found (comp. section 2.4). The films appear lilac - with an optical microscope no structure was visible. In Fig. 5.3 the different peak positions from the powder diffractogram and the thin film phase are shown. The best films showed peaks up to the fifth order and a resolution-limited rocking curve width (FWHM) of 0.019° of the (001) peak. XRR measurements showed no

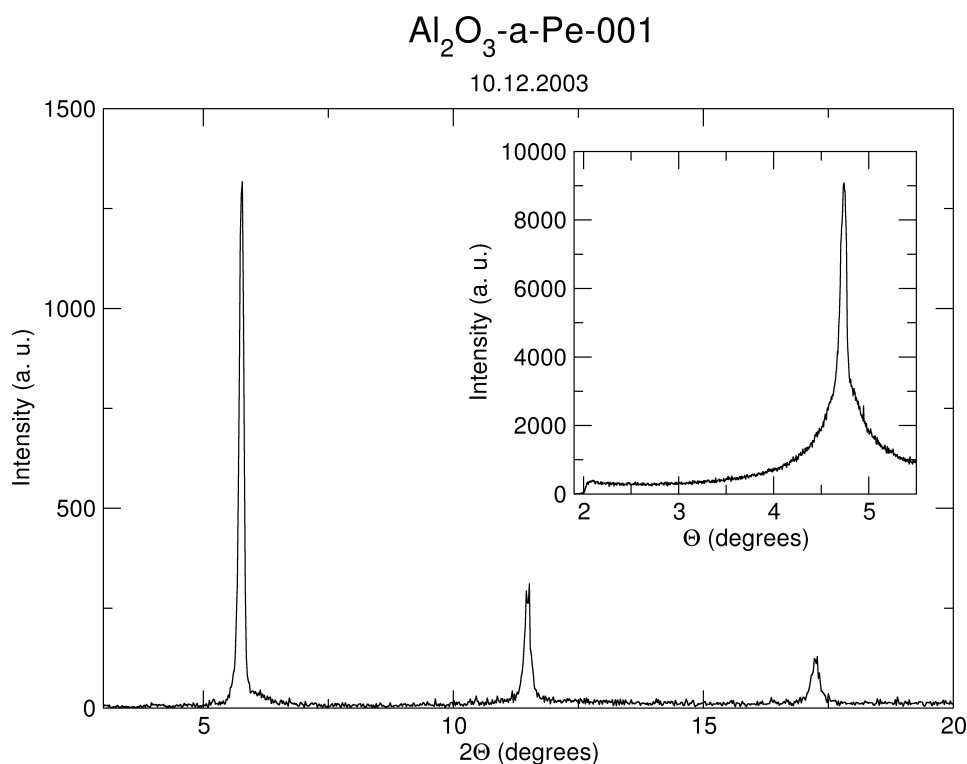


Figure 5.2: The very first pentacene film in our group

This is the Bragg scan of the very first organic thin film prepared in our group. It is a pentacene film on an  $\alpha$ - $\text{Al}_2\text{O}_3$  a-plane substrate. The first three reflexes of the (00 $l$ ) order appear as sharp peaks. The insert shows a rocking curve of the (001) peak. The FWHM of the rocking curve is about  $0.09^\circ$ . This film was prepared in the small MBE system.

Kiessig fringes. The thickness of the films could therefore only be estimated from Laue oscillations. Different substrate temperatures and their influence on the growth process were studied (comp. Fig. 5.4). The temperature series showed no shift in  $d$  value from 305 K to 350 K. The film at 330 K had the sharpest rocking curve and also the highest peaks in the Bragg scan. The fit from the Laue oscillations yielded a thickness of 59 nm.

In conclusion, highly ordered thin films of pentacene have been prepared on  $\alpha$ - $\text{Al}_2\text{O}_3$  substrates. All films grew in the thin film phase in (00 $l$ ) orientation, as known from literature [42]. The highest crystallinity and order could be obtained at a substrate temperature of 330 K. The growth of pentacene was sufficiently established for the preparation of thin film field-effect transistors.

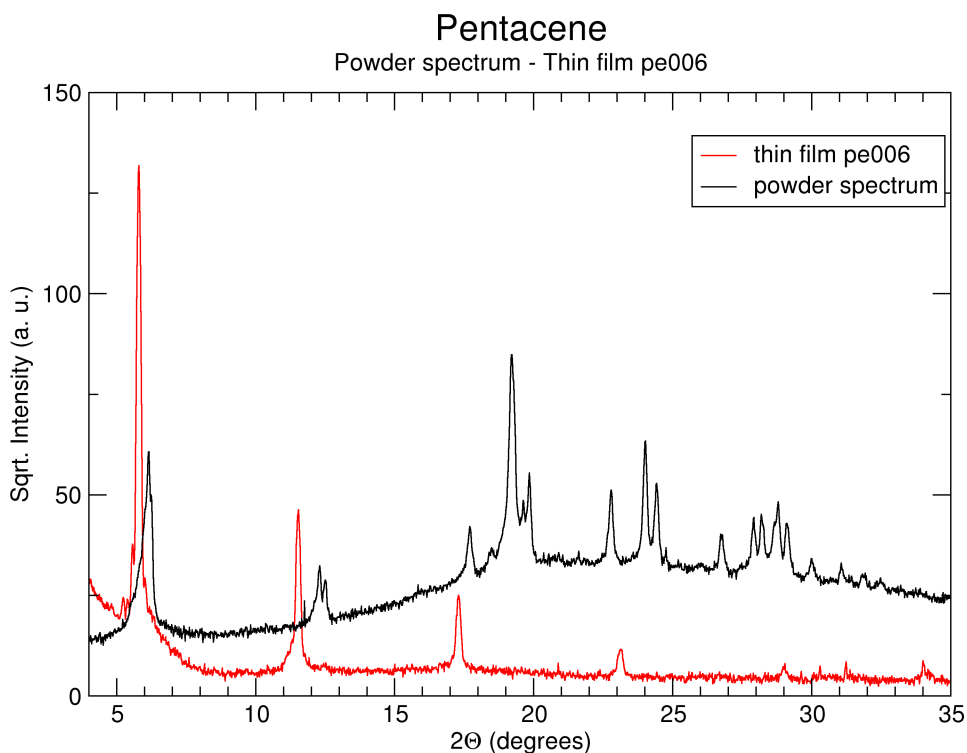


Figure 5.3: Comparison of thin film and powder spectrum

Here the Bragg scan of the pentacene film pe006 is compared to a powder spectrum. The difference in the  $d$  value  $d_{\text{film}} = 15.4 \text{ \AA} > d_{\text{bulk}} = 14.5 \text{ \AA}$  can be easily detected.

## 5.4 Per-Chlorinated Copper Phthalocyanine

Chlorinated copper phthalocyanine ( $\text{Cl}_{16}\text{CuPc}$ ) is a derivative of copper phthalocyanine where some or all of the hydrogen atoms are replaced by chlorine atoms. This increases the electron affinity of the molecule and it was therefore interesting if it could be used as an electron acceptor in charge transfer compounds. Since  $\text{Cl}_{16}\text{CuPc}$  is used as a green pigment in commercial dyes it was readily available in the chemistry department. The source material from the manufacturer Clariant<sup>2</sup> was provided by Prof. Dr. Martin Schmidt. Due to the exchange of hydrogen with chlorine atoms the molecular weight increases, which leads to a higher evaporation temperature as compared to  $\text{CuPc}$  [82]. The first trials were conducted in the test chamber. A first green deposit was observed at a cell temperature of  $460 \text{ }^\circ\text{C}$ , but in subsequent trials no deposit could be observed at this temperature. It is assumed that impurities resulting

<sup>2</sup>[www.clariant.de](http://www.clariant.de)

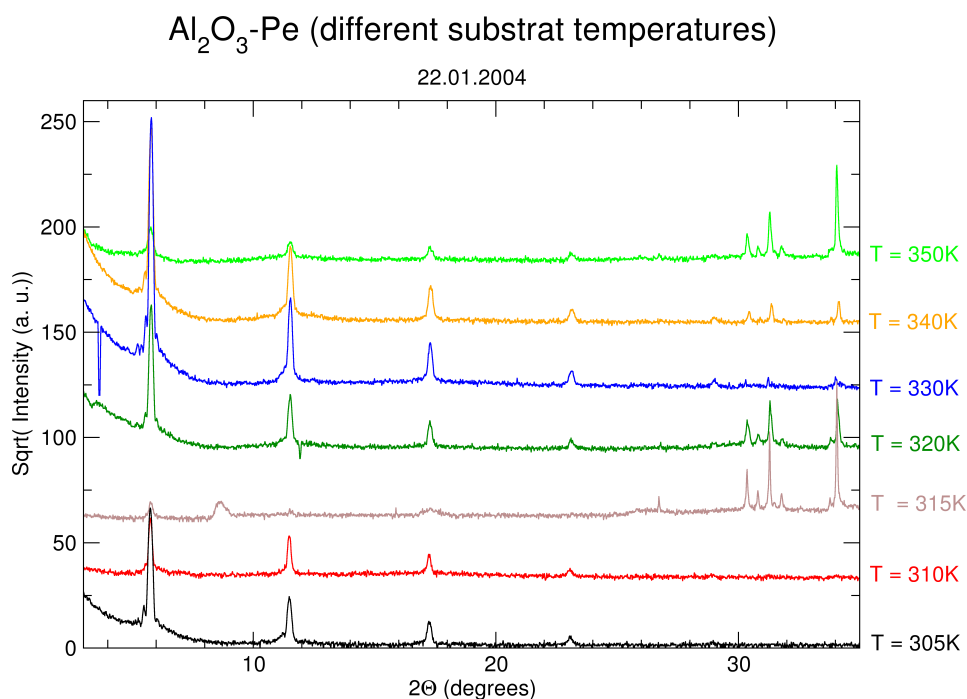


Figure 5.4: Series of pentacene films with different substrate temperature

These are the Bragg scans of an experimental series where the substrate temperature was varied, as indicated on the right. The scans are shifted in y-direction for better readability. The pentacene films were deposited with a nominal effusion cell temperature of 200 °C on  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> a-plane substrates. The deposition time was 1 h for each film.

from not fully chlorinated and therefore lighter molecules were responsible for the first deposit. The cell temperature was subsequently increased to 560 °C where a relatively thick deposit was observed after two hours. The effusion cell was then installed in the OMBD chamber. In the next experiments it was attempted to calibrate the deposition rate. It was possible to measure the film thickness of the Cl<sub>16</sub>CuPc films with XRR as for example shown in Fig. 5.5. It turned out that a proper deposition rate versus temperature calibration was not possible since the rate was not stable and decreasing from one deposition to the next. This was observed by thickness measurements with XRR of the thin films and by a decreasing rate at the quartz micro balance and a decrease of the pressure in the chamber during deposition. It was also observed that the crucible of the effusion cell was clogging from source material. Cl<sub>16</sub>CuPc was the first material where such an effect was found - here the effusion cell

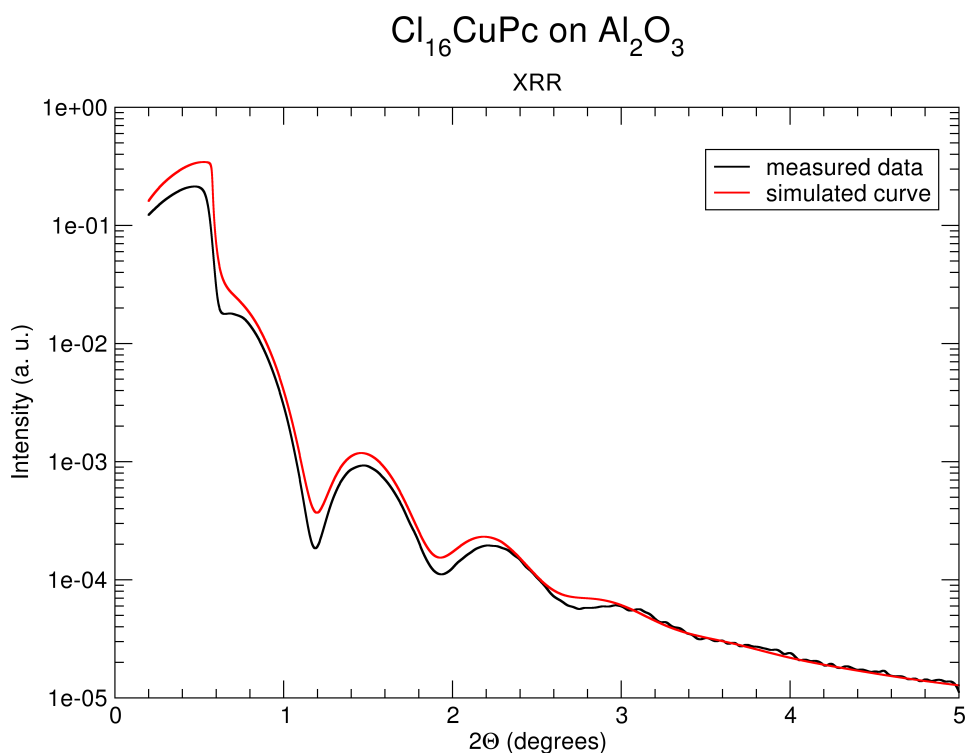


Figure 5.5: XRR result of a  $\text{Cl}_{16}\text{CuPc}$  film

Small angle X-ray diffraction of an  $\text{Cl}_{16}\text{CuPc}$  thin film on an  $\alpha\text{-Al}_2\text{O}_3$  substrate. The film was deposited with an effusion cell temperature of  $580\text{ }^\circ\text{C}$  for 2 hours. Substrate temperature was  $30\text{ }^\circ\text{C}$ . The fit provided a film thickness of about 12 nm.

temperature of  $560\text{ }^\circ\text{C}$  and therefore also the temperature gradient within the cell were significantly higher as compared to pentacene growth with an evaporation temperature of  $200\text{ }^\circ\text{C}$ . A new cell design with a lower temperature gradient within the cell was necessary. This led to a detailed study of temperature and evaporation properties of effusion cells and the development of effusion cells made from a graphite rod [52].

Since the deposition rate of  $\text{Cl}_{16}\text{CuPc}$  was not stable, it was presumed that the material might have been contaminated by volatile organic compounds. Therefore, attempts to purify the source material before usage in the OMBD chamber were undertaken. A sublimator was used for the purification but the yield was relatively poor and the source material partially changed color from green to black. This was a first hint of a possible decomposition of the material.

In parallel a second test run was started in the test chamber. A stainless steel



lid was added to the crucible to modify the cell into a Knudsen cell type [83]. This resulted in several deposits with different colors from white at 500 °C to red/brownish at 530 °C and some greenish/yellow at 560 °C. After this test run the stainless steel lid was corroded on the inside and of black appearance. The source material had also changed to a dark black color, but was still green when pulverized. Also, on effusion cell and manipulator of the OMBD chamber corrosion was observed after the experiments with  $\text{Cl}_{16}\text{CuPc}$ . It was concluded that chlorine must be released from the  $\text{Cl}_{16}\text{CuPc}$  and react with the metals and residual water vapor. To prevent further damage in the vacuum chambers further experiments with  $\text{Cl}_{16}\text{CuPc}$  were stopped for the time being. The effusion cell was removed from the OMBD chamber.

## 5.5 Copper Phthalocyanine

After the experiments with  $\text{Cl}_{16}\text{CuPc}$  copper phthalocyanine was used as source material. It was evaporated in the OMBD chamber and the deposited films were studied with X-ray diffraction. The source material was commercial CuPc and it was used without further purification. For later experiments it was mixed with quartz sand to prevent a possible agglutination of the source material which might reduce the deposition rate.

The first evaporation experiments were conducted with a effusion cell with a tungsten wire (second version). Similar to the experiments with  $\text{Cl}_{16}\text{CuPc}$  it turned out that the temperature at the top of the crucible during deposition was so low that undesired adsorption and recrystallisation of the source material occurred till the cell was almost closed<sup>3</sup>. This prevented stable deposition rates which were determined with a quartz micro balance close to the sample holder and compared to the thickness determined with XRR measurements (comp. Fig. 5.6, 5.7). For the next depositions a new effusion cell made from a graphite rod was used, but this cell was still prone to clogging due to the metal contact at the top.

In the subsequent experiments with a graphite effusion cell with an additional filament at the top recrystallisation could be prevented (comp. Fig. 5.8). The deposition rates observed with the quartz micro balance were fluctuating, even at nominally stable effusion cell temperatures. The graphite cells had their thermocouple fixed directly to the base of the graphite rod with a small screw. Therefore a change in the heating current and voltage caused a feedback to the thermocouple. This easily created fluctuations for the temperature controller. To prevent these fluctuations during deposition the cell was operated in a constant current mode. For a stable deposition rate this current had to be

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<sup>3</sup>Nominal temperature was 400 °C

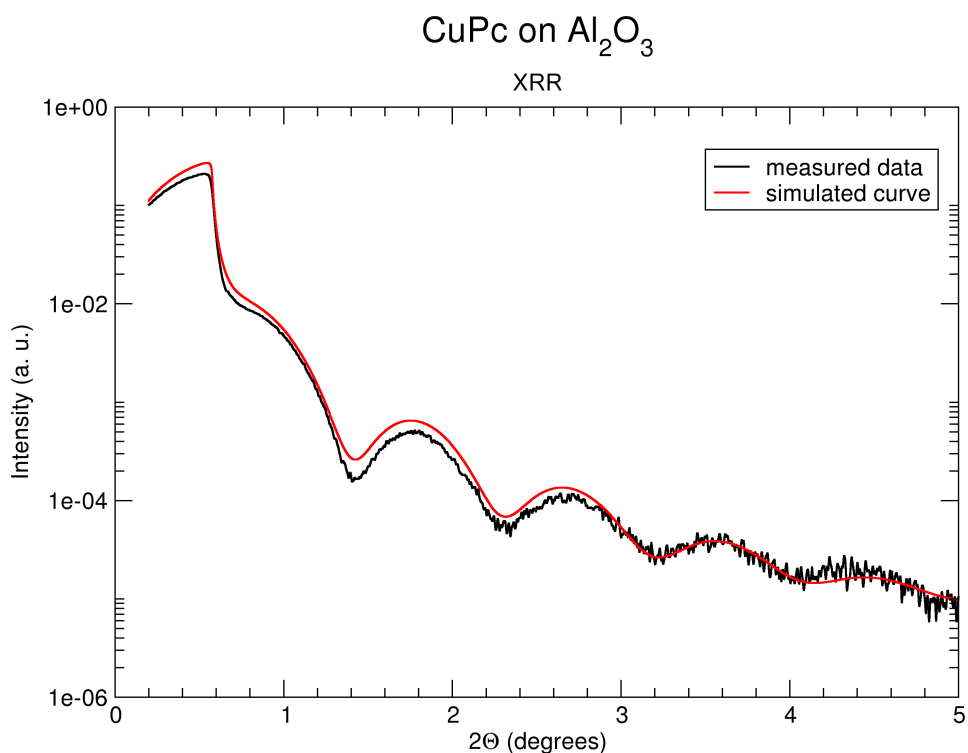


Figure 5.6: XRR result of a CuPc film

Small angle X-ray diffraction of the first CuPc thin film prepared in the OMBD chamber on an  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> substrate. The film was deposited with an effusion cell temperature of 380 °C for 310 minutes. Substrate temperature was 30 °C. The fit yielded a thickness of about 10 nm.

increased for consecutive depositions. To allow for a better comparison of the different films not the duration of the deposition but the accumulated thickness on the quartz micro balance was used as reference. The typical thickness of the films was about 25 nm with deposition time of about 300 minutes.

The influence of the substrate temperature on the growth of CuPc on  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> was studied in the range from room temperature to 140 °C. Here a difference in growth behaviour could be observed with X-ray diffraction. The films changed with increasing substrate temperature from smooth, with small angle oscillations, and only a small Bragg peak to higher crystallinity, with a larger Bragg peak and a rougher surface with few or no small angle oscillations. The behaviour is depicted in Fig. 5.9 for three different temperatures. The thickness of the deposited films was measured either with a fit of the small angle oscillations or a fit of the Laue oscillations of the Bragg peak.

## CuPc-070712

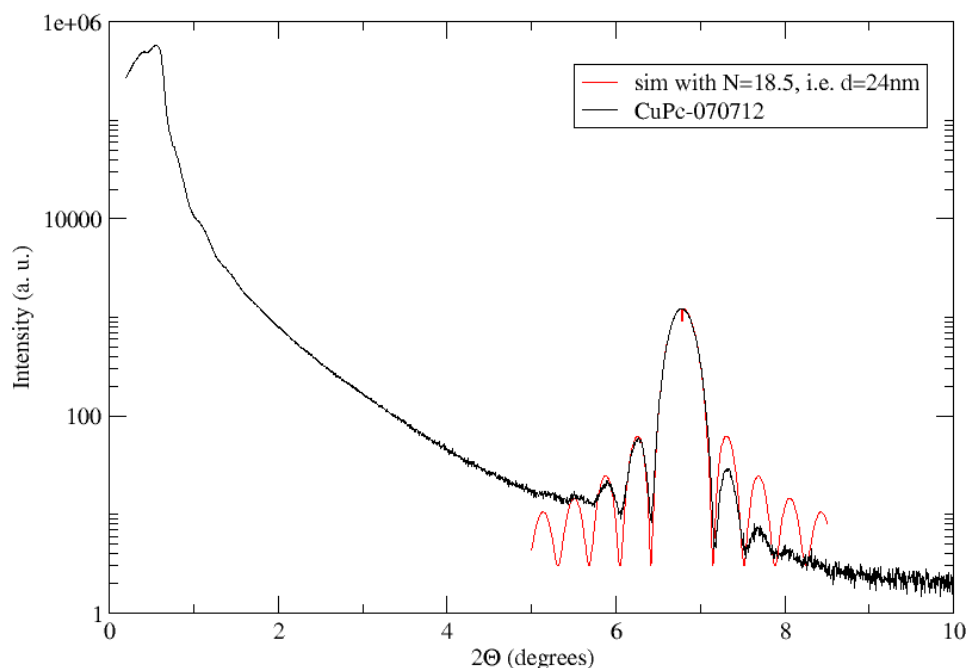


Figure 5.7: XRR result of a CuPc film on SrTiO<sub>3</sub>

Small angle X-ray diffraction of the CuPc thin film 070712 prepared in the OMBD chamber on a SrTiO<sub>3</sub> (100) substrate. The film was deposited with an effusion cell temperature of 365 °C for 265 minutes. Substrate temperature was 140 °C. The fit to the Laue oscillations provided a thickness of about 24 nm.

To study the influence of substrate properties on the growth several films were prepared on different substrates. To ensure equal deposition conditions the substrates were mounted onto one sample holder and all substrates were prepared simultaneously within one deposition process. Thin films of CuPc on SrTiO<sub>3</sub> substrates showed very similar X-ray results to  $\alpha$ -Al<sub>2</sub>O<sub>3</sub>, as depicted in Fig. 5.10. The orientation of the CuPc molecules with respect to the substrate depends on the relative strength of the molecule-substrate interaction compared to the molecule-molecule interaction. On a crystalline metal substrate, where the interaction is strong, CuPc molecules lie on the substrate, while on less interacting or rough substrates the molecules stand on the substrate [84]. Aluminum oxide is considered a weakly interacting substrate, where molecules from the CuPc family, like for example copper hexadecafluorophthalocyanine (F<sub>16</sub>CuPc) are standing on the substrate [85].

The Bragg peaks were detected for all films and substrates at an angle of

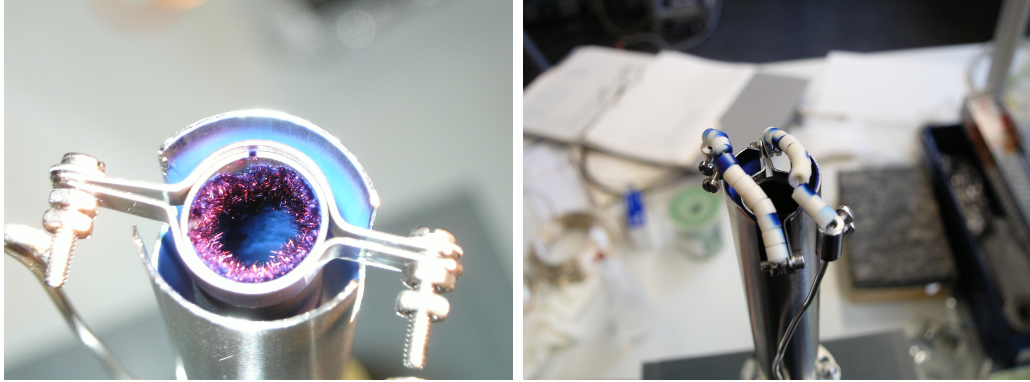


Figure 5.8: Clogged CuPc cell and cell with additional heating filament

The CuPc cell on the left photograph suffered from recrystallization of the source material at the top which lead to clogging and a reduction of the deposition rate. The cell on the right shows a modified version of the cell design with an additional tungsten wire, isolated by ceramics to increase the temperature at the top and prevent the clogging.

$2\theta=6.8^\circ$  which corresponds to a distance between molecular planes of 1.3 nm. Rocking curves of the Bragg peak resulted in resolution-limited FWHM of  $0.015^\circ$ . The Bragg peak is in agreement to the (200) plane of the  $\alpha$ -phase of CuPc. The  $\alpha$ -phase is frequently reported in literature for vacuum deposition of CuPc at moderate substrate temperatures [86], while the  $\beta$ -phase can be found at high substrate temperatures or deposition rates [87]. In the  $\alpha$ -phase the molecules are oriented close to edge-on with respect to the substrate. The agreement in the X-ray results and the observed phase suggest only a weak interaction between substrate and film for the  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> and also the SrTiO<sub>3</sub> substrate. Moderate increase in substrate temperatures lead to a higher crystalline order, detected with an increase in the Bragg peak.

This was reported in the literature to result in an increase of the field effect mobility, when transistors are prepared. At even higher substrate temperatures the field effect mobilities were reported to decrease again, which was attributed to gaps between large non-space-filling crystals [88].

For field-effect transistors an intermediate substrate temperature of 85 °C was chosen. The reasoning was that already high order can be expected in combination with a smooth film.

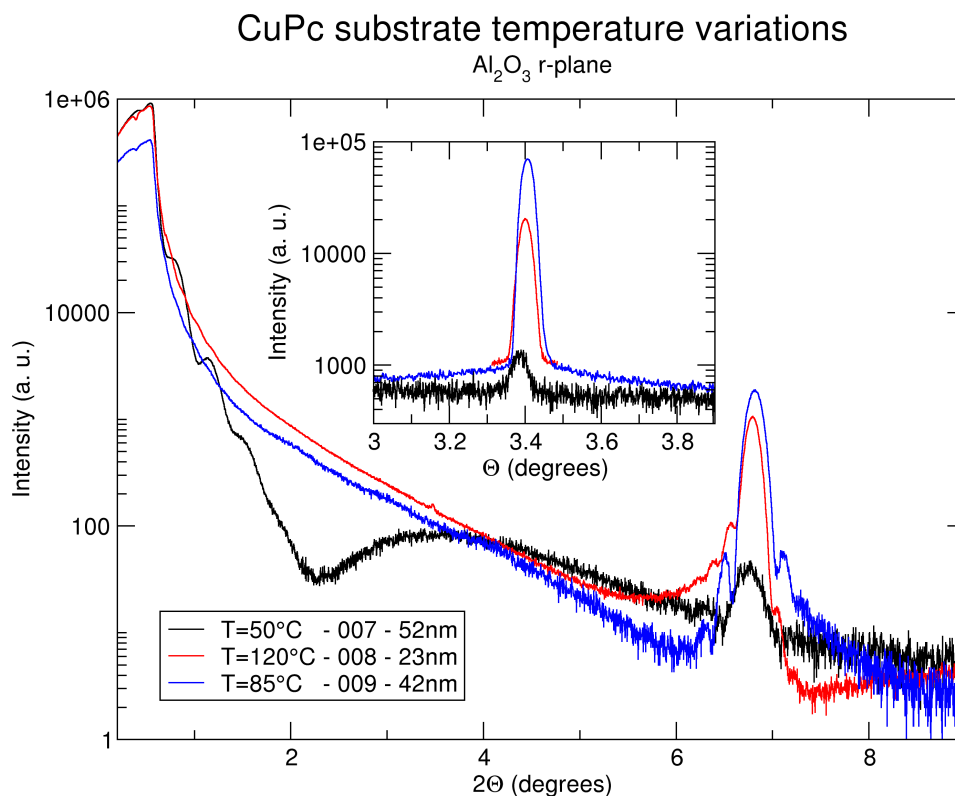


Figure 5.9: Small angle X-ray diffractions of CuPc films on  $\alpha$ -Al<sub>2</sub>O<sub>3</sub>

Small angle X-ray diffraction pattern of the CuPc thin films prepared in the OMBD chamber on  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> substrates. The films were deposited on substrates at different temperatures. The film prepared at 50 °C showed pronounced Kiessig fringes but only a small Bragg peak. It was observed that this changed with higher substrate temperature - the Kiessig fringes disappeared in favour of Laue oscillations. The inset shows the corresponding rocking curves. The width (FWHM) of the rocking curve from film 009 was 0.038°. Deposition time was 2 h for all films. Effusion cell temperatures were 355 °C for film 007, 350 °C for film 008 and 360 °C for film 009.

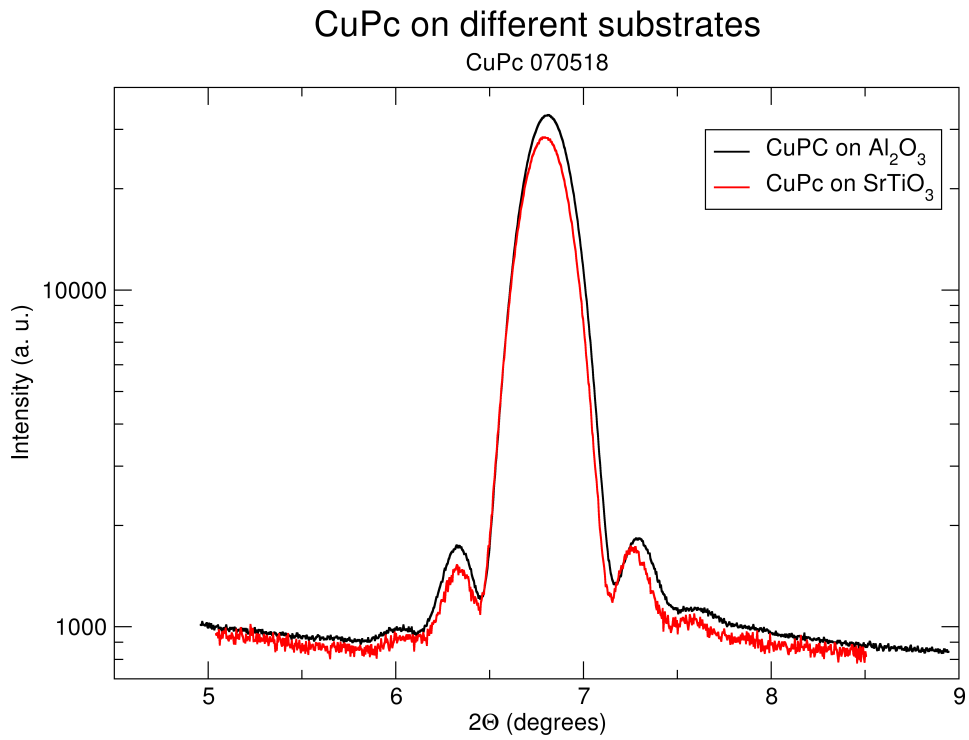


Figure 5.10: CuPc substrate comparison

X-ray diffraction Bragg peak of a CuPc thin film prepared in the OMBD chamber simultaneously on an  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> and a SrTiO<sub>3</sub> (100) substrate. The film was deposited with an effusion cell temperature of 368 °C for 300 minutes. Substrate temperature was 100 °C. The fit results in a thickness of about 26 nm. No influence of the substrate could be observed.

# Chapter 6

## Dielectric layer formation

There are several possibilities to form a dielectric layer for thin film field-effect transistors. The easiest way is to use substrates where a dielectric layer is already present, such as a thermally grown  $\text{SiO}_2$  layer on top of Si. Such substrates are commercially available and do not need any further treatment except for a thorough cleaning.

When a high- $\kappa$  dielectric, such as  $\text{SrTiO}_3$ , is desired in a field-effect transistor structure a different approach is necessary. Commercially available are doped  $\text{SrTiO}_3$  substrates, which can function as gate electrode, but the insulating layer must be prepared on this substrate. The preparation of dielectric thin films of complex oxides is a challenge. Thermal evaporation from effusion cells of the compound is not possible due to the high melting point, and the evaporation with an electron beam evaporator is also difficult since  $\text{SrTiO}_3$  is an insulator. A possibility is the evaporation of strontium and titanium in a stoichiometric ratio with an additional low oxygen partial pressure in an UHV chamber, but this is also very complex [89].

A different deposition method, where the melting point of the material is not important is sputtering. There are two different sputtering methods, DC and radio frequency (RF) sputtering. DC sputtering is not suitable for insulating materials, since charges will build up on the target. In this work RF sputtering was chosen for the preparation of the dielectric  $\text{SrTiO}_3$  layer.

### 6.1 RF-sputtering

RF-sputtering is a relatively easy and cost efficient method especially for the growth of thicker films. The setup consists of a vacuum chamber where a substrate is facing a sputtering cathode containing a sputtering target. Furthermore, a sputtering gas is necessary. First a plasma of the sputtering gas

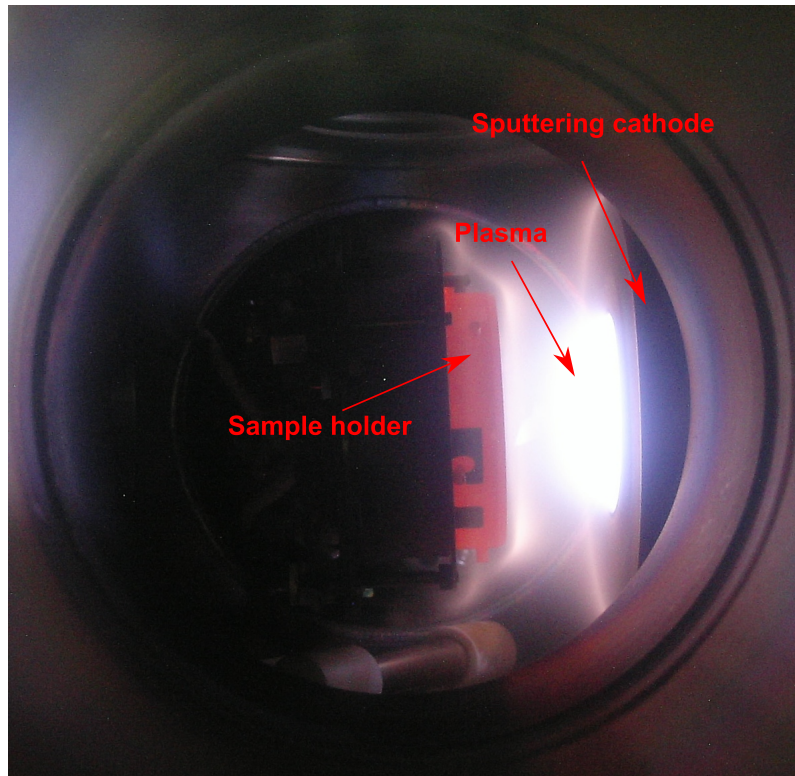


Figure 6.1: The sputter discharge and the sample holder under high temperature

The Inconel sample holder was glowing red (sample temperature around 700 °C) while the other parts of the manipulator were obviously colder. The backplate of the manipulator was connected to the water cooling system, but the sample holder had only minimal contact to the manipulator which prevented cooling via thermal conduction. The sputtering cathode was on the right with the glowing plasma in front of the target.

is created, in this case by a RF-discharge, and ions from the plasma are accelerated onto the target. By using a magnetron in the sputtering cathode, additional electrons are trapped close to the surface and more ions are created by collisions. In this way higher deposition rates are achieved. Via energy transfer atoms from the target material are ejected. The target material is eroded by the bombardment of the ions and the ejected atoms fly through the sputtering chamber. A film of the atoms from the target material is formed by condensation on the substrate surface facing the sputter cathode. A picture from a sputtering process can be seen in Fig. 6.1.

The sputtering process is especially suitable when high deposition rates from



a target consisting of a pure element are desired. For compounds, such as SrTiO<sub>3</sub>, the situation is much more difficult. A stoichiometric target does in general not guarantee a stoichiometric film deposition, since the sputter yield depends among other things on the atomic mass and binding energy on the surface. Furthermore, the rate depends on the preparation conditions, such as gas pressure and atomic mass of the sputtering gas. It has been shown that for example the total gas pressure during deposition has an influence on the Ti/Sr ratio [90] for the sputtering of SrTiO<sub>3</sub>.

Like in the other thin film deposition processes also the substrate temperature influences the morphology of the formed thin film. The sputtering process is often followed by a post heat treatment step which can increase the crystallinity of SrTiO<sub>3</sub> and therefore also the dielectric constant [91]. It has also been shown that a prolonged annealing of SrTiO<sub>3</sub> at more than 1000 °C under ambient pressure can lead to the formation of SrO on the (100) surface [92]. However, a literature survey regarding sputtering of SrTiO<sub>3</sub> yields a variety of very different parameters for power, deposition rate, gas pressure and mixture, source-target distance, substrate temperature and so on. The reason is that every sputter chamber has a different setup and geometry which strongly influences the growth conditions. It is therefore not possible to transfer one recipe just to a different chamber, but one has to optimize the whole process from rough starting parameters. An additional challenge is the high substrate temperature of more than 700 °C during deposition and post-annealing in the sputtering chamber under oxygen atmosphere. At these temperatures it is difficult to determine the true substrate temperature since heat transfer by radiation is dominant and there might be a difference between the temperature measurement point and the temperature of the substrate. Therefore, the substrate temperatures reported in this work should only with caution be directly compared to other publications.

The sputter process was extensively studied in a large parameter space. The most important parameters and the range in which they were studied

- the substrate temperature, from 400 °C up to 800 °C,
- the absolute chamber pressure, determined by gas flow from inlet and pumping speed, from below 0.001 mbar to 2.5 mbar,
- the sputtering power, from 20 W to 200 W,
- the argon/oxygen ratio, from pure argon to pure oxygen, and
- the distance between target and substrate, which was about 15 cm for most of the films.

Unfortunately, the distance between target and substrate was the parameter which was the most difficult to change. Different target substrate distances were tested with a sputter cathode with an adjustable head, but for distances shorter than approx. 4 cm the cathode length had to be readjusted after each sample transfer due to the manipulator geometry. A large difference in sputter rate was observed for the different distances, and the adjustment of the distance was not sufficiently reproducible. The fixed distance was therefore used in the following. For the optimization of the sputtering parameters a stable process during deposition was of paramount importance. The stability was affected by the setup of the sputtering chamber. In the following problematic points and possible solutions are listed

- The sputter power applied to the SrTiO<sub>3</sub> target had to be varied by not more than 10 W per minute. Otherwise a breakage of the target due to thermal stress might occur. This led to a long power up and down phase of 10 minutes each (for 100 W forward sputtering power) compared to the shortest sputtering times of 10 minutes. This was especially problematic for the upscaling of the film thickness from the thin layers which were used to study the growth process to the relatively thick layers, which were used to prepare the transistor structures. This could be solved by turning the substrate away during power up and down.
- The small design of the sputtering chamber prevented the use of a shutter before and after deposition. Therefore the power up and down phase of the cathode could not be completely separated from the sputtering phase. It was attempted to reduce this problem by turning the substrate away from the sputter target during power up and down<sup>1</sup>. This, however, led to a different problem, namely a different temperature of the target or the substrate, while the manipulator was tilted in a different direction.
- The gas flow and the chamber pressure had to be constant during the sputtering process. The sputter gases, argon and oxygen, were supplied from gas bottles. Their mass flow was controlled by mass flow controllers (MFC), but these controllers could not cope with the pressure drop to the vacuum system. To prevent this problem, the MFCs have not been connected directly to the vacuum chamber but to reservoir volumes which were connected to the vacuum chamber with needle valves<sup>2</sup>. Conservation of mass guaranteed that the mass flow through the MFCs was equal to the mass flow through the needle valves when pressure equilibrium conditions were reached.

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<sup>1</sup>Not implemented for all films.

<sup>2</sup>To prevent an interaction of the two gases each gas was connected separately.

- Apart from the gas flow, the pumping system was responsible for a constant pressure in the chamber. The sputtering chamber was pumped with a turbo molecular pump system consisting of a turbo molecular pump and a membrane pump. The membrane pump alone had a too high base pressure ( $\approx 5$  mbar), therefore the turbo pump had to run during the sputter process as well. For longer depositions or higher pressures the gas flow represented a considerable burden for the turbo pump. This could be reduced by utilizing a lower rotation frequency.
- The ignition of the plasma was not possible at low pressure (below about 0.03 mbar). When sputtering at low pressures was desired an ignition at higher pressure was necessary combined with a reduction of the pressure afterwards. To ignite the plasma at higher pressure and reach the sputtering pressure as fast as possible, a valve between turbo pump and membrane pump was closed for several seconds. When the valve was opened after ignition, the chamber returned to its original pressure very quickly. This method was of advantage compared to increasing the mass flow at the inlet which took a longer time till the pressure reached the pre-ignition level.
- The pressure during deposition was measured with a capacitance gauge. The calibration of this gauge was sensitive to high pressure such as during annealing after deposition and had a lowest measurement range of 0.001 mbar. Therefore absolute pressure values, especially for pressures below 0.02 mbar from different depositions may be affected by systematic measurement errors.
- The sputtering chamber was also used for sputtering of aluminum. Therefore, it existed a risk of cross contamination from one cathode to the other. To minimize these effects only aluminum or SrTiO<sub>3</sub> was sputtered for a series of consecutive films and after switching to the cathode which had not been in use it was cleaned by a separate sputtering run.

One of the most critical factors for the growth of SrTiO<sub>3</sub> is the substrate temperature, which was in the used setup measured indirectly with a thermocouple in the heating system of the manipulator. As an additional control the power to the heating system (current and voltage) was also recorded. This resulted in several difficulties and uncertainties related to the extreme conditions in the sputtering chamber.

- The heating system, e.g., heating wires and feed cables had to be changed several times which led to nominally different power/temperature relations.

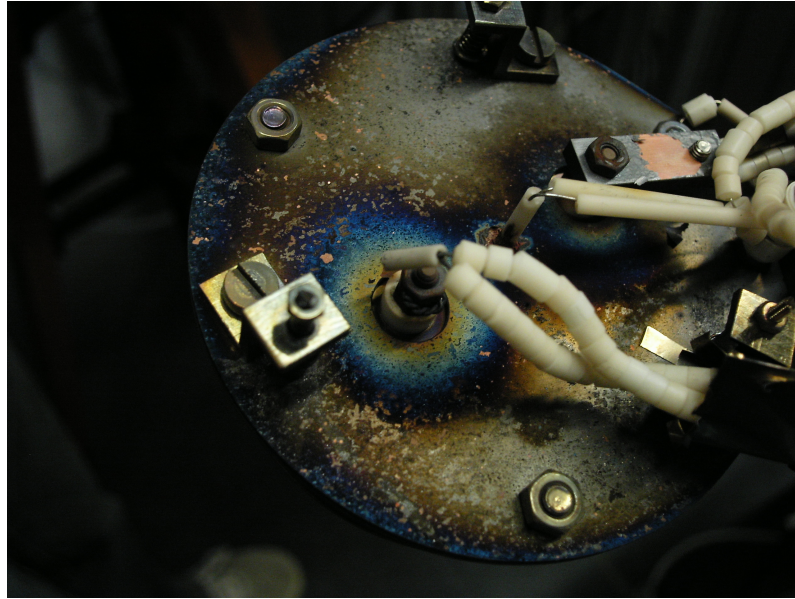


Figure 6.2: Manipulator corrosion

Picture of the sputter manipulator backside after several sputtering runs. The surfaces suffered from corrosion due to the high temperatures and aggressive atmosphere.

- The metal surfaces of the manipulator and sample holder changed due to oxidation and depositions. Over time the manipulator suffered from corrosion as shown in Fig. 6.2. This led to a different emissivity of the surfaces and caused temperature changes.
- The substrates were glued to the sample holder. This process was not perfectly reproducible - different amount of glue on the sample holder might also have had an influence due to thermal conduction.
- There was a difference from one sample holder to another. This was for example observed for a series of consecutive films with two sample holders which were fabricated at the same time in the workshop. At the same temperature the heating power for the one was always higher than the heating power for the other.
- The gas flow through the sputter chamber influenced the temperature.
- The sputtering power also had an influence on the temperature.

A plot of the currents which were necessary to obtain the temperature set-point is depicted in Fig. 6.3. Before sputtering the substrate temperature set-point

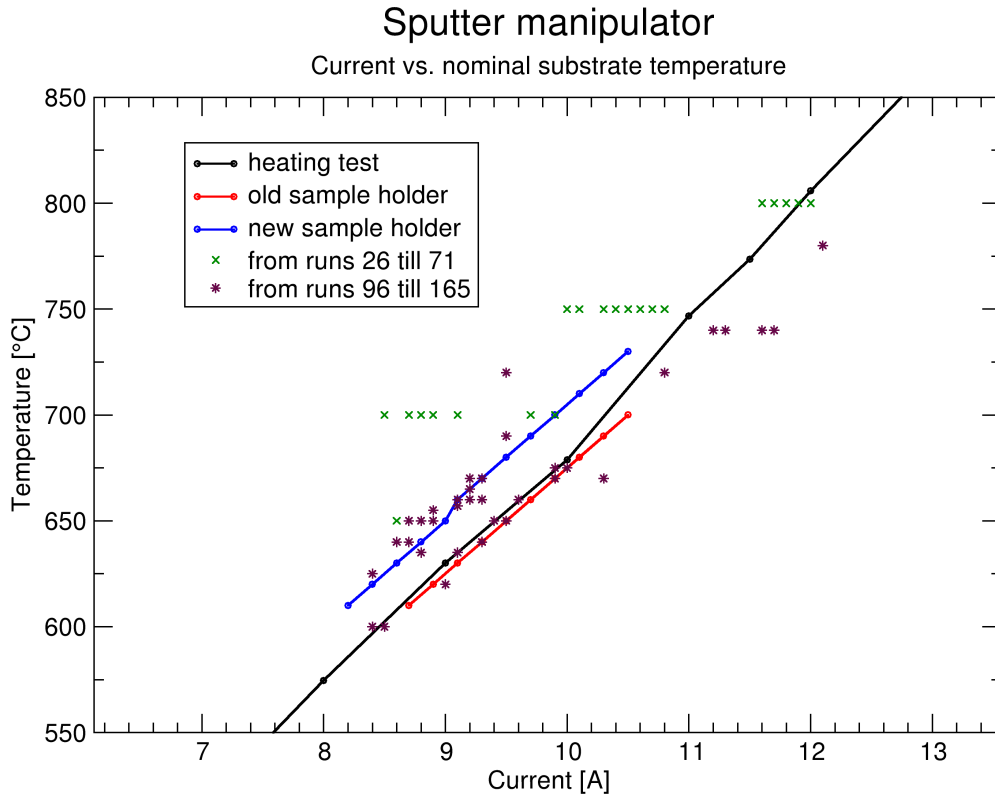


Figure 6.3: Temperature vs. heating current

This plot shows the temperature-heating current dependency of the sputter manipulator. The black line was obtained from an initial heating test. Usually, a temperature set point was provided and the current which is necessary to obtain this temperature was recorded. A test run with two different sample holders showed a clear difference from sample holder to sample holder. The question is whether the true substrate temperature was the same for different sample holders at the same nominal temperature.

was provided. The PID controller adjusted the power of the resistive substrate heater. The heating current was recorded after temperature stabilization in high vacuum before the gas flow for sputtering was adjusted. The plot shows that very different currents were necessary to obtain the same temperature set-point in different sputtering runs. It also shows the clear difference between two sample holders. On the other hand the old sample holder still proved well in agreement with the initial heating test.

## 6.2 SrTiO<sub>3</sub> - growth results

In the literature SrTiO<sub>3</sub> has been grown on several substrates [93], usually substrates with a crystal structure close to SrTiO<sub>3</sub>, such as for example MgO or LaAlO<sub>3</sub>, were used [79]. Other choices were commercially interesting substrates like doped silicon [91].

In this work, for device preparation SrTiO<sub>3</sub> was grown on Niobium-doped SrTiO<sub>3</sub> substrates with (100) orientation. This had the advantage of no lattice mismatch which is optimal for epitaxial growth where the highest dielectric constant and breakdown field are expected. On the other hand it was difficult to optimise the preparation conditions since it was hard to distinguish substrate from film with the standard analytical methods such as, e.g., XRD.

Starting from literature parameters the sputter process was optimized for crystal structure and roughness on random cut  $\alpha$ -Al<sub>2</sub>O<sub>3</sub>, which for our substrates corresponded almost to r-plane, MgO (100) and later also on Niobium doped and undoped SrTiO<sub>3</sub> (100). In total 165 sputtered films (including transistors) were prepared. The sputtered films were examined with respect to thickness, surface roughness and crystal structure with X-ray diffraction and optical microscopy. A sufficiently large growth rate was established.

**Results on  $\alpha$  - Al<sub>2</sub>O<sub>3</sub>** Apart from the desired (100) orientation also other orientations could be detected with X-ray diffraction, especially (110) and (111) when deposited on random cut  $\alpha$ -Al<sub>2</sub>O<sub>3</sub>. The corresponding literature values for the relative intensities and the positions of the Bragg reflexes are:

- (100),  $2\theta=22.754^\circ$ , I/rel=3.85
- (110),  $2\theta=32.397^\circ$ , I/rel=100
- (111),  $2\theta=39.957^\circ$ , I/rel=21.20
- (200),  $2\theta=46.472^\circ$ , I/rel=41.20

Some examples are shown in Fig. 6.4 and Fig. 6.5, where different phases were found on one film. Also nominally equal sputtering parameters resulted in different ratios of crystal orientations, which was concluded from different peak heights. This indicates that the  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> substrate had only a minor influence on the growth behavior. The  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> substrates were primarily used in the first experiments to find suitable deposition rates. Later  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> substrates were used together with MgO substrates to have a second thickness reference. In a few cases peaks which could not be attributed to SrTiO<sub>3</sub> were

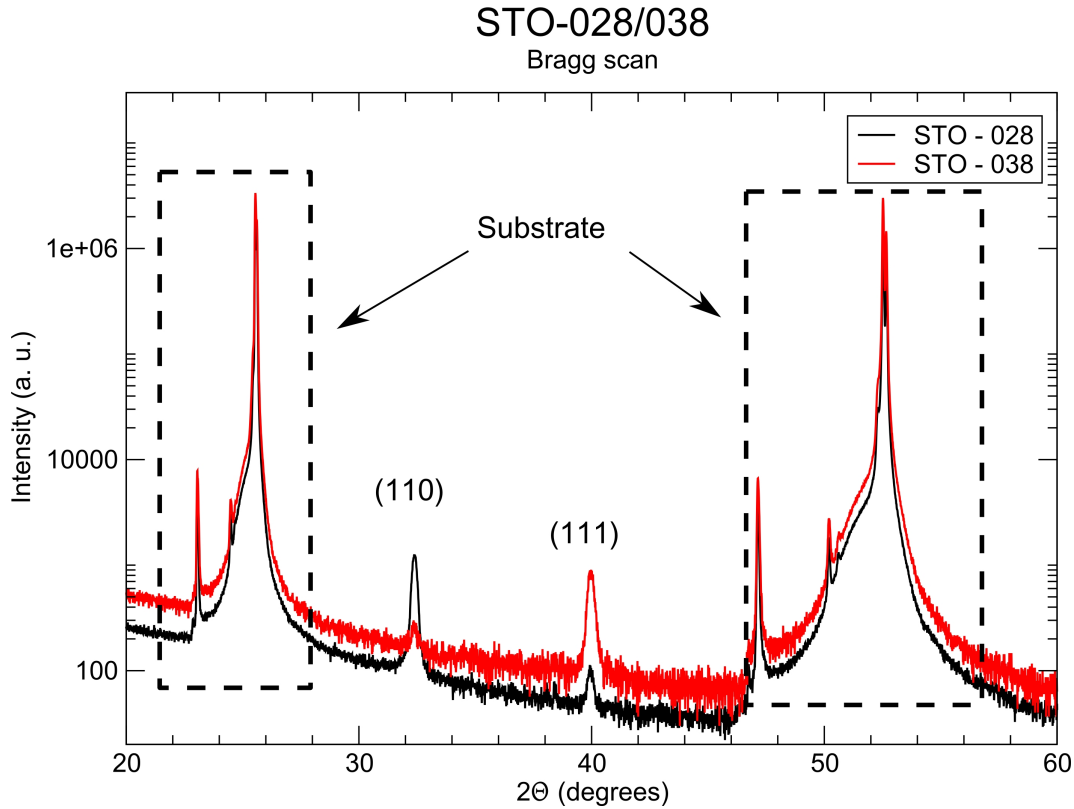


Figure 6.4: Different SrTiO<sub>3</sub> peaks on  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> substrates

Bragg scan of SrTiO<sub>3</sub> film 028 and 038. In film 028 a large (110) peak at 32.4° and a (111) peak at 40° could be detected. In film 038 the (111) peak at 40° was dominating, over the (110) peak at 32.4°. These films had practically identical sputtering parameters: Substrate temperature of 800 °C, sputtering power of 40 W, pressure of about 0.240 mbar, deposition time of 30 minutes, mass flow of Ar 16 sccm and mass flow O<sub>2</sub> 2 sccm. The thickness of film 028 was about 39 nm and of film 038 about 37 nm.

detected. These suggest sputter conditions where films in a different structure were obtained, such as the surface layers of the Sr<sub>*n*+1</sub>Ti<sub>*n*</sub>O<sub>3*n*+1</sub> type which were reported for SrTiO<sub>3</sub> at elevated temperatures in oxidizing or reducing conditions [94, 95].

**Results on MgO** On MgO the SrTiO<sub>3</sub> films grew preferentially in the (100) direction. The Bragg peaks of the sputtered films were shifted to a lower  $2\theta$  value as compared to bulk SrTiO<sub>3</sub>. This was probably related to the larger

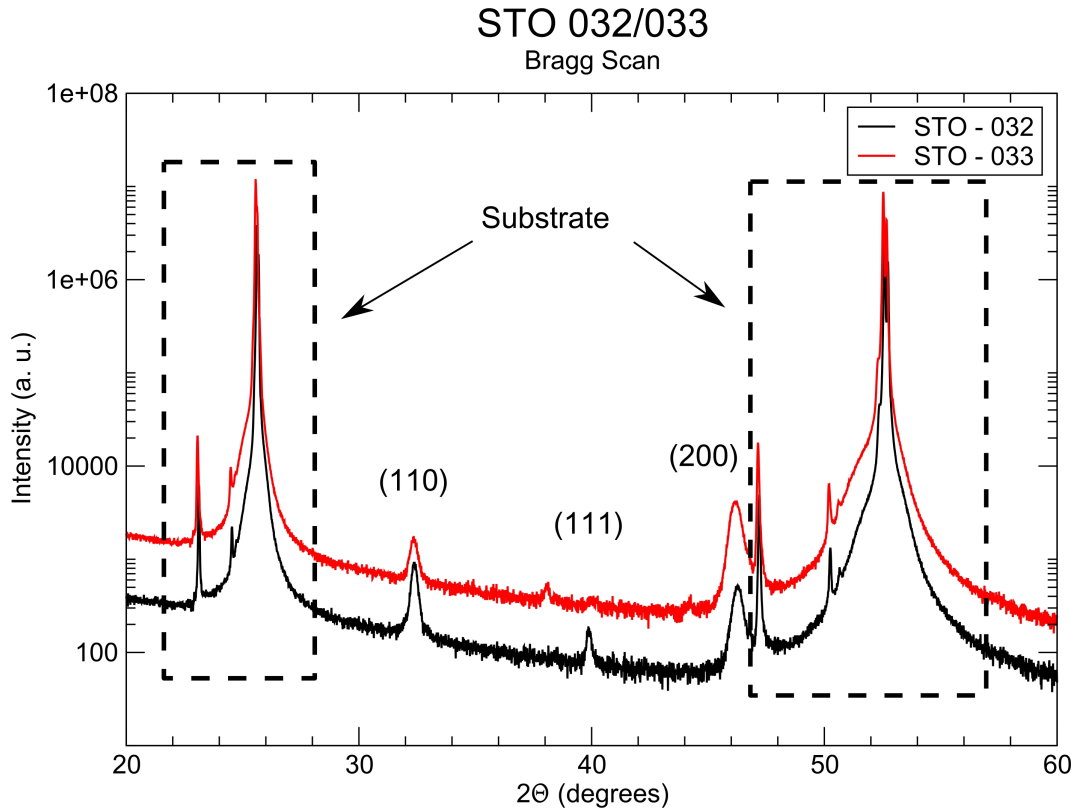


Figure 6.5: Different SrTiO<sub>3</sub> peaks on  $\alpha$ -Al<sub>2</sub>O<sub>3</sub> substrates

Bragg scan of SrTiO<sub>3</sub> film 032 and 033. In film 032 a (110) peak at 32.4°, a (111) peak at 40° and also a (200) peak at 46.4° could be detected. Film 033 showed a smaller (110) peak at 32.4°, the (111) peak at 40° was barely visible. The (200) peak at 46.4° increased compared to the previous film 032. These films were prepared with practically identical sputtering parameters: Substrate temperature of 800 °C, sputtering power of 40 W, deposition time of 30 minutes, mass flow of Ar 16 sccm and mass flow O<sub>2</sub> 1.5 sccm. The pressure of film 032 was 0.090 mbar and for film 033 0.110 mbar. These parameters were also very similar to the films for which the X-ray diffractograms are shown in Fig. 6.4, and differed only by a slightly reduced oxygen mass flow and a resulting lower pressure. The film thickness of these films were about 58 nm for film 032 and about 51 nm for film 033.



lattice constant of MgO ( $a = 4.216\text{\AA}$ ) as compared to SrTiO<sub>3</sub> ( $a = 3.905\text{\AA}$ ) which caused a tensile stress due to the misfit [96]. This effect was stronger for films prepared at lower pressure (e.g., 0.430 mbar and lower), but on the other hand the deposition rate was much lower at higher pressures (e.g., 0.700 mbar). This relationship is illustrated in Fig. 6.6. In addition to X-ray studies the sputtered films were examined with an optical microscope. Although an ideal film has a texture which can not be distinguished from the substrate, the optical microscope was very useful to get an indication on film quality of non ideal samples. In Fig. 6.7 the top left picture shows an example of a well-ordered and smooth film as reference. The other pictures and the pictures in Fig. 6.8 show a variety of films with different properties, e.g., with a rough or de-wetted surface, which were unsuitable for devices preparation. Some of them showed peaks in X-ray diffraction or thickness oscillations, but for most of them it was not possible to fit a thickness or observe a Bragg peak from the film. Often a too low or too high substrate temperature was the root cause. The pictures at the bottom of Fig. 6.8 are from two different field effect transistor devices. The rough structures indicate that no homogeneous dielectric layer was formed during sputtering. This was confirmed when it was attempted to measure the devices. The leakage current through the dielectric layer was too large, i.e., the resistance of the dielectric was low. One problem in the optimization process for devices was the stability of the sputter discharge. The films used for devices were much thicker and the sputter process was therefore much longer. This further increased the stability requirements on the sputtering process not only from run to run but also within one (long) run. Low deposition rates increased the required sputtering time for device preparation and also the possibility that impurity atoms were incorporated into the layer. It was therefore concluded that high deposition rates were even more important to obtain a reliable dielectric layer.

In the literature it was reported that annealing improved the crystalline quality of SrTiO<sub>3</sub> films. This was tested on the grown films with ex-situ tempering in an oven. Multiple films could be tempered at the same time and changes were observed with X-ray diffraction. The tempering was performed at 800 °C for 24 h. This annealing of SrTiO<sub>3</sub> films showed an increase in the height of the Bragg peak and a shift in position in direction of bulk SrTiO<sub>3</sub>, as it can be seen in Fig. 6.9. An annealing process step was therefore also included for device preparation. This was done in situ directly after the deposition of the SrTiO<sub>3</sub> films. The annealing was conducted in an oxygen atmosphere within a pressure range between 0.02 mbar and 100 mbar at temperatures from 600 to 900 °C and durations of 10 minutes up to 2 hours.

## SrTiO<sub>3</sub>- Bragg scans on MgO

different pressures during sputtering

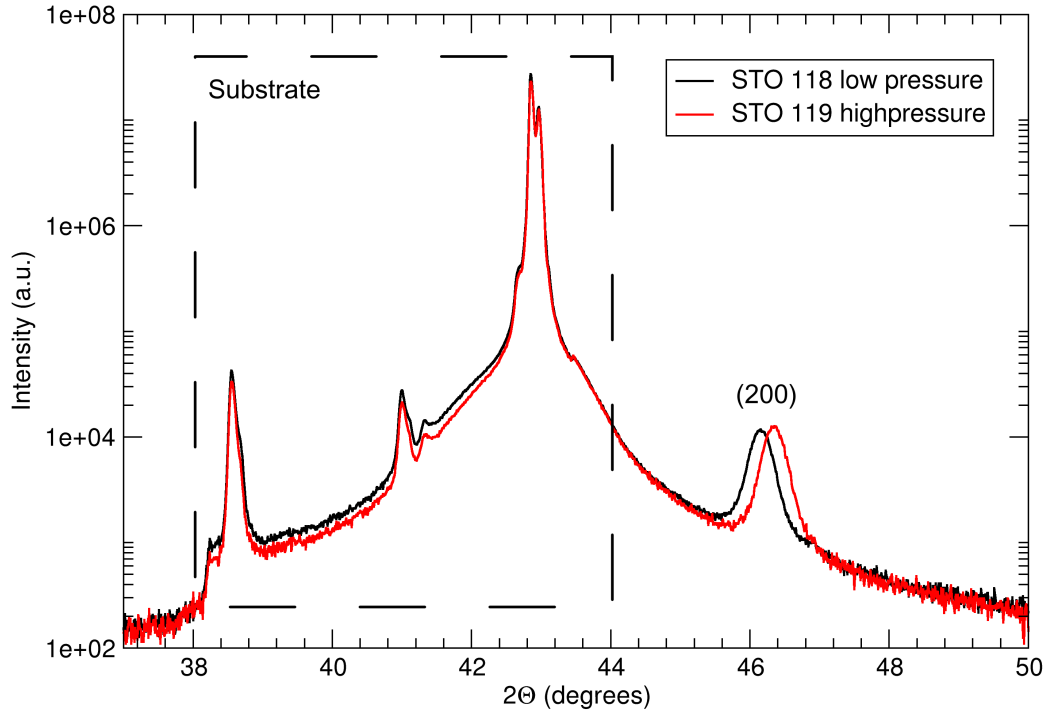


Figure 6.6: Films prepared under different pressures on MgO

This is a Bragg scan of SrTiO<sub>3</sub> film 118 (black) and film 119 (red) prepared at different pressures. The sputter gas was controlled by the mass flow controllers to an argon flow of 10.4 sccm and an oxygen flow of 1.8 sccm for both films. The different pressure was achieved by a higher rotation frequency of the turbo molecular pump for film 118 (455 Hz) as compared to film 119 (425 Hz). Film 118 was prepared at a pressure of 0.430 mbar with a deposition time of 40 minutes. The film thickness was estimated to be 62 nm. In contrast, film 119 was prepared at a pressure of 0.700 mbar with a deposition time of 60 minutes. The thickness of this film was 65 nm, hence the deposition rate was reduced by a factor of 1.5. On the other hand, the center of gravity of the SrTiO<sub>3</sub> (200) Bragg peak was detected at a  $2\theta$  angle of  $46.15^\circ$  for film 118 and at  $46.34^\circ$  for film 119 (the literature value for bulk SrTiO<sub>3</sub> is  $46.47^\circ$ ).

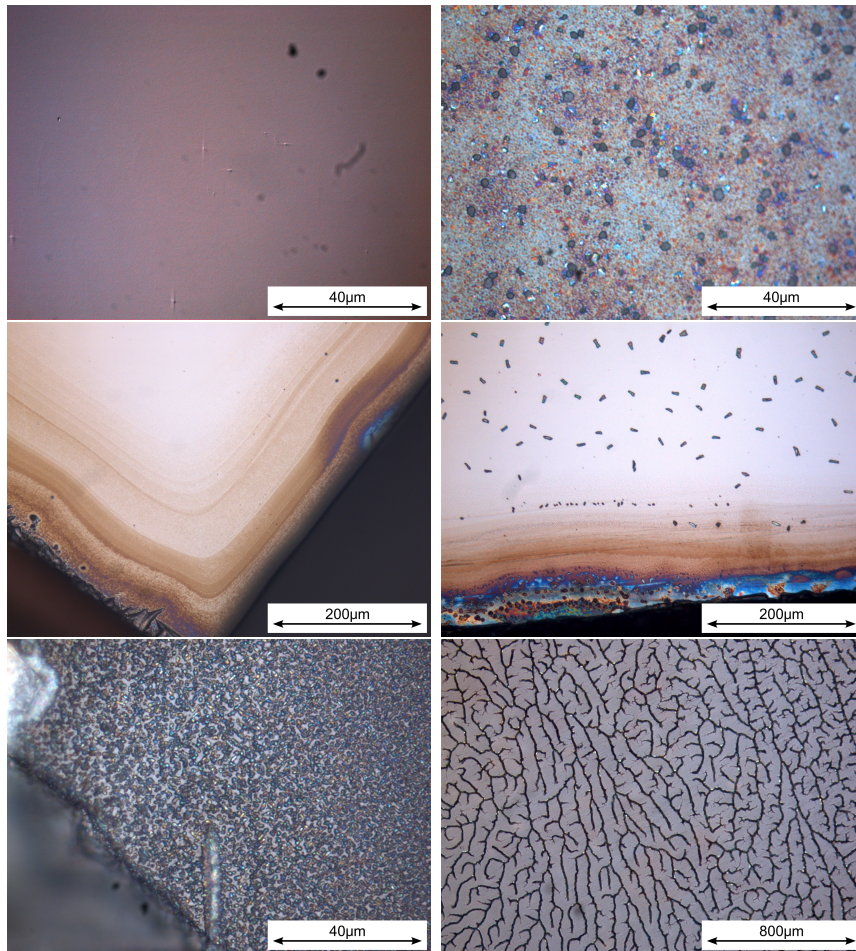


Figure 6.7: Microscope images of sputtered films (1)

These are microscope pictures of sputtered  $\text{SrTiO}_3$  films. The top left pictures shows a film (162) with a flat surface structure, as it is necessary for transistor preparation. The other pictures show films which are not suited for devices, to give an impression what could be determined with an optical microscope. The top right for example is a film on a quite cold ( $550\text{ }^\circ\text{C}$ ) substrate (076). The film is not homogeneous and rough. The pictures in the second row show films with a structure along the edge (057, 023), the film on the right exhibits also micro crystals in that area. The reason is not clear, both films were prepared with very different sputtering parameters. The pictures at the bottom are from a sputtering run (074) with a high temperature of  $800\text{ }^\circ\text{C}$  and a high pressure of 1.9 mbar. Here no closed layers were formed. The picture on the left was on a  $\text{MgO}$  substrate, where the surface consisted of small crystallites, on the right on an  $\text{Al}_2\text{O}_3$  substrate, where a dendrite like surface structure was obtained.

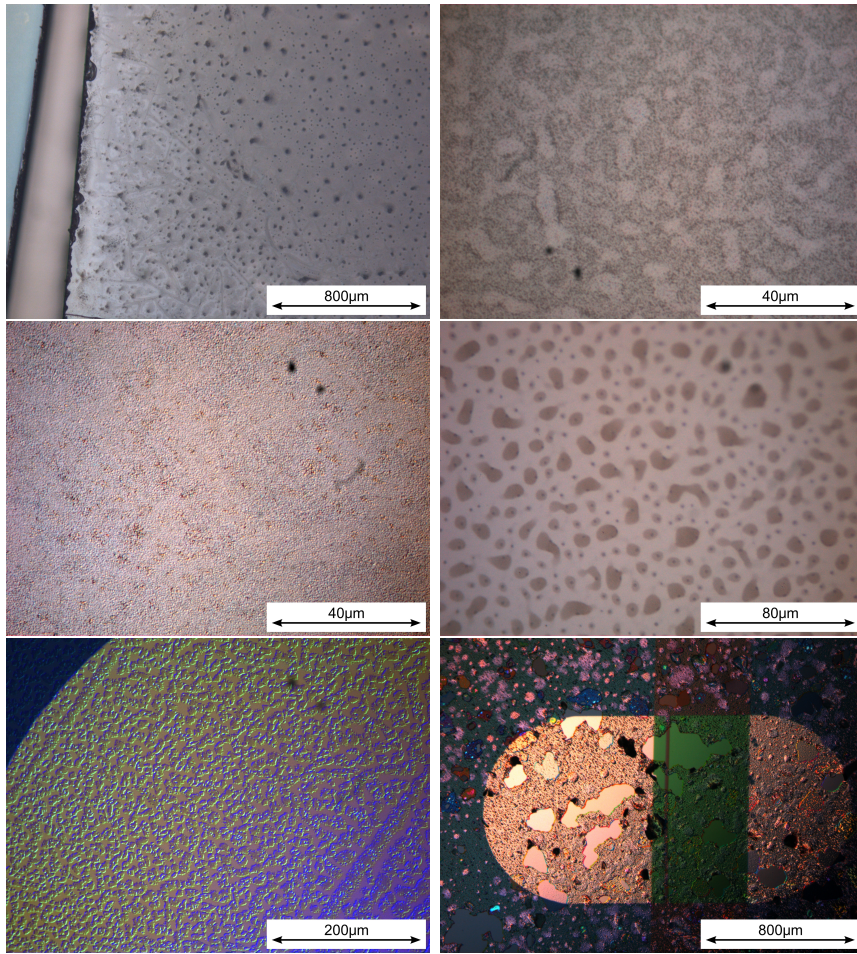


Figure 6.8: Microscope images of sputtered films (2)

These are some more microscope pictures of sputtered  $\text{SrTiO}_3$  films not suitable for device preparation. In the top row on the left is a film (082) which was prepared under relative high pressure (1.3 mbar), for the film on the top right the temperature was slightly too cold. Both films had a rough surface. In the middle row on the left (148) a film which was prepared with a high sputter power (200 W) has also a rough surface. In the middle on the right (137) an inhomogeneous surface is observed, however the reason is not clear. At the bottom pictures, where the preparation of field effect transistors was attempted (left: fet8, right: fet9) are shown. On the left picture a part of a gold electrode deposited after sputtering is visible. The surface was very rough and the  $\text{SrTiO}_3$  layer was not insulating. This film was prepared with a relative high power of 150 W and a pressure of (0.64 mbar) with a deposition time of (335 min). On the picture at the bottom right the dielectric layer was prepared at low pressure (0.02 mbar), but the substrate temperature was too cold ( $400^\circ\text{C}$ ).

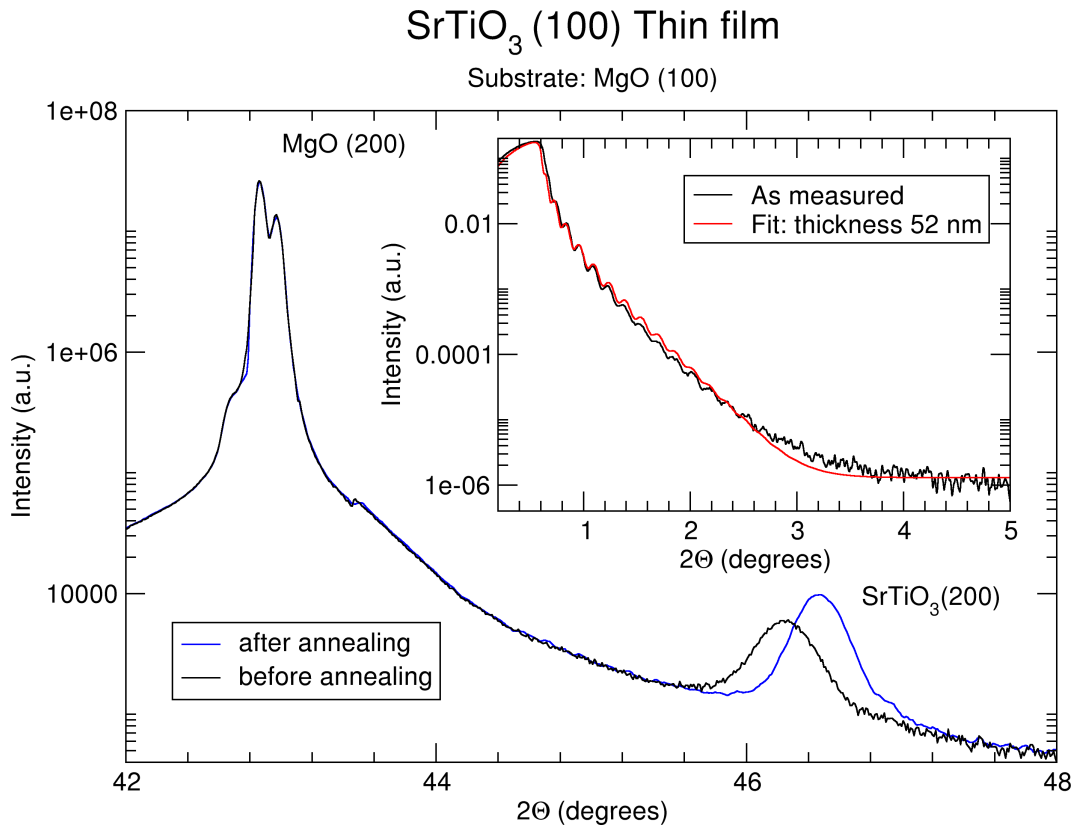


Figure 6.9: Annealing of a SrTiO<sub>3</sub> film

X-ray diffraction Bragg peak of SrTiO<sub>3</sub> (100) film 101 before and after annealing in air. The height of the peak increased and the center shifted toward the literature value for bulk SrTiO<sub>3</sub>. Similar behaviour was observed for several films. The inset shows the corresponding thickness measurement of the SrTiO<sub>3</sub> film on the MgO substrate.

**Sputtering parameter summary** Since the sputter process was influenced by a collection of different parameters, the most important ones are recapitulated here. Although there were some counterexamples, the general observations were:

- Highest sputtering rate was observed at a low pressure of about 0.02 mbar. An increase of pressure decreased the sputtering rate.
- An increase of sputter power increased the sputtering rate. A bubble plot (comp. Fig. 6.10) is used to illustrate that.
- The argon/oxygen ratio had no major influence on the sputtering rate.



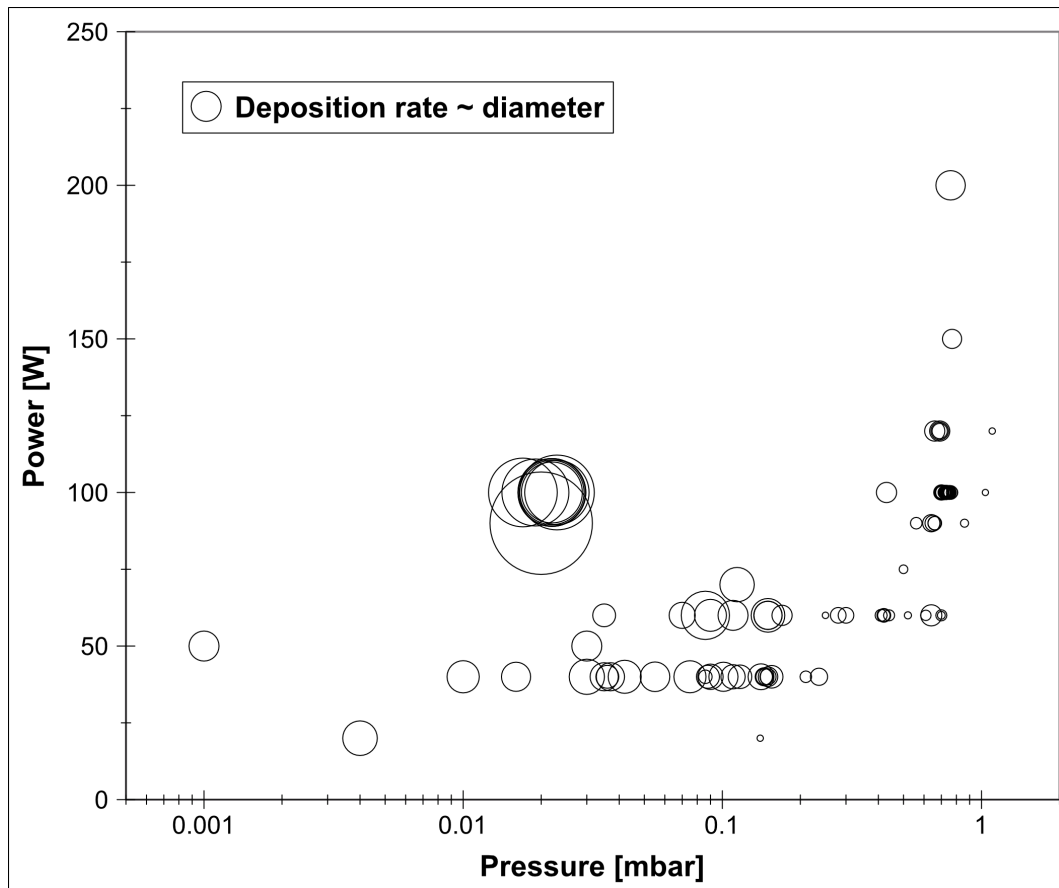


Figure 6.10: Influence of power and pressure

This bubble plot illustrates the influence of sputter power and pressure on the deposition rate. The size of the bubbles indicates the deposition rate (thickness determined by X-ray diffraction divided by deposition time). In general the deposition rate decreased with increasing pressure, and increased with increasing sputtering power.

- Substrate temperature was critical to obtain a well ordered film.
- The films with high rate had a small roughness.
- The pressure during sputtering influenced the position of the (200)  $\text{SrTiO}_3$  Bragg peak when an MgO substrate was used. A stronger shift away from the bulk value was observed for low pressures.
- Annealing improved the film quality.

**Optimized parameters for device preparation** The best parameters for sputtering of (100) SrTiO<sub>3</sub> in our chamber, based on microscopy and X-ray studies, which were found in this work are:

- An argon/oxygen mixture of 2:1 with mass flow Ar 8.4 sccm and mass flow O<sub>2</sub> 4.2 sccm.
- The turbo molecular pump throttled to a frequency of 550 Hz to achieve a pressure of 0.025 mbar.
- A substrate temperature of 720 °C.
- A forward sputter power of 100 W with a deposition time of 90 minutes for field-effect transistor preparation.
- Post annealing at 890 °C for 1 hour in an oxygen atmosphere of 0.01 mbar.

These parameters were the ones used for the best FET devices which have been prepared in this work. It was possible to prepare working FETs with SrTiO<sub>3</sub> as the dielectric with them, but there is room for improvement. The sample size of working dielectrics in transistors or device structures is rather limited and the growth process could be improved with respect to the dielectric properties of the films.





## Chapter 7

# Contact preparation by gold evaporation

For the field-effect transistors gold was selected for the source and drain contacts. Contact preparation was realized by evaporation through a shadow mask.

Since gold is relatively easy to evaporate, initially it was attempted to use one of our own effusion cells with a tungsten filament and  $\text{Al}_2\text{O}_3$  support capillaries. The cell was installed with a water cooling shroud in the contact preparation chamber. It was possible to evaporate gold at a low rate at a nominal temperature of  $1235\text{ }^\circ\text{C}$ , but eventually the effusion cell was damaged. The steel cage supporting the crucible melted and destroyed the filament. It is believed that with some modifications, e.g. employing a tantalum cage instead of a steel cage, our cells should be able to sustain the necessary temperatures for gold evaporation, but a commercial cell was in this work. This cell allowed for a sufficient temperature for the evaporation of gold. Since the commercial cell was equipped with a large crucible one of our standard crucibles was put inside the cells crucible, supported by two tantalum sheets, to reduce the amount of necessary source material.

The deposition rate was calibrated with several samples and the deposition process was automated with a computer program, which executed a temperature ramp from standby temperature of  $400\text{ }^\circ\text{C}$  to deposition temperature, controlled the deposition time and executed a second ramp down to standby temperature. The pressure in the contact preparation chamber was recorded during the deposition process. A data file recorded from the computer program is depicted in Fig. 7.1. It shows how the temperature followed the temperature set point. It also shows the pressure increased due to the rise of the effusion cell temperature. Since there was no heating system for the sample holder in the contact preparation chamber the substrate was always nominally at room

## Au evaporation

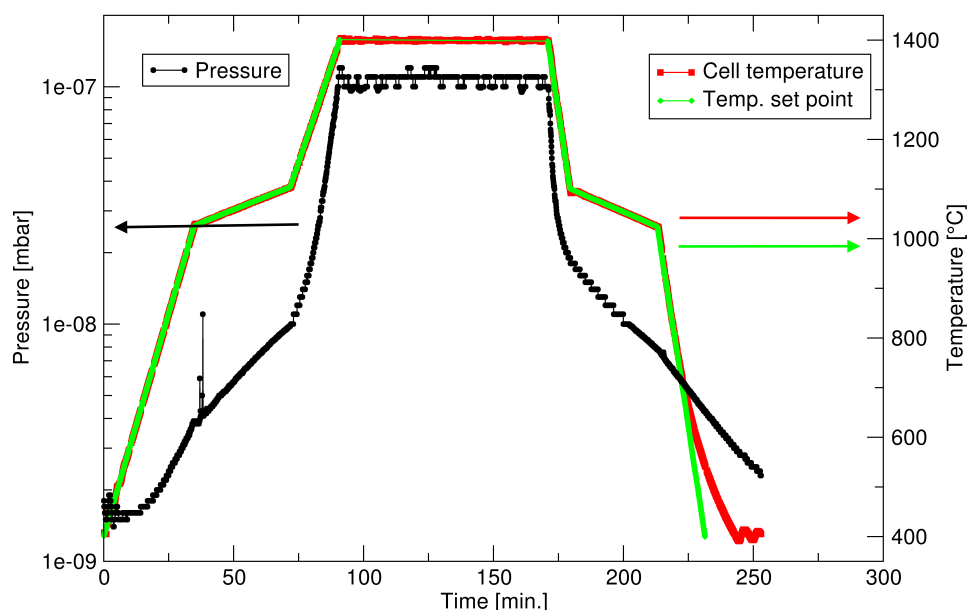


Figure 7.1: Record of a typical Au deposition process

Temperature (red/green right y-axis) and pressure (black left y-axis) vs. time curves for Au contact evaporation. The temperature (red curve) followed the temperature set point (green curve) accurately except for the last part of the ramp down. The temperature was increased by  $18\text{ }^{\circ}\text{C}/\text{min}$  and ramped down with  $36\text{ }^{\circ}\text{C}/\text{min}$ . In the Au melting region (melting point of  $1064\text{ }^{\circ}\text{C} \pm 40\text{ }^{\circ}\text{C}$ ) the temperature was varied with a lower rate of  $2.4\text{ }^{\circ}\text{C}/\text{min}$  which allowed for a homogeneous melting and freezing of the material. The deposition temperature of  $1400\text{ }^{\circ}\text{C}$  was reached after 90 min. The pressure in the chamber was monitored and increased and decreased according to the effusion cell temperature.

temperature during deposition. But due to radiation heating from the effusion cell the true substrate temperature was considerably increased. This increase has not been quantified, but when samples were moved out of the vacuum system through the load lock shortly after the gold deposition process, they were still quite hot. The contact preparation chamber was not equipped with a shutter. There was the possibility to control the deposition time by turning the sample holder away from the effusion cell during ramp up and/or ramp down. The alternative was to leave the sample holder directed towards the effusion cell during the whole time. This increased the thickness of the gold layer, since material was already evaporated below the nominal deposition temperature.

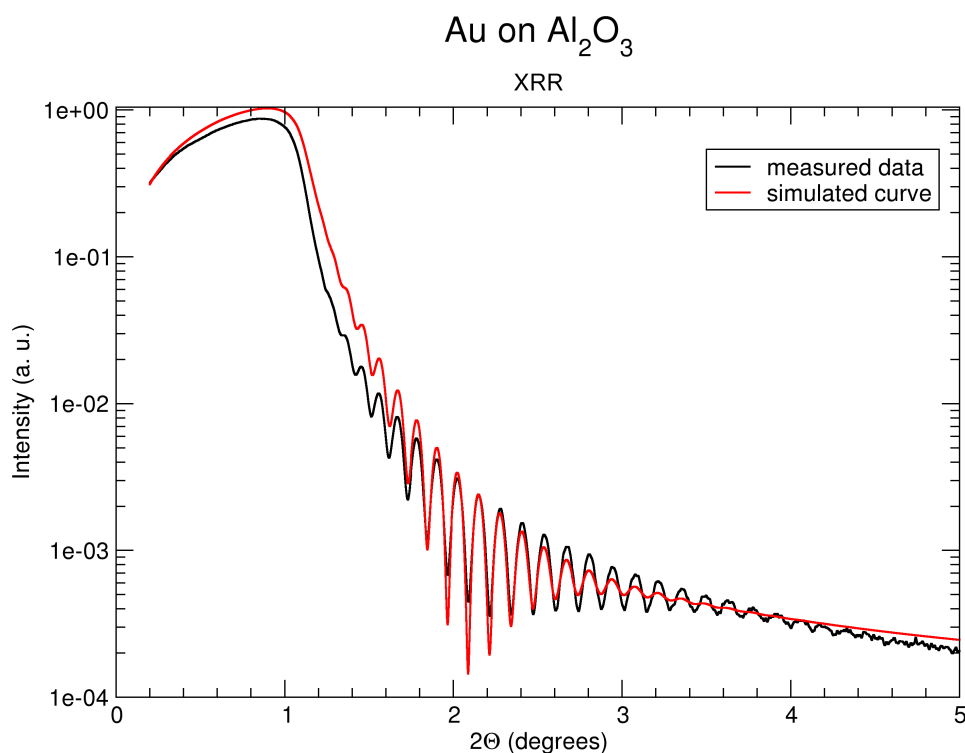


Figure 7.2: Au X-ray data

An X-ray reflectometry scan (black) and fit (red). The fit was performed by the Leptos software from Bruker. The fit region was restricted to the area between 1° and 3.8°. Gold (film 5) was evaporated here at 1400 °C for 80 minutes (plus ramps). The thickness was determined to 60 nm, the roughness to 1.37 nm.

Thickness calibration was performed by X-ray reflectometry measurements and the deposition rate proved to be quite reproducible. An example of an XRR measurement and fit is depicted in Fig. 7.2. This Au thin film had a thickness of 60 nm and was deposited within 80 minutes (plus ramps) at 1400 °C.

For contact preparation shadow masks were used. Here it was important to tilt the sample holder in the proper angle<sup>1</sup> to the effusion cell to prevent a lateral displacement of the contact pads on the substrate surface. In the worst case, displacements in the subsequent deposition processes for a FET accumulated so that the channel between source and drain electrode was not or only partially filled. Due to the very short distance between shadow mask and substrate (a few μm) the contact areas were very sharp as was observed with optical microscopy (Fig. 7.3), where no half-shade could be detected, and

<sup>1</sup>Angle of 300° on the scale of the sample manipulator.

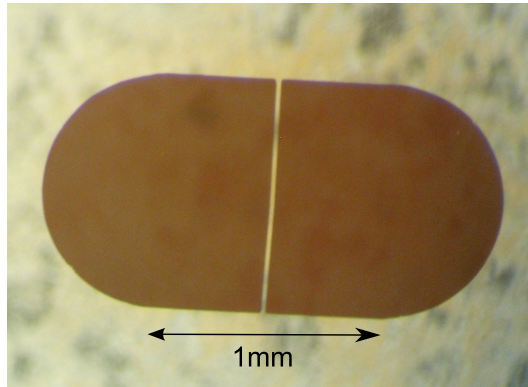


Figure 7.3: Gold pads

Microscope picture of a test deposition of gold source and drain electrode. The width of the gap was 1 mm, the length was 20  $\mu\text{m}$ . With an optical microscope no half-shade was visible.

AFM (Fig. 7.4), where a half shadow of 5  $\mu\text{m}$  on the channel length of 20  $\mu\text{m}$  was determined. This resulted in an effective channel length of 15  $\mu\text{m}$ .

Standard deposition conditions established were a temperature of the gold effusion cell of 1400  $^{\circ}\text{C}$  for a duration of 40 minutes which resulted in a thickness of approximately 30 nm. In Tab. 7.1 different deposition conditions and the resulting film thicknesses are reported. The duration was always the time at the deposition temperature. The column "Ramp included" refers to the state of the sample holder, whether it was directed towards the effusion cell during ramp up (18  $^{\circ}\text{C}/\text{min}$ ) and ramp down (36  $^{\circ}\text{C}/\text{min}$ ) or not. To allow for an automatic deposition, the ramps were included in the standard process. In this way also the source material is used more efficiently.

Number	Temperature	Duration	Thickness	Ramp included	Date
gold1	1320	20	8.5	no	15.02.2006
gold2	1320	60	16	no	16.02.2006
gold3	1370	60	26	no	21.02.2006
gold4	1400	60	38	no	07.04.2006
gold5	1400	80	60	yes	10.04.2006
gold6	1400	80	49	yes	23.05.2006
Au-070910	1400	30	19.6	yes	10.09.2007
Au-071213	1400	40	24.6	yes	13.12.2007

Table 7.1: Overview of the prepared gold samples

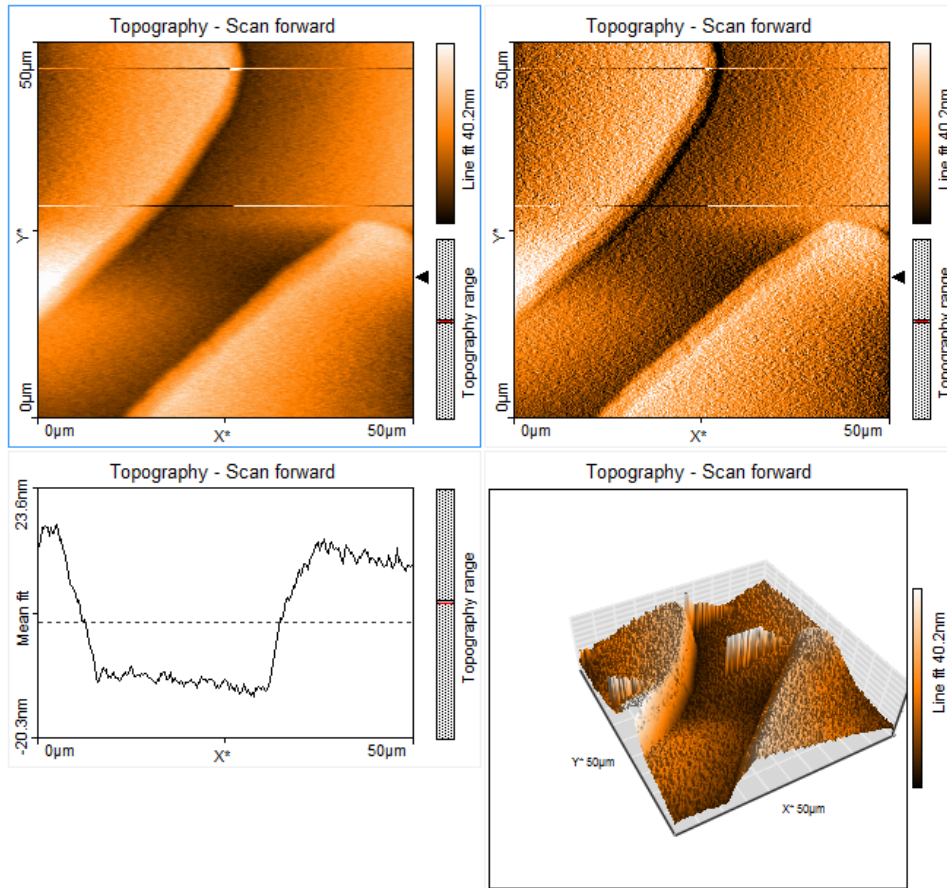


Figure 7.4: Gap between the source and drain electrode - AFM scan

This is an AFM scan of on end of the gap between the source and drain electrode. The source and drain electrodes were deposited through a shadow mask on a sputtered  $\text{SrTiO}_3$  film. The gap on the bottom of the channel was about  $15 \mu\text{m}$  while the gap at the top was about  $20 \mu\text{m}$ . This indicates a half-shade area of only  $2.5 \mu\text{m}$ . The relevant channel length in a TFT is the length at the interface to the dielectric, in our case this was accordingly  $15 \mu\text{m}$ .



# Chapter 8

## Field-effect measurements

In this chapter the electronic measurements of the devices are reported. They consist of measurements of the dielectrics, the response and the transfer curves of the field-effect transistors.

### 8.1 FET measurement preparation

By combining the deposition techniques from the previous chapters thin film field-effect transistor devices were realized. The first step was always the preparation of a dielectric layer. A bottom contact device was created by depositing the contacts before the organic layer. Alternatively a top contact geometry was realized by depositing the organic thin film in the second and the contacts in the last step.

Field-effect transistors in thin film geometry with CuPc as active layer and SrTiO<sub>3</sub> as dielectric were prepared in-situ on Nb doped SrTiO<sub>3</sub> substrates. Additionally, transistors on Si-SiO<sub>2</sub> with CuPc were also prepared for comparison. The source and drain electrodes were made of gold by evaporation through shadow masks. The shadow masks used to prepare the FETs (one mask for the gold source and drain contacts and one mask for the active layer) had a four-segment arrangement. That is, there were always four (identical) transistors prepared, one in each "sector" of the substrate. A successfully prepared transistor is shown in Fig. 8.1. To measure the electronic properties of the transistors, a reliable setup was required. The gate, source and drain electrodes of each of the four transistors on a substrate had to be connected to measurement equipment so that voltages could be applied and currents could be measured. The connection to the measurement setup was realized with a carrier chip (Fig. 8.2). This chip was designed like a small circuit board with 24 contacts. The contacts were soldered to contact pins which were used

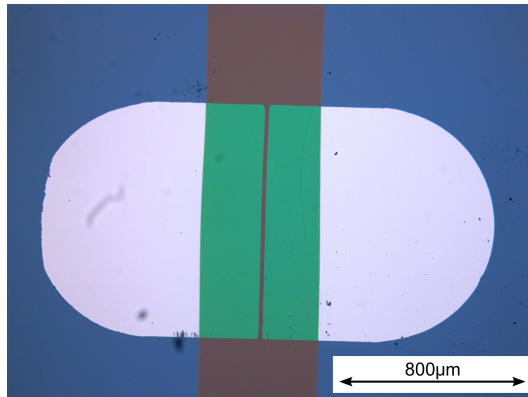


Figure 8.1: CuPc-FET

Microscope picture of a field-effect transistor with CuPc as active layer and gold source drain contacts. The structures were defined by shadow masks. The channel length was 20 μm, channel width 1 mm.

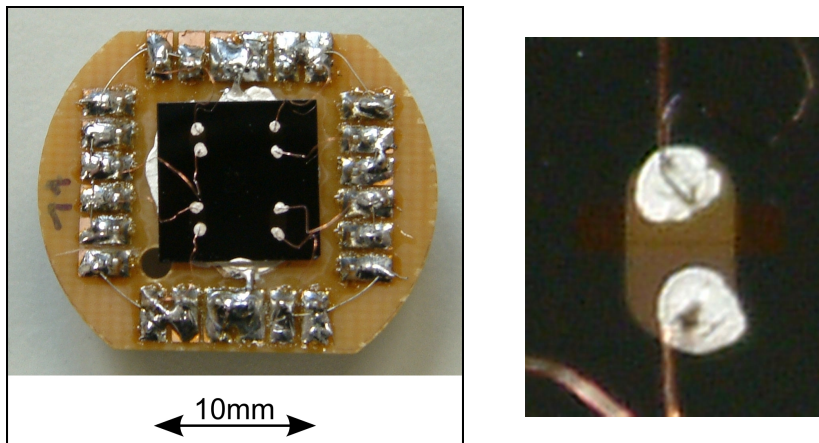


Figure 8.2: FET on carrier for measurements

Carrier chip for electronic measurements with mounted FET sample and a magnification of one of the four transistors with silver contacted copper wires.



to attach the chip to a fixture, connecting it electrically and mechanically to the measurement devices. A small metal plate was glued to the center of the chip and soldered to the pins designated for the gate contact. The Nb doped SrTiO<sub>3</sub> had the function of the gate of the transistors and was contacted with conductive silver paint to the metal plate. On the carrier chip itself thin copper wires were soldered to the contacts and used to connect the pins to the source and drain electrodes on the substrate. The copper wires were bent to the gold source and drain electrodes and tiny drops of conductive silver were applied by hand to provide the mechanical and electric contact. This manual contact preparation required some practicing but allowed for reliable contacts once the process was mastered, although the area where the silver paint was applied often spilled over the drain or source area defined by the gold contacts. One wire was attached to each source and drain electrode on the substrate. On the chip the pin to which the wire was connected was also connected to additional contacts. Therefore the "chips" could be measured in four wire geometry. The carrier chip was also compatible to the fixture on the top-loading probe of the cryostat [97], which allowed for measurements at low temperatures.

The dielectric layer was characterised and  $I - V$  and transfer characteristics were measured ex-situ at room temperature. The measurements were performed with a Keithley sourcemeter, multimeter and electrometer on a custom-built chip holder. The measurements were recorded with a PC. The measurement programs were written in the Python programming language. In the course of the measurements the measurement programs were further developed to allow for the automatic complete mapping of the transistor characteristics, i.e. transfer and output curves for different voltages in a batch process.

## 8.2 FET measurements

For the measurement of the field-effect transistors it is crucial to verify that the dielectric layer is not leaky. Therefore the first measurements made on the transistor structures consisted of resistivity measurements between source-gate and drain-gate, respectively. Here a DC voltage between, e.g., source and gate was ramped up and the current was measured. This was then repeated with reversed polarity. An overview over the prepared transistors is reported in table 8.1. As it can be seen from the table, only one third of the SrTiO<sub>3</sub> transistor were working regarding the dielectric. When the dielectric layer was intact, i.e. the leakage currents were below 1 nA<sup>1</sup>, the capacitance of the electrodes was measured with an LCR meter. For the calculations the source/drain electrode

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<sup>1</sup>With a contact size of  $A = 0.893 \text{ mm}^2$  this corresponds to about  $1 \cdot 10^{-7} \text{ A/cm}^2$ .

No.	Date	Dielectric	Layer	Performance
FET1	04.10.2006	SrTiO <sub>3</sub>	CuPc	bad dielectric
FET2	07.11.2006	SrTiO <sub>3</sub>	CuPc	bad dielectric
FET3	21.03.2007	SrTiO <sub>3</sub>	CuPc	bad dielectric
FET4	23.04.2007	SrTiO <sub>3</sub>	CuPc	functional
FET5	12.07.2007	SrTiO <sub>3</sub>	CuPc	bad dielectric
FET6	27.07.2007	SrTiO <sub>3</sub>	pentacene	bad dielectric
FET7	13.09.2007	SrTiO <sub>3</sub>	CuPc	dielectric allows only small voltages
FET8	18.09.2007	SrTiO <sub>3</sub>	CuPc	bad dielectric
FET9	20.09.2007	SrTiO <sub>3</sub>	CuPc	very bad dielectric
FET10	27.09.2007	SrTiO <sub>3</sub>	CuPc	functional
FET11	05.10.2007	SrTiO <sub>3</sub>	CuPc	functional
FET12	16.10.2007	SrTiO <sub>3</sub>	no layer	working dielectric
FET13	01.11.2007	SiO <sub>2</sub>	CuPc	working dielectric
FET14	05.11.2007	SiO <sub>2</sub>	CuPc	not measured
FET15	22.11.2007	SiO <sub>2</sub>	CuPc	functional
FET16	11.12.2007	SrTiO <sub>3</sub>	ET-TCNQ	active layer not functional

Table 8.1: FET table

In this table the prepared FETs and FET structures (without active layer) are reported. The dielectric was regarded as working when at least a few volt could be applied without a current flow above 1 nA. The transistor was regarded as functional when response curves could be measured.

area was used. When the capacitance of source and drain electrode together was measured, the value approximately doubled as expected. The values from the four sectors were very similar. From the capacitance measurement the dielectric constant of the dielectric layer was calculated. The thickness of the layer, required for this calculation, was estimated from measurements of the deposition rate of reference films, since the thickness of the dielectric layer in the devices could not be measured by X-ray reflectometry. The reason were that Kiessig fringes require a different density of substrate and film and a film thickness smaller than 300 nm [81]. The data are summarized in table 8.2. The values obtained for  $\kappa$  from the transistors with SrTiO<sub>3</sub> as the dielectric layer were all much higher than the value of SiO<sub>2</sub>, but significantly lower than bulk SrTiO<sub>3</sub> and they showed a large variation. The FETs number 10 and 11, for example, were prepared with nominally identical deposition conditions of the dielectric, but the resulting capacitance differed by a factor of two. For

Number	Dielectric	Capacitance	Thickness	kappa
FET4	SrTiO <sub>3</sub>	3.9E-09F	390nm	192
FET6	SrTiO <sub>3</sub>	5.3E-09F	265nm	262
FET10	SrTiO <sub>3</sub>	1.8E-09F	460nm	89
FET11	SrTiO <sub>3</sub>	3.7E-09F	460nm	183
FET12	SrTiO <sub>3</sub>	3.9E-09F	500nm	192
FET13	SiO <sub>2</sub>	1.6E-10F	nom. 300nm	4.5
FET15	SiO <sub>2</sub>	1.6E-10F	nom. 300nm	4.5

Table 8.2: Capacitance table

In this table the measured capacitance, calculated thickness from a reference film and resulting dielectric constant for several films are summarized. The listed values of the capacitance resulted from measurements from source or drain electrode versus gate. The area of source or drain electrodes was  $8.93 \cdot 10^{-7} \text{ m}^2$ .

the transistors on Si-SiO<sub>2</sub> the nominal thickness of the dielectric was 300 nm. To calculate mobilities from the FET characteristics the capacitance per unit area was required, which was calculated from the measured capacitance and the area of the electrodes. Thereafter the response characteristics of the transistors were measured. The gate voltage was fixed and the source drain voltage was varied. Transistors were measured multiple times consecutively, each time increasing the gate voltage and, when possible (i.e. at sufficiently low leakage currents), also to higher drain voltages. When in the following "increasing" or "larger" voltages are discussed this refers to the absolute value of the voltages<sup>2</sup>. The voltages were usually ramped up and down slowly and often a hysteresis was observed. Finally, the transfer curves were measured. Different source drain voltages were fixed and the gate voltage was ramped up and down and also a hysteretic behaviour was observed. During the response and transfer measurements the source gate leakage currents were monitored and recorded. A hysteresis behaviour in organic FETs is not uncommon and usually related to trapped charges [98].

### 8.3 CuPC FETs

Several FETs with CuPc as the active layer were successfully prepared. The first devices were prepared in TFT bottom contact configuration since it was speculated that the high temperatures during gold contact deposition might damage the organic layers. Later also top contact devices were tested with

<sup>2</sup>For *p*-type semiconductors the gate and the drain voltage are usually negative.

good results. The first successfully prepared transistor was the CuPc FET No. 04. The current voltage characteristic is shown in Fig. 8.3. The characteristic clearly showed *p*-type field-effect behaviour with the peculiarity that the saturation drain current did not increase as strongly as expected for larger gate voltages. Usually, from the current voltage curve the mobility can be calculated, as introduced in section 3.2.1, in the saturation regime by

$$\mu = \left( \frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \cdot \frac{2L}{C_I W}. \quad (8.1)$$

In the linear regime the mobility is obtained from the transfer curve by

$$\mu = \frac{\partial I_D}{\partial V_G} \cdot \frac{L}{W C_I V_D} \quad (8.2)$$

or from the slope of a plot, where the slopes of the response curves in the linear regime at constant gate voltage are plotted over gate voltage by

$$\mu = \frac{\partial I_D}{\partial V_D} \cdot \frac{L}{W C_I (V_G - V_T)}. \quad (8.3)$$

The method to extract the mobility from the linear regime of the current voltage characteristic was performed for FET No. 04 in Fig. 8.4. The slopes of the different response curves in the linear regime were determined by a linear fit. The different slopes were then plotted versus the corresponding gate voltages. A subsequent linear fit of this plot yielded the mobility in the linear regime, for FET 4 a mobility of  $\mu = 5.0 \cdot 10^{-4} \text{ cm}^2/\text{Vs}$  was derived.

The mobility in the saturation regime was also determined. The corresponding graph is pictured in Fig. 8.5. Here the square root of the saturation currents were plotted versus the gate voltage. For the saturation current, the current obtained at  $V_D = -3 \text{ V}$  was used - this was the highest drain voltage which was measured. Although a saturation of the drain current was not fully obtained, as it can be seen from Fig. 8.3, the slopes of the response curves were relatively flat. The mobility in the saturation regime ought to have been obtained from a linear fit of the square root of the saturation currents, but for FET 4 clearly two regions had to be distinguished, i.e. a different slope was obtained for small and for larger gate voltages. Therefore also two different mobilities were extracted. For gate voltages between  $V_G = 0 \text{ V}$  and  $-1 \text{ V}$  the obtained mobility was  $\mu = 1.9 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$ , for larger gate voltages  $\mu = 1.4 \cdot 10^{-4} \text{ cm}^2/\text{Vs}$  was extracted. This was a surprisingly large difference of one order of magnitude. It is notable that the larger mobility was obtained for smaller gate voltages. Commonly in the literature the opposite was observed and the fit to the data was performed for the largest gate voltages. A reason for that behaviour could

### CuPc-FET with SrTiO<sub>3</sub> gate dielectric

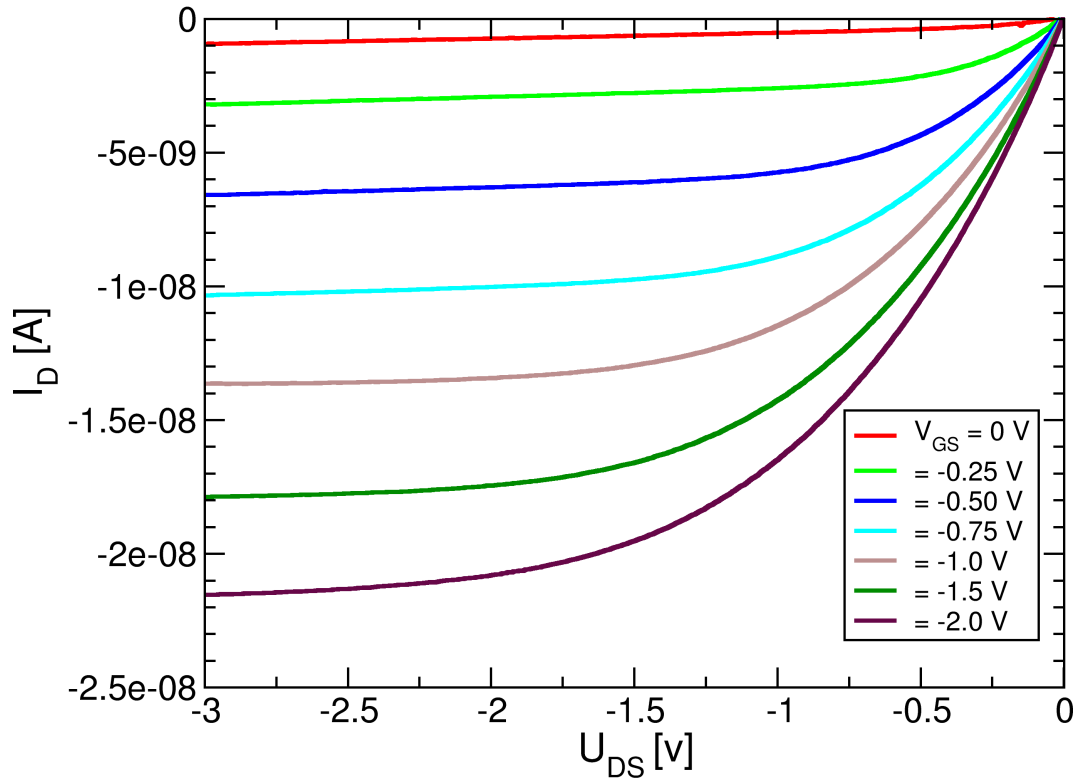


Figure 8.3: Response curves of a CuPc FET

This is a current voltage characteristic of the first successfully prepared CuPc FET (No. 04) with SrTiO<sub>3</sub> as dielectric layer. This FET was prepared in bottom contact configuration, i.e. the gold contacts were deposited before the CuPc. Substrate temperature during the deposition of the CuPc film was 85 °C. The CuPc film was very thin. The exact thickness could not be measured in the device structure, but from optical comparison to reference films with the microscope and measurements from the quartz micro balance the thickness was estimated to about 15 nm. The transistor showed *p*-type behaviour. The linear region could be clearly distinguished from the saturation region. With increasing negative gate voltage the drain current increased, but this increase was smaller than expected for larger voltages. An increase from  $V_G = -1.5$  V to  $V_G = -2$  V should have resulted in a stronger drain saturation current increase than the increase from  $V_G = -1$  V to  $V_G = -1.5$  V, but the opposite was observed.

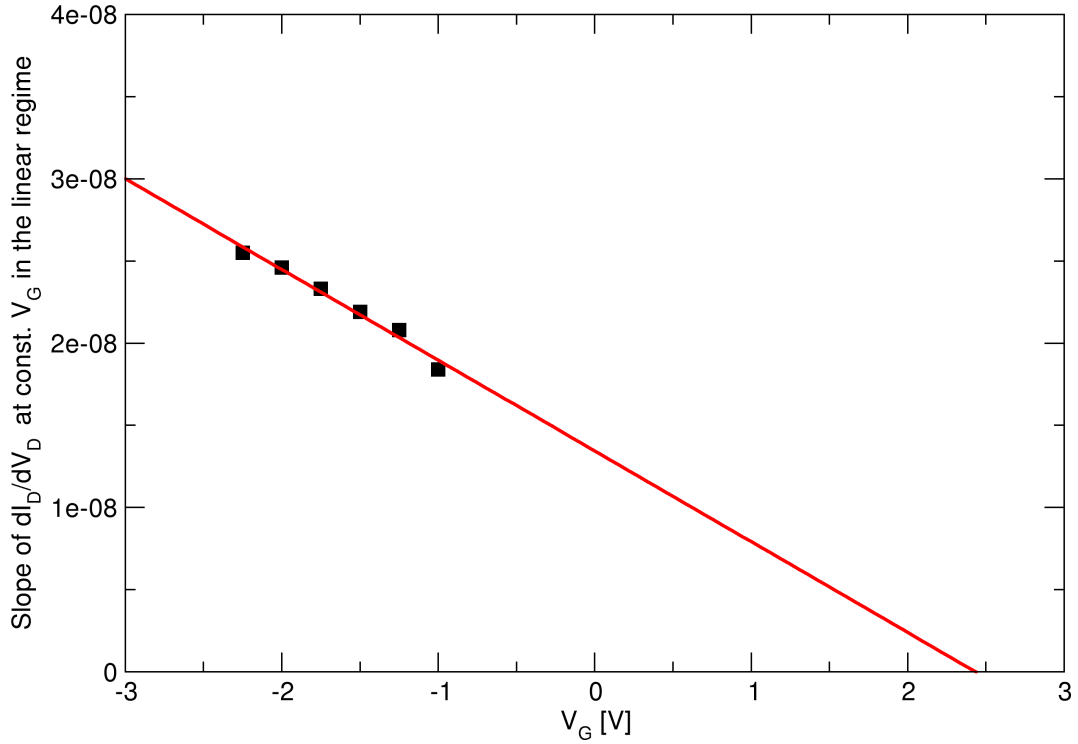


Figure 8.4: Mobility in the linear regime

In this figure the slopes of the drain current over the drain voltage  $dI_D/dV_D$  as a function of the gate voltage  $V_G \gg V_D$  (linear regime) are shown for CuPc FET (No. 04). From the linear fit the threshold voltage was estimated by the x-axis intercept to  $V_T = 2.44$  V and the mobility can be derived from the slope to  $\mu = 5.0 \cdot 10^{-4}$  cm<sup>2</sup>/Vs.

have been a decrease of  $\kappa$  and therefore of the capacitance with an increasing electric field (gate voltage).

Finally, the mobility was extracted from a transfer curve, as pictured in Fig. 8.6. Here a mobility of  $3.3 \cdot 10^{-4}$  cm<sup>2</sup>/Vs was obtained from the slope.

Summing up the results from FET 4, varying mobilities in dependence of gate voltage and measurement method were found. As the highest mobility determined for this transistor  $\mu = 1.9 \cdot 10^{-3}$  cm<sup>2</sup>/Vs was calculated. The device showed a clear field effect behaviour but deviated from the expected properties at higher gate voltages.

A FET with more regular characteristics than FET 4 was obtained with FET 11. This FET was prepared in top contact configuration and the response curve in Fig. 8.7 (obtained from sector 4) showed regular field-effect properties. Compared to FET 4 the drain current increased stronger with increasing gate voltage, as expected. For positive gate voltages the conduction was suppressed

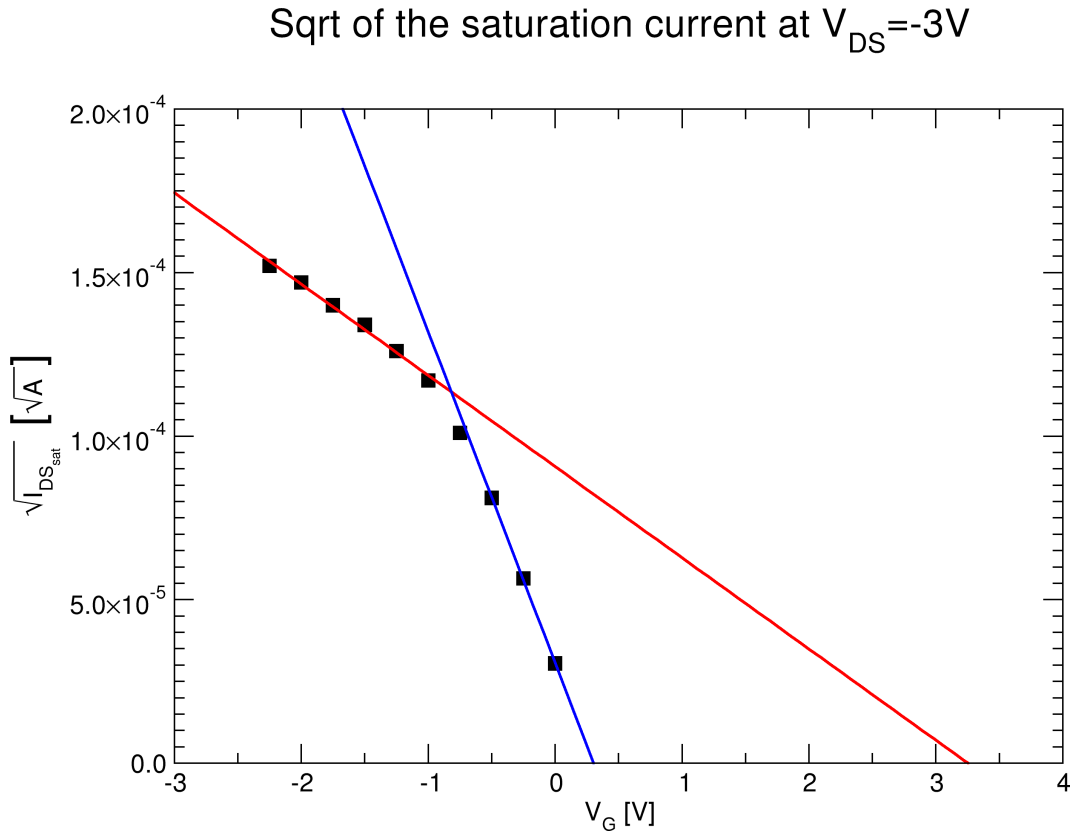


Figure 8.5: Mobility in the saturation regime

In this figure the square root of the saturation current at  $V_D = -3$  V as a function of the gate voltage is shown. There are two linear fits, one at lower gate voltage (blue curve) and one at higher gate voltage (red curve). From the linear fits the threshold voltage were estimated by the x-axis intercept to  $V_T = 3.25$  V for high gate voltages and  $V_T = 0.3$  V at low gate voltages. The mobility was derived from the slopes to  $\mu = 1.4 \cdot 10^{-4}$  cm<sup>2</sup>/Vs for high gate voltages and  $\mu = 1.9 \cdot 10^{-3}$  cm<sup>2</sup>/Vs for small gate voltages.

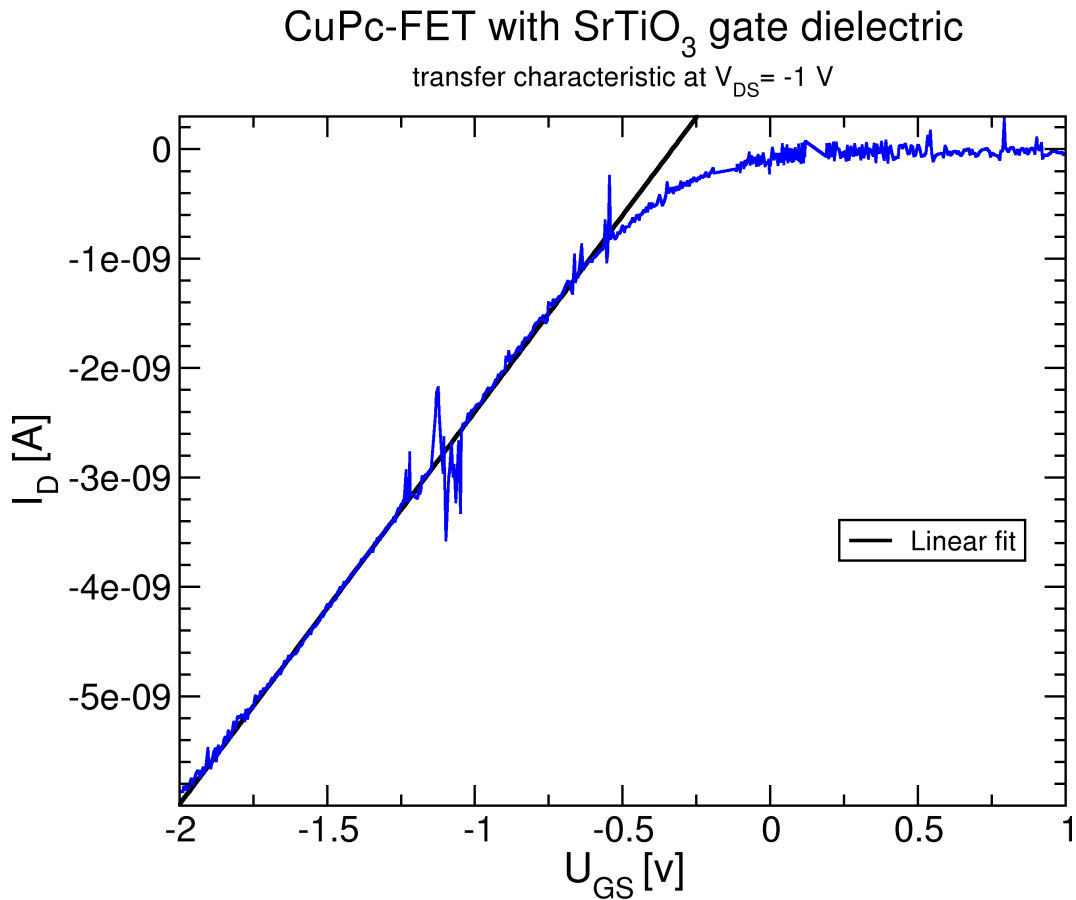


Figure 8.6: Transfer curve of a CuPc-FET with SrTiO<sub>3</sub> as the dielectric layer

In this figure a transfer curve of the first successfully prepared CuPc FET (No. 04) with SrTiO<sub>3</sub> as dielectric layer is presented. From the linear fit the mobility was derived from the slope to  $\mu = 3.3 \cdot 10^{-4}$  cm<sup>2</sup>/Vs. The channel width in this device was only about 0.5 mm due to a bad alignment of the shadow masks.

and the drain current decreased below the zero gate voltage current, which was interpreted as a depletion behaviour. Saturation was hardly obtained for drain currents exceeding the gate voltage. This indicated a negative build in zero (threshold) voltage which biased the transistor. This FET had a "on/off ratio" of about  $10^3$ , which is comparable to literature results [36]. The mobility for this transistor was derived in the same way as for FET 4.

The mobility obtained in the linear regime was derived from transfer curves in Fig. 8.8. All sectors of this FET were separately measured over the course of several days. The first measured device was in sector 1. Compared to the



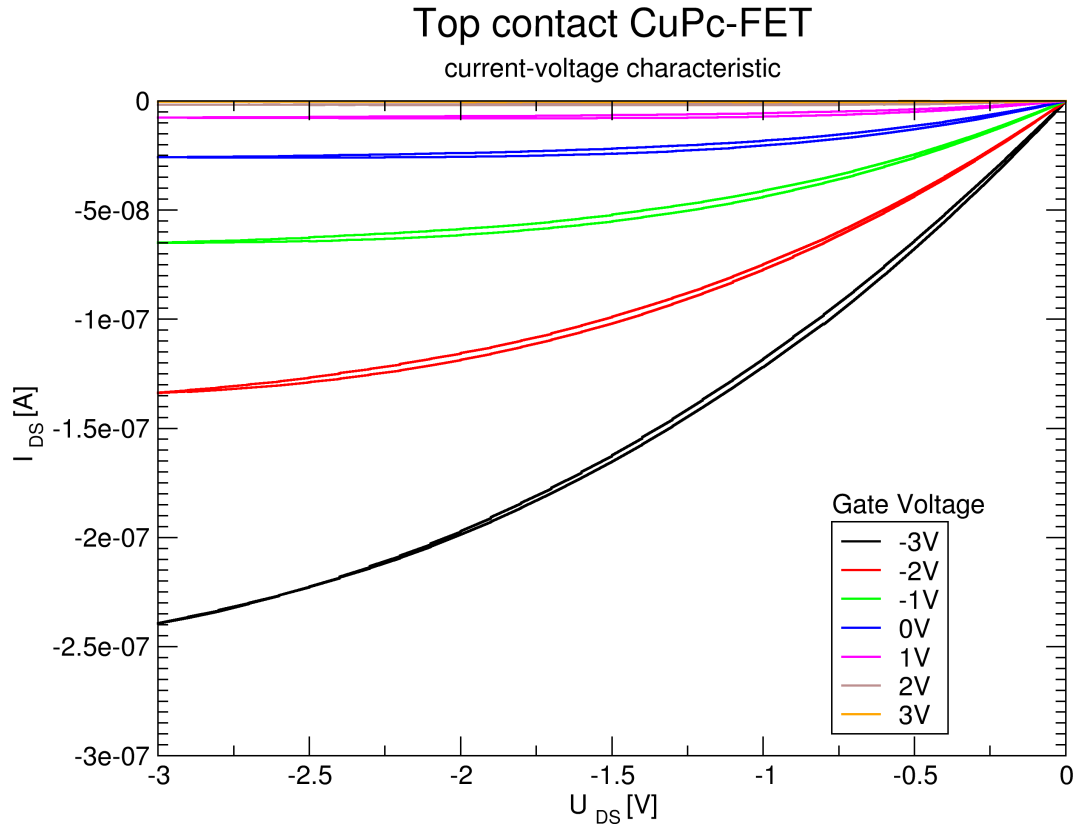


Figure 8.7: Current voltage characteristic of a CuPc-FET with SrTiO<sub>3</sub> as the dielectric layer

This was a current voltage characteristic of a successfully prepared CuPc FET (No. 011) with SrTiO<sub>3</sub> as dielectric layer. This FET was prepared in top contact configuration, i.e. the CuPc layer were deposited before the gold contacts. Only low voltages were necessary to achieve a pronounced modulation of the source drain current. The "on" current at  $-3$  V source drain and gate voltage was  $2.4 \cdot 10^{-7}$  A. The "off" current at  $-3$  V source drain voltage and  $0$  V gate voltage was  $(2.5 \cdot 10^{-8}$  A) and was further suppressed to  $3.5 \cdot 10^{-10}$  A with a gate voltage of  $3$  V. The "on/off ratio" was about  $10^3$ .

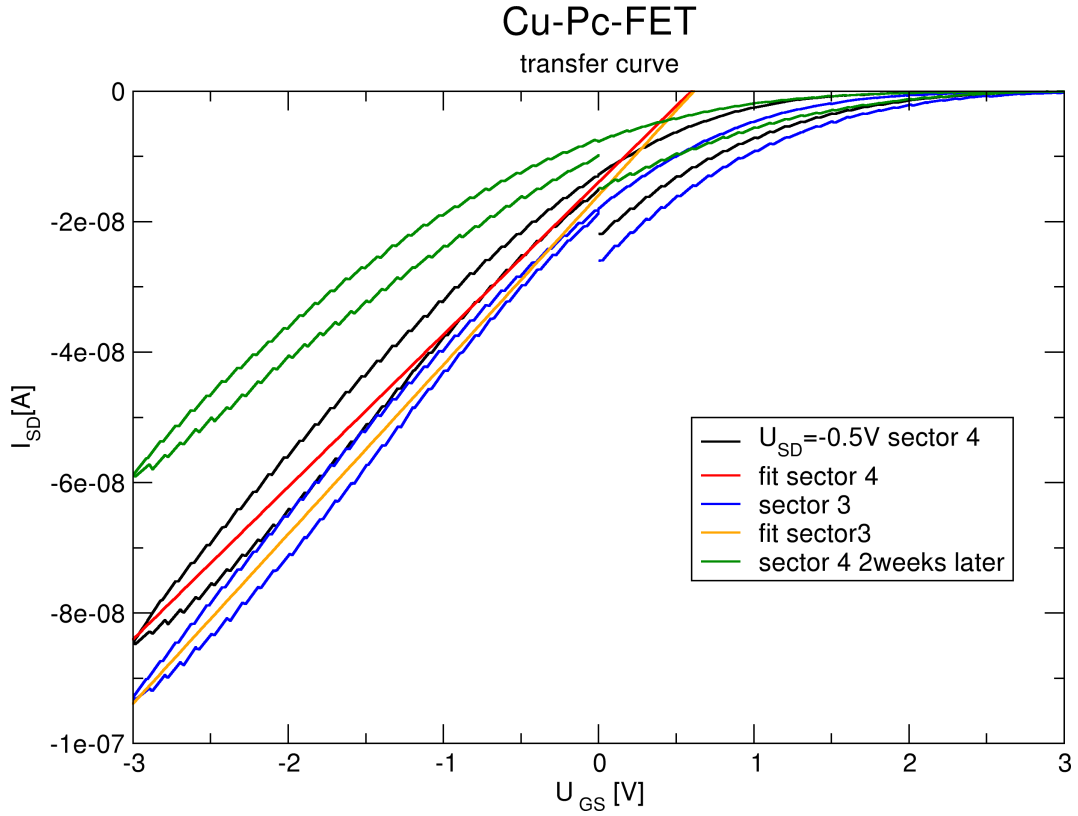


Figure 8.8: FET 11 Mobility in the linear regime

This plot shows transfer curves at small drain voltage of  $-0.5$  V for CuPc FET 011. The black and blue curves were recorded from different sectors (sector 3 and sector 4), measured on consecutive days. Sector 4 was remeasured 2 weeks later with a significantly reduced response. The mobilities were extracted from the slopes of the curves. For sector 3 a mobility of  $\mu = 1.9 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$  was obtained from the fit, while the mobility of sector 4 was calculated to  $\mu = 1.7 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$ . The sawtooth behaviour in the plot is caused by the measurement routine. The gate voltage is ramped, but the measured gate voltage and the drain current are recorded. The measurement is performed four times for each preset gate voltage and the values are slightly changing. The measured gate voltage approaches the set point, while the absolute value of the drain current slightly decreases/increases when the gate voltage is ramped up/down.

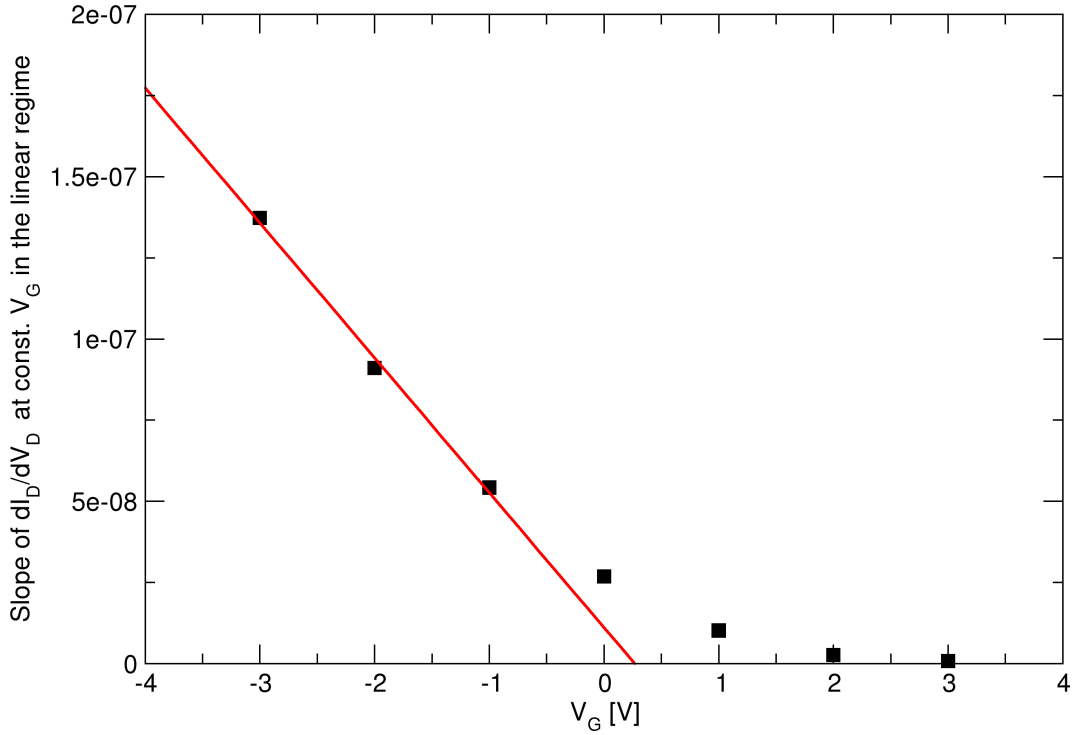


Figure 8.9: FET 11 Mobility in the linear regime from the response curve

In this figure the slopes of the drain current over the drain voltage  $dI_D/dV_D$  as a function of the gate voltage  $V_G \gg V_D$  (linear regime) are shown for CuPc FET (No. 11). From the linear fit the threshold voltage was estimated by the x-axis intercept to  $V_T = 0.27$  V and the mobility was derived from the slope to  $\mu = 1.5 \cdot 10^{-3}$  cm<sup>2</sup>/Vs.

curves of sector 3 and 4 it showed lower response and had a higher leakage current through the dielectric. Sector 2 was measured next, with a transfer curve in between sector 3 and 4, but also had relatively high leakage current through the dielectric of about 7.5 nA at a gate voltage of  $V_G = -3$  V. Sector 3 which was measured next showed the highest mobility of the four sectors with  $\mu = 1.9 \cdot 10^{-3}$  cm<sup>2</sup>/Vs, the measured leakage current was one order of magnitude lower with 0.75 nA for  $V_G = -3$  V. The mobility of the device in sector 4, measured one day later was calculated to  $\mu = 1.7 \cdot 10^{-3}$  cm<sup>2</sup>/Vs with an even lower leakage current of  $1.5 \cdot 10^{-10}$  A. Overall, it was concluded that the devices in the four sectors showed very similar results, when the dielectric is intact. Furthermore, it was observed that the electronic properties of the devices changed over time. Sector 4 for instance was remeasured 2 weeks later and showed lower response, but also a decrease in leakage current to

### Sqrt of the saturation current at $V_D = -3V$

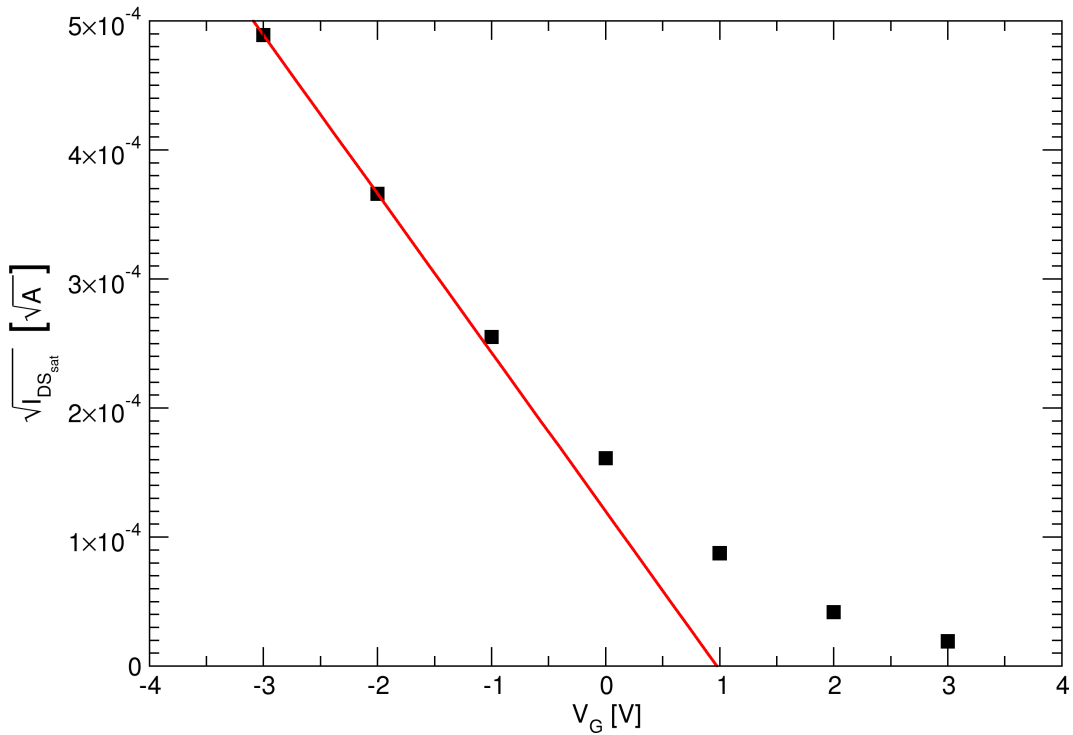


Figure 8.10: FET 11 Mobility in the saturation regime

This plot shows the square root of the saturation current at  $V_D = -3$  V as a function of the gate voltage for CuPc FET 011, sector 4. The mobility was obtained from a fit at the highest gate voltage to  $\mu = 1.1 \cdot 10^{-3}$  cm<sup>2</sup>/Vs and the threshold voltage to  $V_T = 0.98$  V. In contrast to FET 4 (Fig.8.5) the common increasing slope with gate voltage was found.

$7 \cdot 10^{-11}$  A. A deterioration of device properties is not uncommon in organic FETs and usually attributed to oxidation.

The second method to obtain the mobility in the linear regime was also used. The slopes of the response curves were determined for small drain voltages. A plot of the derived slopes is presented in Fig. 8.9. From a fit to these values a mobility of  $\mu = 1.5 \cdot 10^{-3}$  cm<sup>2</sup>/Vs and a threshold voltage of  $V_T = 0.27$  V was calculated.

The mobility was also extracted from the saturation current as depicted in Fig. 8.10. The currents at  $V_D = -3$  V were obtained from the response curves from Fig. 8.7. The square roots of these currents were then plotted over gate voltage and from the slope the mobility was calculated to  $\mu = 1.1 \cdot 10^{-3}$  cm<sup>2</sup>/Vs

and the threshold voltage to  $V_T = 0.98$  V. The plot showed the typical increase in slope towards higher gate voltages.

In conclusion FET 11 showed typical field-effect behaviour. The values derived for mobility in the linear and the saturation regime were fairly close together, around  $\mu = 1.5 \cdot 10^{-3}$  cm<sup>2</sup>/Vs. These mobilities were not exceptionally high, but the growth of the CuPc layer was not yet optimized with respect to transport properties. In the literature the highest mobilities of  $\mu = 1.5 \cdot 10^{-2}$  cm<sup>2</sup>/Vs were reported for a substrate temperature of 150 °C [36]. Unfortunately the device lacked (long term) stability under ambient conditions. Finally, the field-effect transistors prepared on SrTiO<sub>3</sub> were compared to FETs with a commercial SiO<sub>2</sub> dielectric layer. A response curve of such a transistor (FET 15) is shown in Fig. 8.11. The off current was very high compared to the SrTiO<sub>3</sub> devices and much higher gate voltages were necessary for a (moderate) modulation. The response curves of this CuPc-FETs showed no saturation in source drain current. This could be interpreted as an Ohmic current in parallel with the channel current which is expected for thick layers, but the thickness of the CuPc layer was also only 40 nm which was about as thick as on the FETs with SrTiO<sub>3</sub> as the dielectric layer. Also, since saturation of the source drain current is expected above the gate voltage for the channel current, the increase of the current should have had the same slope when the channel current saturated. A mobility for the saturation regime could therefore not be extracted. From transfer curve measurements a mobility in the linear regime of about  $\mu = 1.5 \cdot 10^{-4}$  cm<sup>2</sup>/Vs could be obtained for source drain voltages of  $-1$  V and  $-3$  V. In comparison to the best devices with SrTiO<sub>3</sub> (FET 11) dielectrics the performance of the SiO<sub>2</sub> based transistor was poor.

Experiments to cool down the FETs to deeper temperatures were also performed, but several problems were encountered. The low temperatures reduce the conductivity of the CuPc layer and the dielectric SrTiO<sub>3</sub> had a lower breakdown voltage. When the capacitance of the dielectric alone was measured with an LCR meter no dramatic changes, especially no strong increase as reported for bulk SrTiO<sub>3</sub>, were observed. A measurement of the capacitance vs. temperature is depicted in Fig. 8.12. In summary the potential of SrTiO<sub>3</sub> as dielectric layer could be demonstrated for organic field-effect transistors. The drawback was the poor yield of the sputtering process which resulted more often than not in an insufficient dielectric layer. When a FET was prepared successfully, only small voltages were necessary to induce charges in the active layer and modulate the conductance of the channel. The highest mobility were close to  $\mu = 2 \cdot 10^{-3}$  cm<sup>2</sup>/Vs without optimization. An "On/off ratio" of about  $10^3$  was reached.

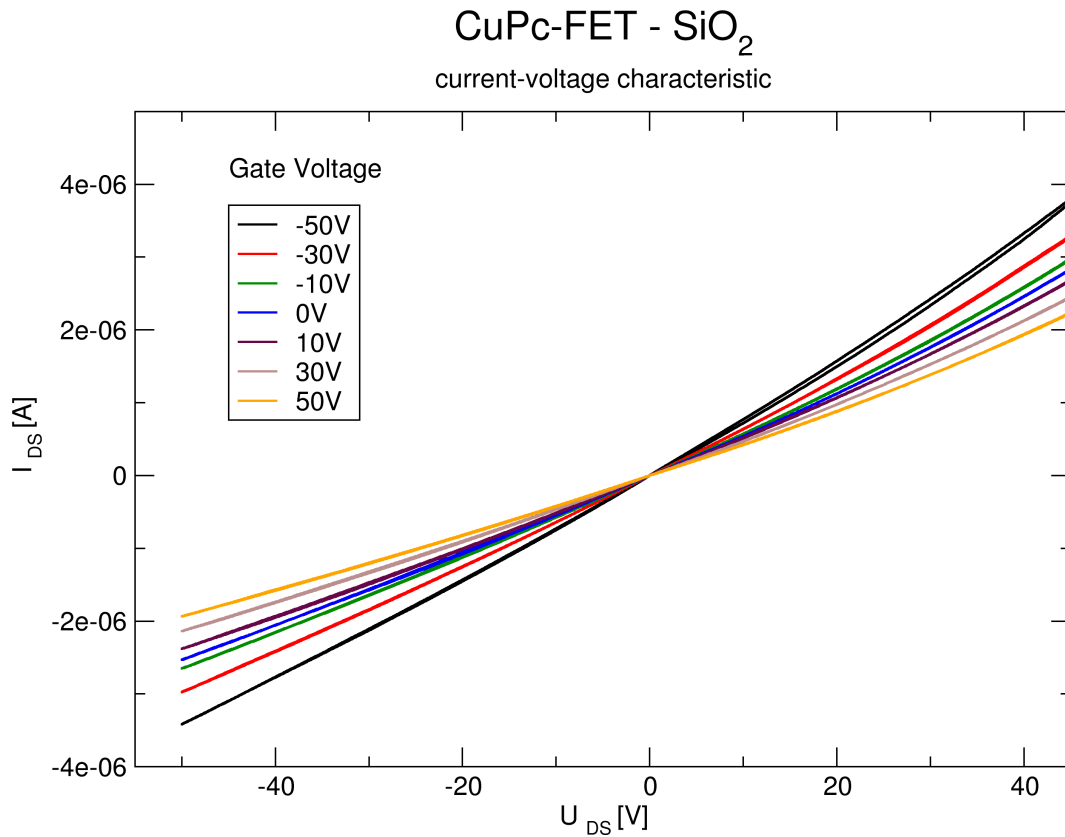


Figure 8.11: Current voltage characteristic of a CuPc FET with SiO<sub>2</sub> as the dielectric layer

This FET 15 was prepared on a commercial Si-SiO<sub>2</sub> substrate. It was used as a reference CuPc-FET with SiO<sub>2</sub> as dielectric layer. The CuPc layer of about 40 nm was deposited before the contacts, resulting in a top contact structure. The off current was very high compared to the SrTiO<sub>3</sub> devices and much higher gate voltages were necessary for a modulation.

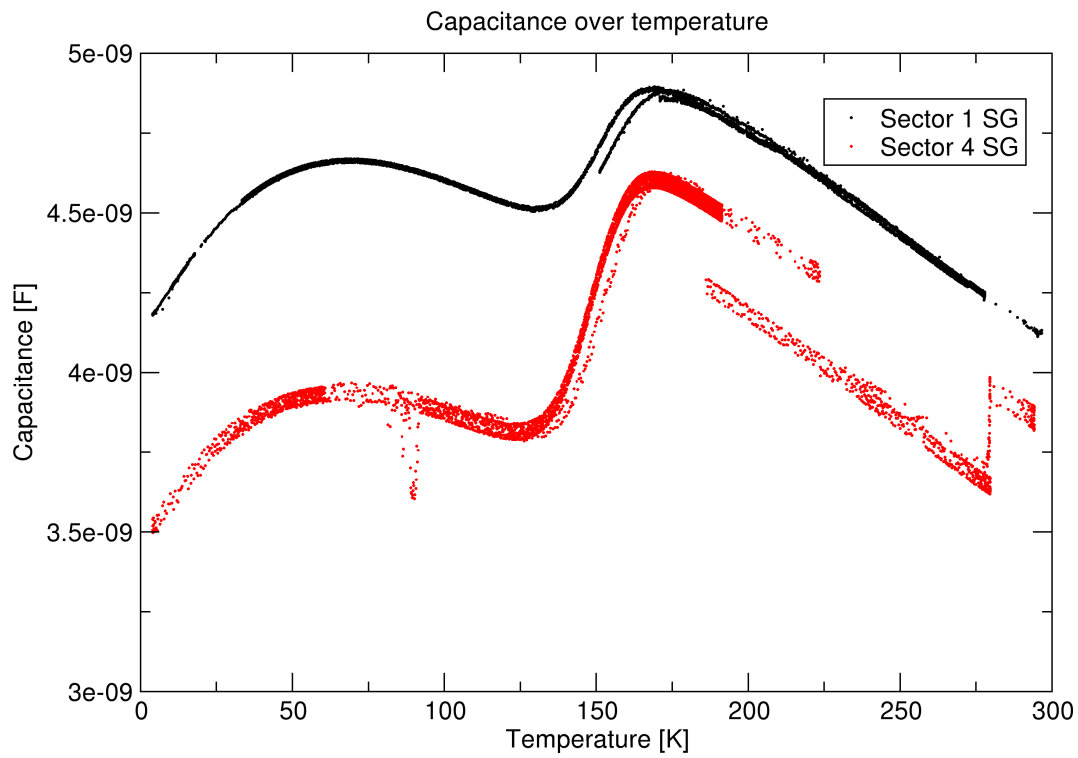


Figure 8.12: Capacitance of source versus gate electrodes from FET 11

FET 11 was mounted on the top-loading probe of the cryostat and the capacitance of a single source electrode versus the gate electrode was measured at different temperatures. The values from sector 1 were measured over three days. The capacitance changed only slightly with temperature. The measurement of sector 4 showed repetitive jumps in the capacitance measurement of unknown origin.





# Chapter 9

## Summary and Outlook

During this thesis work significant progress was made towards the long-term goal: Realizing FETs, where the active layer is an organic semiconductor or charge transfer salt, with high mobilities ( $\geq 1 \text{ cm}^2/\text{Vs}$ ) and the possibility to reach high sheet charge densities in these devices.

The main prerequisites to realize this goal are the preparation of a high- $\kappa$  dielectric layer with high quality and the optimization of an organic layer, deposited in a controlled UHV environment.

To enable the preparation of complete devices, an UHV chamber system for the growth of all layers - dielectrics, organic thin films and contacts - was designed and put into operation. Due to the different requirements of the used materials the system was designed in a modular fashion so that the single deposition processes for FET preparation take place in distinct chambers. The main focus in this thesis was the construction and assembly of this chamber system and the preparation of the dielectric layer.

As high- $\kappa$  dielectric  $\text{SrTiO}_3$ , and as deposition method RF sputtering were selected. For the deposition a sputtering chamber was set up and a manipulator with the capability to heat the samples up to about  $900 \text{ }^\circ\text{C}$  in oxygen atmosphere was developed. The impact of the sputtering parameters, like pressure, temperature, gas mixture or sputtering power on the deposition process was studied. The growth of sputtered  $\text{SrTiO}_3$  was characterized with X-ray diffraction and optical microscopy and optimized with respect to high crystallinity, a smooth surface and a sufficient growth rate. A set of parameters to allow for FET preparation was found. In devices the dielectric constant of the dielectric layer was estimated to about 190 with a thickness of about 500 nm in the best transistors.

To allow for the preparation of organic semiconductors or charge transfer salts as thin films by means of evaporation, a new UHV chamber and most of the hardware such as a manipulator which could be heated, cooled and rotated

and various effusion cells with different designs were constructed.

Growth studies were performed on pentacene,  $\text{Cl}_{16}\text{CuPc}$  and in particular on  $\text{CuPc}$ . For  $\text{CuPc}$  the substrate temperature had a major influence on the crystallinity of the films, as observed with X-ray diffraction. For the FET structures in-situ preparation was realized by a shadow mask system, where masks could be transferred onto the sample holder and used in the different chambers. This enabled structured deposition of the films down to structure sizes of  $20\ \mu\text{m}$ .

For the transistor preparation the combination of  $\text{SrTiO}_3$  as dielectric,  $\text{CuPc}$  as semiconducting layer and gold as drain and source electrode was chosen. The equipment and software for the measurements of the devices was established. The response and transfer curves of the transistors were measured. The  $\text{CuPc}$  transistors showed a  $p$ -type conduction behavior with an increase of the source drain current with negative gate voltage. The mobilities in the devices reached  $\mu = 2 \cdot 10^{-3}\ \text{cm}^2/\text{Vs}$  and "on/off ratios" of about  $10^3$  were achieved with low driving voltages of  $\pm 3\ \text{V}$ . Due to the higher polarization of the  $\text{SrTiO}_3$  much higher response in comparison to reference FETs prepared on  $\text{Si-SiO}_2$  substrates could be observed, which was an expected result. The observed mobilities are lower than the best values reported in the literature, which can be attributed to the fact that the growth of the organic layer on  $\text{SrTiO}_3$  has not been optimized with respect to the mobility, yet.

The preparation system which was constructed during this work allows for a variety of further studies.

First of all different organic materials can be used as active materials. As one example, the family of phthalocyanines e.g. allows for controlled modifications of the ionization potential and can be studied further, but also different molecule classes, charge transfer compounds or organic superconductors can be used in field-effect studies. To improve the quality of the organic layer purification of the source material before evaporation can be added as a preparation step and detailed studies of deposition parameters in the OMBD chamber can be performed. Different electrode materials can be used and the influence of the work function on the charge injection can be analyzed. Using the transferable shadow mask system the preparation of the source and drain contacts can even take place in the metal MBE chamber and the materials available there can be used.

The transistor structures up to now all have the same channel length of  $20\ \mu\text{m}$ . To study the influence of the channel length additional masks can be constructed. It is also possible to combine four transistors with different channel length on one substrate so that the preparation conditions are identical for all transistors.

Another but more complicate upgrade would include in situ measurements of the prepared devices to prevent oxidation of the organic layer. This would require an extension of the vacuum system with an additional chamber which is challenging but possible.

In summary the modular preparation setup with dedicated chambers for different functions and the transferable shadow mask system allow for a variety of further experiments.



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# Appendix A

## Sputtered films

Table of the sputtered SrTiO<sub>3</sub> films with sputtering conditions and resulting thickness.

No	substrat	T°C	P[W]	Ar	O2	pkk mbar	t min	d nm
1	alo a-plane	600.00	20	-	-	0.004	20	53
2	random	700.00	20				20	26
3	A-plane	800.00	31	5	2.5	0.003-0.005	20	
4	A-plane	700.00	20	8	-	0.003	20	44
5		700.00	20	4	4	0.001	20	
6	A-plane	700.00	60	4	4	0.001	20	22
7	A-plane	700.00	20	7	1	0.001	20	13
8	R-plane;mgo	700.00	20	7.5	0.5	0.001	30	25
9	R-plane	700.00	40	7.5	0.5	0.001	30	73
10	R-plane	700.00	40	15	1	0.055-0.035	30	76
11	R-plane	700.00	40	15	2	0.107-0.185	30	37
12	R-plane	700.00	40	13	2	0.016	30	67
13	R-plane	700.00	40	16	2	0.088	30	53
14	R-plane	700.00	40	10	1		30	60
15	R-plane	700.00	40	10	3.3	0.101	30	67
16	R-plane	700.00	40	16	2	0.141	30	59.5
17	R-plane	700.00	40	15	2	0.120	30	54.2
18	R-plane;2x	700.00	40	15	2		30	54
19	R-plane	700.00	150	8.6	4.3	40-156	20	
20	R-plane;2x	750.00	40	15	2	0.155	30	52
21	R-plane	700.00	90	8.6	4.3	0.020	20	157
22	Alo-r	700.00	60-80	16	2	0.114	30	79
23	Alo-r	700.00	40	14	2	0.055	30	68
24	Alo-r	700.00	40	16	0.2	0.030	30	81
25	Alo-r	700.00	40	5	0	0.000	30	
26	Alo-r	700.00	40	12	0.3	0.010	30	74
27	Alo-r	800.00	40	16	0.2	0.075	30	73.7
28	Alo-r	700.00	40	16	2	0.236	30	39.6
29	Alo-r	800.00	40	16	1	0.145	30	41.4
30	Alo-r	750.00	40	16	2	0.145	30	38

31	Alo-r	800.00	40	15	2.5	0.210	30	26.8
32	Alo-r	800.00	40	16	1.5	0.090	30	58.3
33	Alo-r	800.00	40	16	1.5	0.110	30	55.7
34	Alo-r;sto-001	800.00	40	16	1.5	0.150	30	45
35	Alo-r	800.00	40	5	-	0.000	30	76
36	Alo-r	800.00	40	5	0.5	0.000	30	50.2
37	Alo-r	800.00	40	5	2	0.000	30	59.1
38	Alo-r	800.00	40	16	2	0.248	30	
39	Alo-r	800.00	40	16	2	0.363-0.088	30	33.5
40	Alo-r	750.00	40	9.2	4.5	0.040	30	53.65
41	Alo-r	750.00	40	11.4	3.8	0.055	30	60.58
42	Alo-r	750.00	40	9.1	4.6	0.028	30	55.8
43	Alo-r;sto-001	750.00	40	9.6	4.8	0.065	30	54.8
44	Alo-r;sto-nb	750.00	40	9.7	4.7	0.036	31	61.02
45	Sto-nb	750.00	40	10	5	0.038	30	
46	Alo-r	750.00	20	10	5	0.140	30	14.7
47	Alo-r	750.00	60	10	5	0.150		65.2
48	Alo-r	800.00	60	10	5	0.150		77.4
49	Alo-r	800.00	60	10	5	0.086		111
50	Alo-r	800.00	60	10	5	0.150		64.6
51	Alo-r		60					53.5
52	Alo-r	22.00	40	9.7	4.8	0.036	30	52.6
53	Sto-nb	750.00	40	9.8-9.7	4.8	0.036	120	
54	mgo	750.00	40	9.7	4.8	0.037	30	64.70
55	mgo	750.00	40	9.6	4.7	0.035	30	64.7
56	mgo;alo	750.00	40	-	11.5	0.086	30	31
57	mgo;alo	750.00	60	-	10.5	0.035	30	52.4
58	mgo;alo	750.00	90	-	-	0.860	30	18.7
59	mgo;alo	800.00	120	-	-	1.100	30	14.8
60	mgo;alo	750.00	120	10	0.1	1.200	30	
61	mgo;alo	750.00	100	-	-	1.035	30	14.5
62	mgo;alo	750.00	100	-	13.2	0.175	40	1
63	mgo;alo	750.00	100	-	11.5	1.500	30	
64	mgo;alo	650.00	100	-	12	1.187	32	2.2
65	mgo;alo	750.00	100	10.5	4	1.100	30	4.88
66	mgo;alo	750.00	60	12	3.6	1.400	30	
67	mgo;alo	750.00	100	10.5	4	1.050	195	21
68	mgo;alo	750.00	100	10.5	4	1.050	195	44
69	mgo;alo	750.00	100	10.5	4	1.100	105	
70	mgo;alo	750.00	100	5.5	2	0.180	198	12
71	mgo;alo	750.00	100	16	6	2.475	>30	
72	mgo;alo	750.00	100	15.5	5.5	2.060	90	
73	mgo;alo	750.00	100	15.5	5.5	1.890	120	
74	mgo;alo	800.00	100	15.5	5.5	1.880	120	
75	mgo;alo-r	770.00	100	12	5.5	1.440	120	
76	mgo;alo	550.00	100	12	5.5	1.480	120	
77	mgo;alo	720.00	100	7	4	0.440	120	
78	mgo;alo	730.00	100	15.5	5.5	2.000	137	
79	mgo;alo	730.00	100	16	2.5	1.540	90	

80	mgo;alo	700.00	85	15.5	5	2.100	90	
81	mgo;alo	690.00	100	15.2	0.2	1.050	90	
82	mgo;alo	700.00	85	12	4.5	1.300	45	
83	mgo;alo	700.00	60	7	3.5	0.440	40	34
84	mgo;alo	700.00	60	9	3.5	0.700	40	24
85	mgo;alo	700.00	60	7	5.1	0.700	40	34
86	mgo;alo	700.00	60	8.8	2	0.420	40	42
87	mgo;alo	700.00	60	5	5	0.420	40	38
88	mgo;alo	700.00	60	7.8	2	0.280	40	48
89	mgo;alo	685-666	60	7	3.5	0.410	40	37
90	mgo;alo	640.00	60	7.8	2	0.300	40	48
91	mgo;alo	650.00	60	7.2	1.7	0.170	40	62
92	mgo;alo	650.00	60	6.6	5.6	0.720	40	16
93	mgo;alo	650.00	60	6	5	0.520	40	22
94	mgo;alo	650.00	60-80				>40	44
95	mgo;alo	644.00	60	6.4	1.7	0.110	40	92
96	mgo;alo	725.00	50	0		0.001	?	92
97	mgo;alo	650.00	60	5	3.5	0.250	40	20
98	mgo	650.00	60	3.3	1.1	0.005	40	7?
99	mgo	650.00	60	4.5	2.5	0.090	40	98
100	mgo	670.00	60	10.2	1.4	0.610	40	32
101	mgo	675.00	90	10.8	1.2	0.640	40	53
102	mgo	670.00	60	10.4	1.4	0.640	45	73
103	mgo	600.00	90	10.4	1.4	0.650	40	49
104	mgo	675.00	50	8	2	0.030	40	92
105	mgo	675.00	60	1.8	7.5	0.070	40	80
106	mgo	675.00	75	1.8	7.5	0.500	45	30
107	mgo	690.00	90	2	7.8	0.560	120	107
108	mgo;sto-nb	670.00	90	10.2	1.5	0.600	300	
109	mgo;sto	670.00	90	10.2	1.6	0.660	40	41
110	mgo;sto-nb	670.00	90	10.2	1.7	0.660	60	63
111	mgo	670.00	120	10.2	1.6	0.660	40	62
112	mgo111	640.00	120	10.4	1.8	0.690	40	47
113	mgo	640.00	120	10.4	1.8	0.690	40	54
114	mgo100;mgo111	640.00	120	10.4	1.8	0.690	40	62
115	mgo	650.00	100	10.4	1.8	0.700	40	44
116	mgo	650.00	100	10.4	2	0.740	40	38
117	mgo	650.00	100	10.6	1.8	0.730	40	42
118	mgo	650.00	100	10.4	1.8	0.430	40	62
119	mgo	650.00	100	10.4	1.8	0.700	60	65
120	mgo;sto-nb	650.00	100	10.4	1.8	0.700	360	102
121	mgo	650.00	100	10.4	1.8	0.750	120	122
122	mgo	650.00	100	10.4	1.8	0.730	60	60
123	mgo	690.00	100	10.4	1.8	0.737	63	60
124	mgo	670.00	100	10.4	1.8	0.700	60	70
125	mgo	650.00	100	10.4	1.8	0.700	60	58
126	mgo	655.00	100	10.4	1.8	0.730	60	56
127	mgo	640.00	100	10.4	1.8	0.720	75	66
128	mgo	625.00	100	10.4	1.8	0.720	60	58

129	mgo	650.00	100	10.4	1.8	0.720	60	59
130	mgo	640.00	100	10.4	1.8	0.720	60	56
131	mgo	660.00	100	10.4	1.8	0.700	60	60
132	mgo	660.00	100	10.5	1.7	0.750	60	64
133	mgo	660.00	100	10.3	1.9	0.730	60	58
134	mgo	660.00	100	10.3	1.9	0.730	60	48
135	mgo	665.00	100	10.4	1.8	0.710	60	67
136	mgo	660.00	100	10.5	1.8	0.760	60	63
137	mgo;sto-nb	660.00	100	10.5	1.8	0.730	60	65
138	mgo;sto-nb	657.00	100	10.4	1.8	0.730	60	65
139	Sto-nb	660.00	100	10.4	1.8	0.700	360	
140	mgo;sto-nb	650.00	100	10.4	1.8	0.750	60	54
141	mgo;sto-nb	670.00	100	10.4	1.9	0.740	60	57
142	mgo	660.00	100	10.4	1.8	0.770	60	53
143	Sto-nb	660.00	100	10.4	1.8	0.730	300	
144	mgo;sto-nb	660.00	100	10	2	0.750	60	51
145	mgo;sto-nb	660.00	100	11	1	0.700	60	57
146	mgo;sto-nb	660.00	150	10.5	2	0.770	60	88
147	mgo	650.00	100	10.4	1.8	0.730	60	52
148	Sto-nb;mgo	660.00	200	10.5	2	0.760	40	90
149	Sto-nb	660.00	150	10.5	2	0.83	340	
150	Sto-nb	680.00	150	9	1.8	0.64	335	
151	lao	660.00	150	10.5	2	0.788	40	
152	Sto-nb	400.00	100	8.4	4.2	0.020	120	
153	mgo;lao	620.00	100	8.4	4.2	0.022	15	78
154	mgo;lao	635.00	100	8.4	4.2	0.022	15?	70
155	Sto-nb	635.00	100	8.4	4.2	0.017	15	79
156	Mgo;sto-nb	660.00	100	8.4	4.2	0.019	15?	77
157	mgo;sto-nb	600.00	100	8.4	4.2	0.022	15	78
158	mgo;sto-nb	720.00	100	8.4	4.2	0.022	15	77
159	Sto-nb	720.00	100	8.4	4.2	0.021	90	
160	mgo	780.00	100	8.4	4.2	0.022	15	74
161	Sto-nb	720.00	100	8.4	4.2	0.025	90	
162	mgo	740.00	100	8.4	4.2	0.023	15	74
163	mgo;lao	740.00	100	9.4	3.5	0.023	15	86
164	Sto-nb	740.00	100	9.4	3.5	0.025	90	
165	Sto-nb	740.00	100	9.4	3.5	0.025	90	

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